

California State University, Northridge
ECE 520L - System on Chip
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Lab 1
First Design on Zynq

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Instructor: Saba Janamian

Troy Israel

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Introduction

The purpose of this experiment was to get familiar with Vivado and Vitis softwares and understand their design flow. We will be creating both a Vivado IP block diagram and exporting it to Vitis. Vitis will allow the Zynq processor to integrate with the IP implementation that was created in vivado. Connecting the hardware server will allow Vitis to work with Zynq processors.

Procedure

The first step is to create a Vivado project. I then set up the project to be configured with the Zybo Z7-10 board. Next I added a block design from the IP Integrator and used the ZNQ Processing System. Once the block design was placed, I then ran the Run Block Automation. It created the following connections, DDR and Fixed_io. I then selected the AXI GPIO and selected the S_AXI so that the GPIO would be connected to the Zynq.

The next step was to set up the GPIO interface so that would configure the LEDs. 4 LEDs are going to be used for this lab. Now that a port that contains the LEDs was created I then needed to Validate the design. After the validation was done, I created an HDL wrapper file and generated a bitstream file. After these two types of files were created I could then create a Vitis project

In the Vitis project I created an empty C project. Inside I added the source file that was made earlier. I then went back into the slides to retrieve the C code that was given. After all the C code was written, I built the project to see if all the code would compile.

Once the C code is compiled and built, I then connect the Zybo Z7-10 board to my laptop and have Vitis and Vivado transfer the code onto the board. The board should have the leds flashing on and off if everything done by Vitis and Vivado was done correctly.

Test Strategy

Firstly, I opened the IP Integrator and created a block design. I then added an existing block design called ZYNQ Processing System. I ran the Block Automation so that the system would have the DDR and Fixed_IO would be set up. I then added a GPIO called an AXI GPIO to the design and ran the Connection Automation. I also set the GPIO port to LEDs 4 bits.

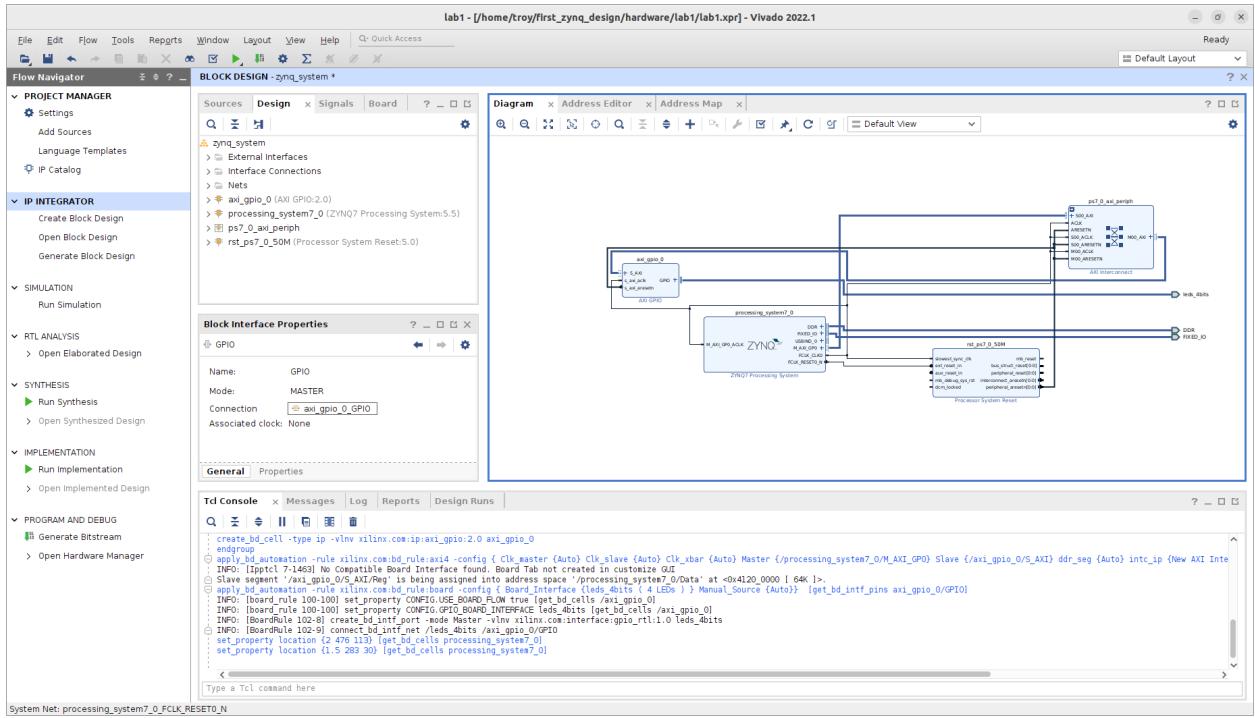


Fig 1.1 Zynq Design System

After the Design was created, I then tested the validation. After it passed the validation, I then created an HDL wrapper file. Then I generated the bitstream so that I could start working on Vitis. I exported the hardware so that an XSA file would be created.

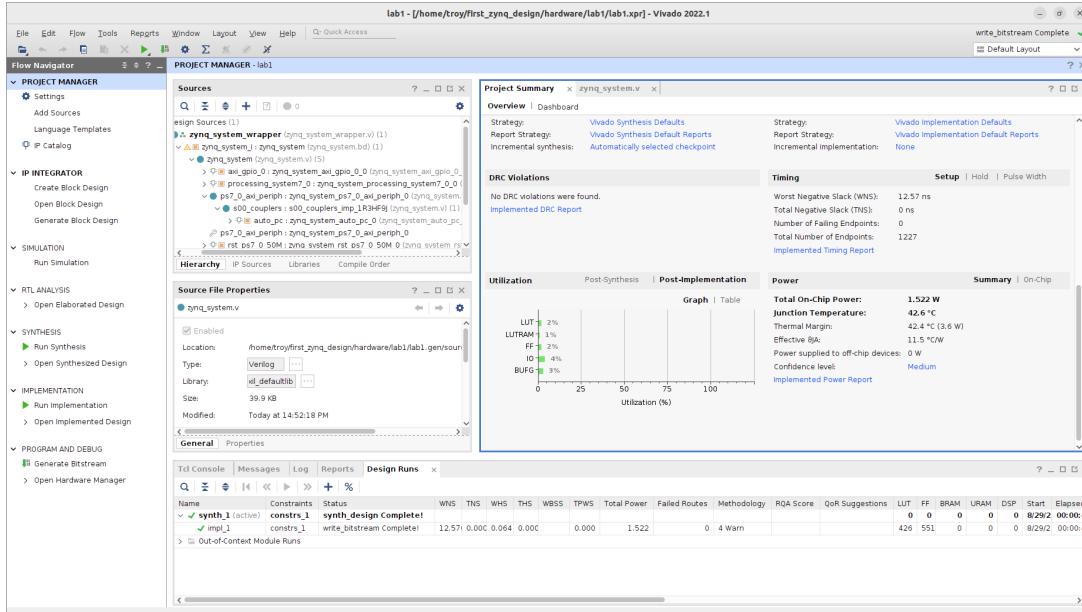


Fig 1.2 Project Summary

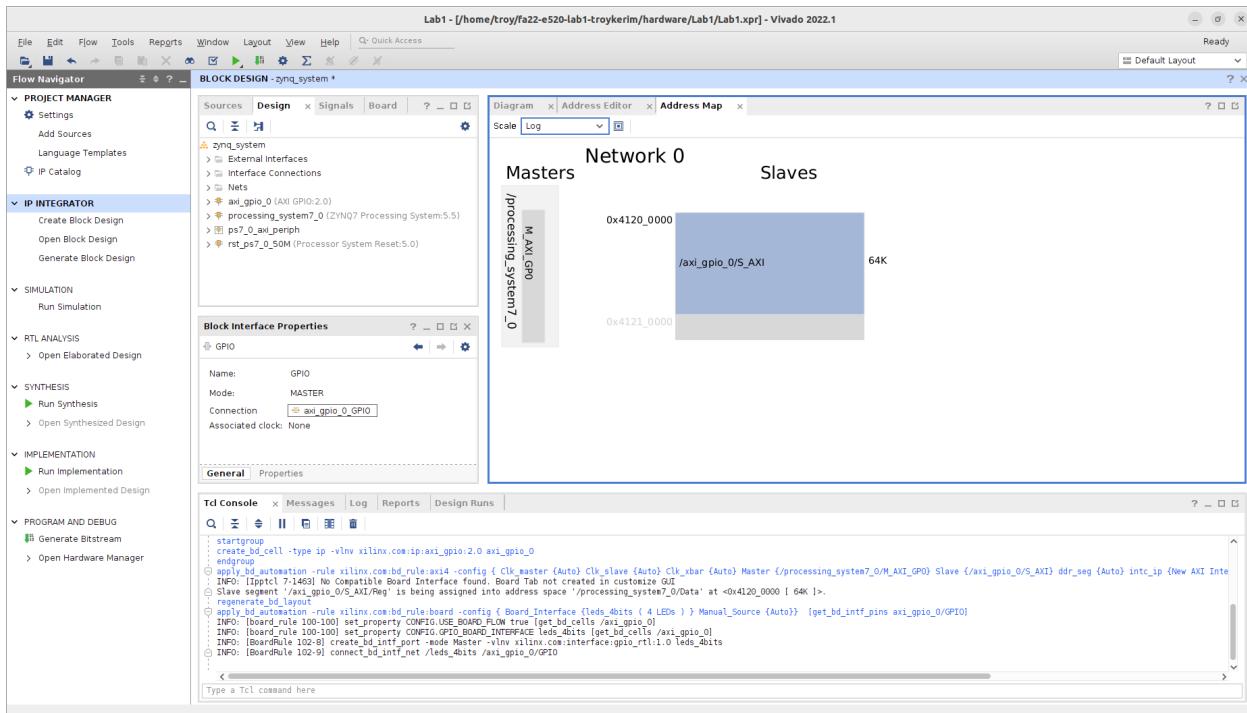


Fig 1.3 Address Map

On Vitis I created the project using the XSA file that was made in vivado. I then made an empty C application and typed in the C code that was in the slides. I built and compile the C code to verify that there were no errors.

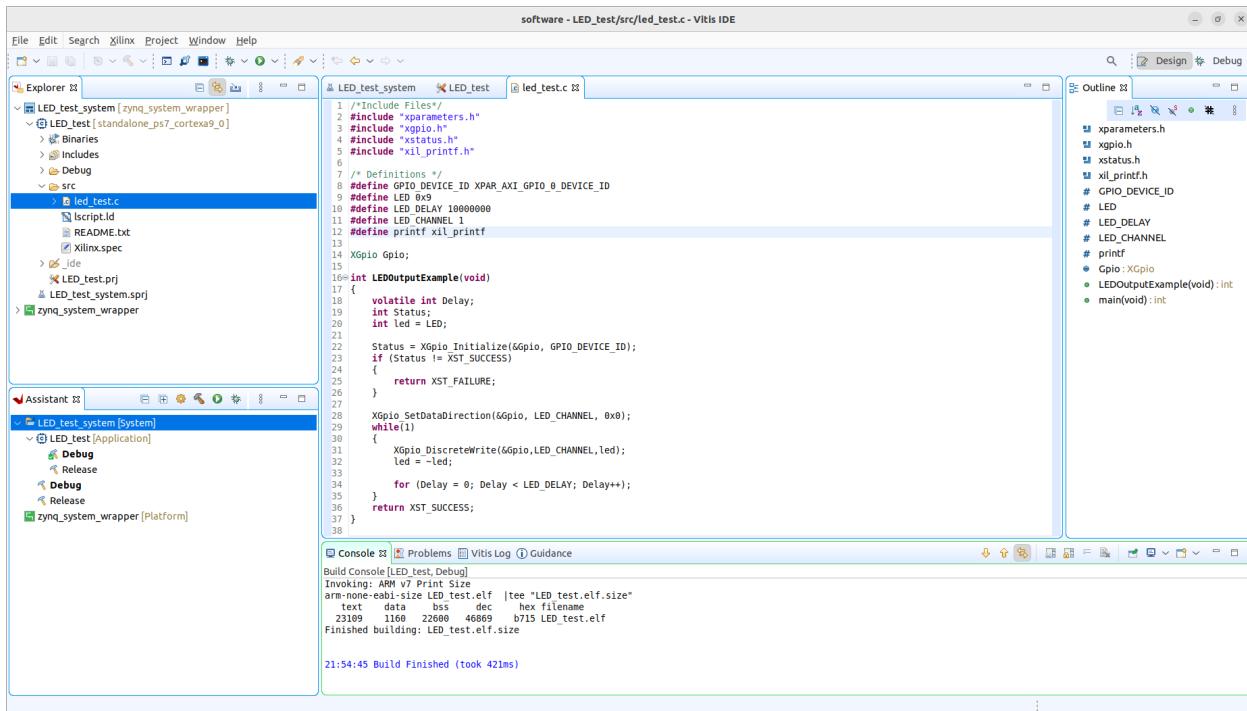


Fig 1.4 Compiled C Code

Results

On Vitis I connected the cable from my FPGA board to my laptop. I then went to the Xilinx tab and selected “Program Device”. It loaded the project onto the board and the board had Program LED set to green to indicate that my project was loaded onto the board. Next I ran the LED_test file and the LEDs on the board began alternating on and off.

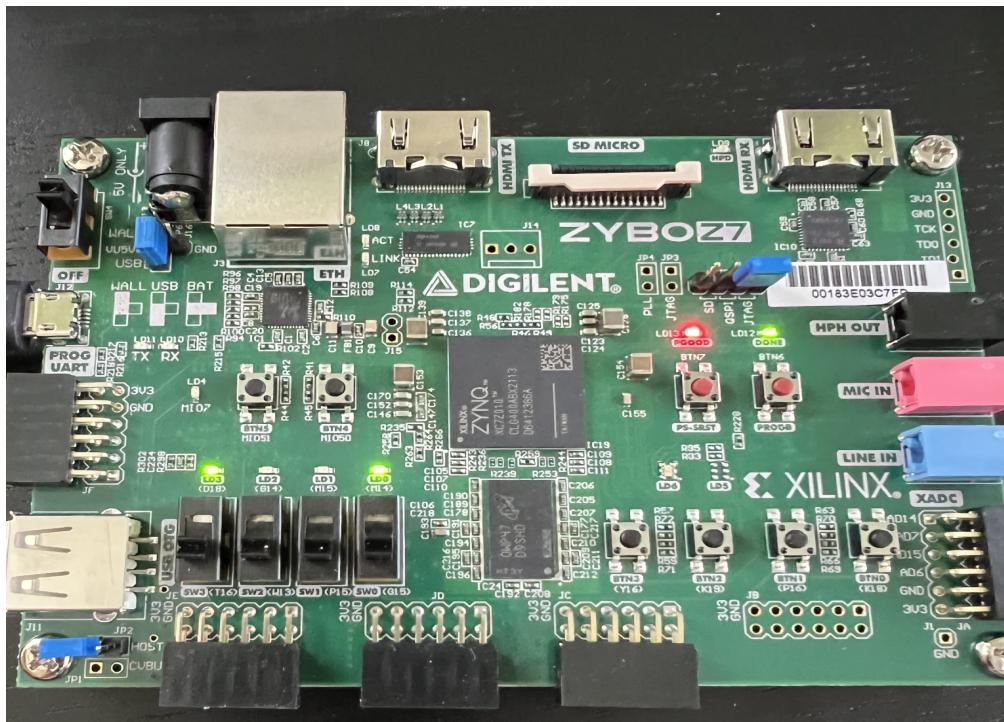


Fig 1.5 LEDs flashing on Zybo board

Conclusion

In this lab I learned how to create a Vivado project, specifically creating IP block diagrams and connecting them together. I also learned how to generate a Bitstream and HDL wrapper file. I also learned how to create a Vitis Project and integrate HDL wrapper file and bitstream with that project as well. While working on this lab I did notice that initially I was not using the given file from github. I did fix the issue and restarted the lab with the correct file name so I wouldn't have to do any extra steps with the TCL commands. I also ran into an issue with a driver problem, where the cable wasn't set up correctly on my Ubuntu laptop. Initially the Zybo board was not working, but after finding the right driver it finally worked.

Appendix

<https://github.com/csun-ece/fa22-e520-lab1-troykerim>