California State University, Northridge
ECE 520L - System on Chip
Fall 2022

Lab 7: Zybo Z7 HDMI Input/Output

October 22nd, 2022
Instructor: Saba Janamian

Troy Israel

IP MODULES:

AXI4-Stream Subset Converter:

This IP is a collection of modular cores that can be used to connect AXI4-Stream master and slave Ip systems in an effiecent manner. All the modules have AXI4-stream master and slave interfaces that allow them to be daisy-chained together. The IP collection proves a common set of functions including buffering, transforms and routing. The subset converter provides clock crossing logic to bridge two domains. It provides TDATA/TUSER remapping functionality. It allows streams with different signal sets to be connected. It also allows for programmable TLAST to be generated and add signals based on default value rules. The Subset converter allows masters and slaves with varying AXI4-Stream characteristics to exchange in AXI4-Stream transfers.

Video in to AXI4-Stream:

This IP converts incoming video with explicit sync and timing to the AXI4-Stream Video protocol to interface with the Xilinx video processing cores that use this protocol. The Video In accepts video inputs and a pixel clock and uses the following sets of timing signals: Vsync, Hsync, Vblack, Hbalck and Data Valid. Here I put the middle configuration but it can accept 3 sets, 5 sets or 7 sets. Any of these sets of signals is enough for the operation of this IP core. The output side of the core is an AXI4-Stream that will interface in master mode. This interface consists of parallel video data, tdata, handshaking signals tvalid and tready and finally two flags, tlast and tuser. These interface connections will identify certain pixels in the video stream. The core is designed to be used in parallel with detector functionality of the VTC. The video timing detector detects the line standard of the incoming video, and makes the detected timing values, such as the number of active pixels per line and the number of active lines available to video processing cores downstream of the Video In to AXI-Stream core via an AXI4-Lite interface.

Video Timing Controller:

The video timing controller serves the function of both detecting and generating these timing signals. The input side of the core automatically detects horizontal and vertical synchronization pulses, polarity, blanking timing and active video pixels. On the outputs it generates the horizontal and vertical blanking and synchronization pulses used with a standard video system including support for programmable pulse polarity. The core is commonly used with the Video in to AXI4-Stream core to detect the format and the timing of incoming video data or with the AXI4-Stream to Video out core to generate outgoing video timing for downstream sinks such as a video monitor. Video systems may utilize different combinations of blank, synchronization or active signals with various polarities to synchronize processing and control video data.

Links:

Github: https://github.com/csun-ece/fa22-e520-lab7-troykerim
Youtube: https://youtube.com/shorts/MH_NCeZwgsw?feature=share