Lab 3 - Where No Clock Has Gone Before

Embedded Systems 1
Lab Report 3
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Part 1:

Purpose

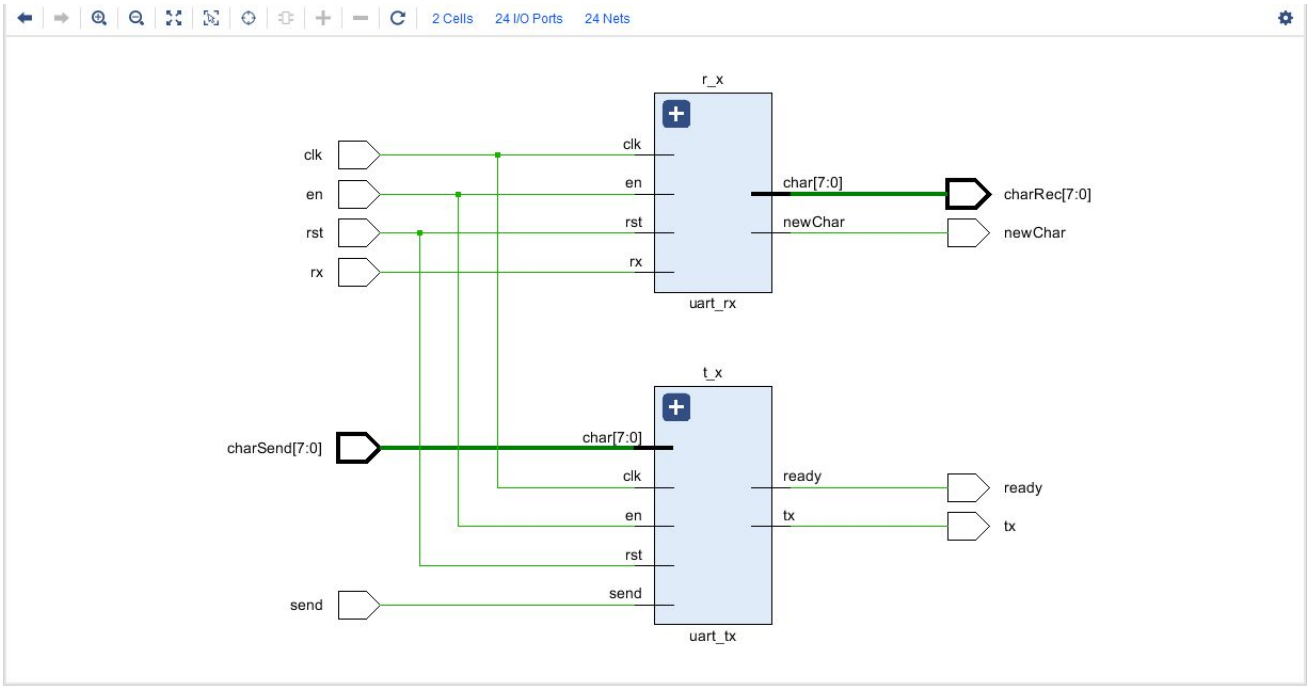
Create an entity called uart tx with the following interface that sends data using the protocol in figure (3.1) with 8 data bits, 0 parity bits, and 1 stop bit. See listing (3.1) for entity description. It should have the following behavior:

- When rst is asserted, all internal registers are cleared and it goes into an idle state
- When it is in the idle state, ready is 1
- When send is asserted and enable is 1 and the clock is on a rising edge, it stores char into a register and begins the sequence of sending data

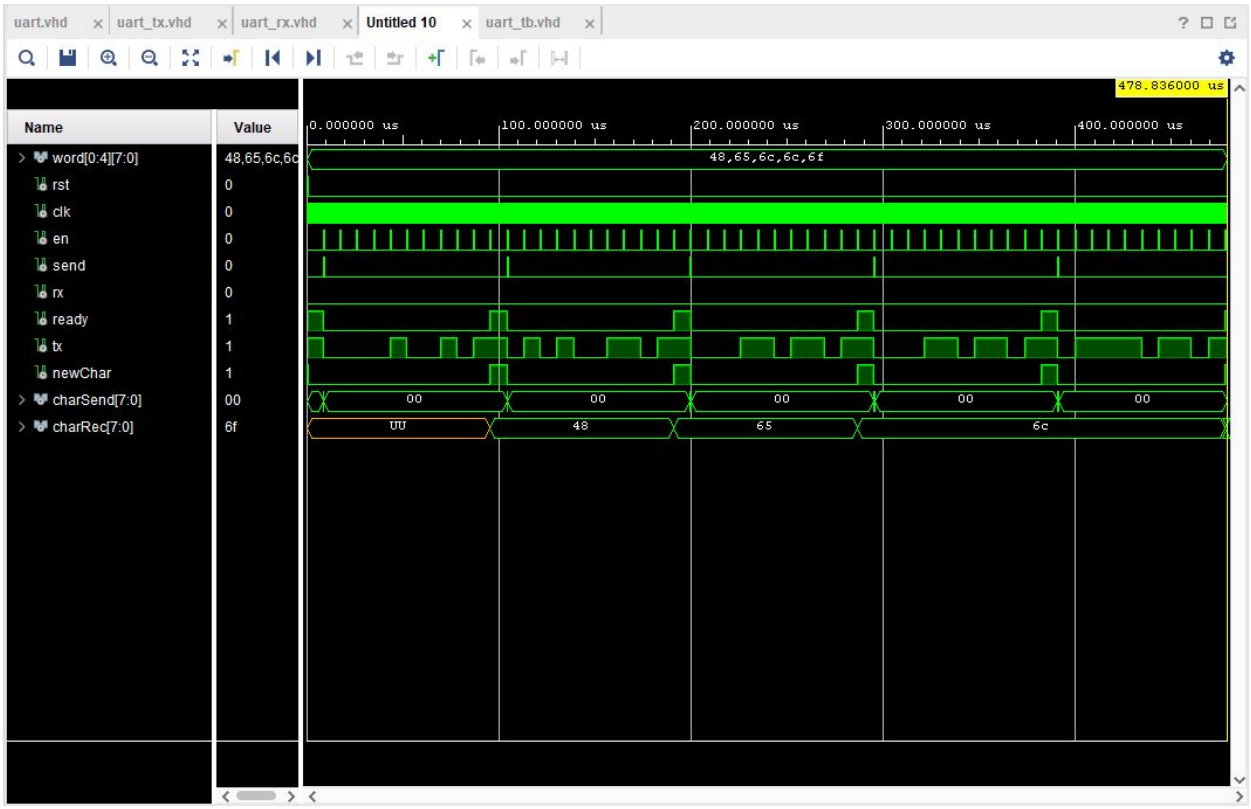
Uart_tx.vhd

Code is on github: trp87-rutgers

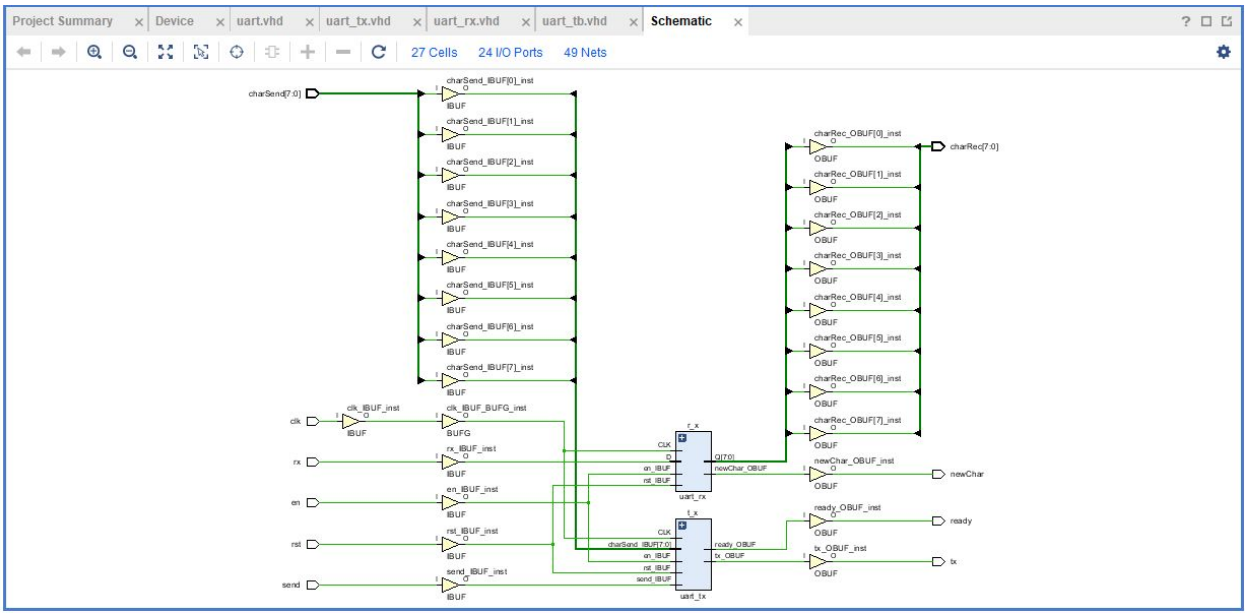
RTL Schematic



Simulation Waveform



Synthesis Schematic:



Post Synthesis Utilization Table

On Chip Power Graph

Part 2:

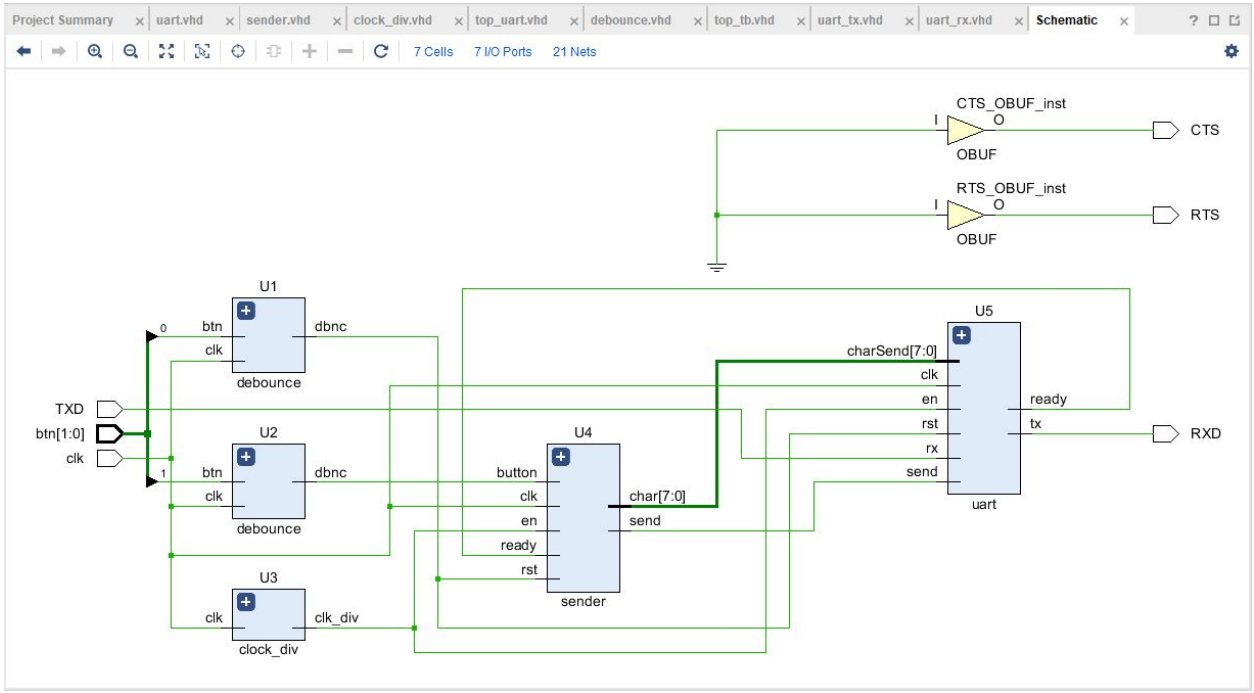
Purpose

Purpose of this part is to successfully combine the previous debounce, and modified clock div, with the new sender, and uart to communicate ‘trp87’ serially over a wire RXD.

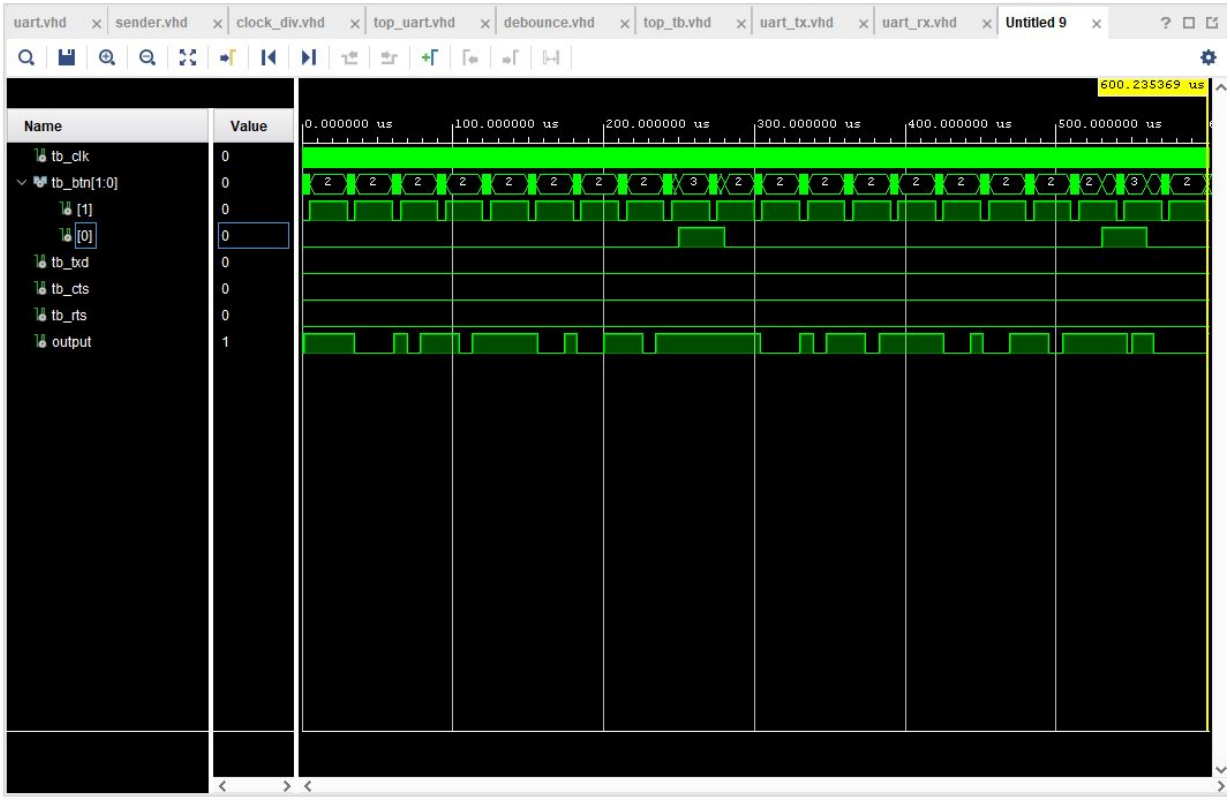
Top_uart.vhd

Code is on github for all files including test bench: trp87-rutgers

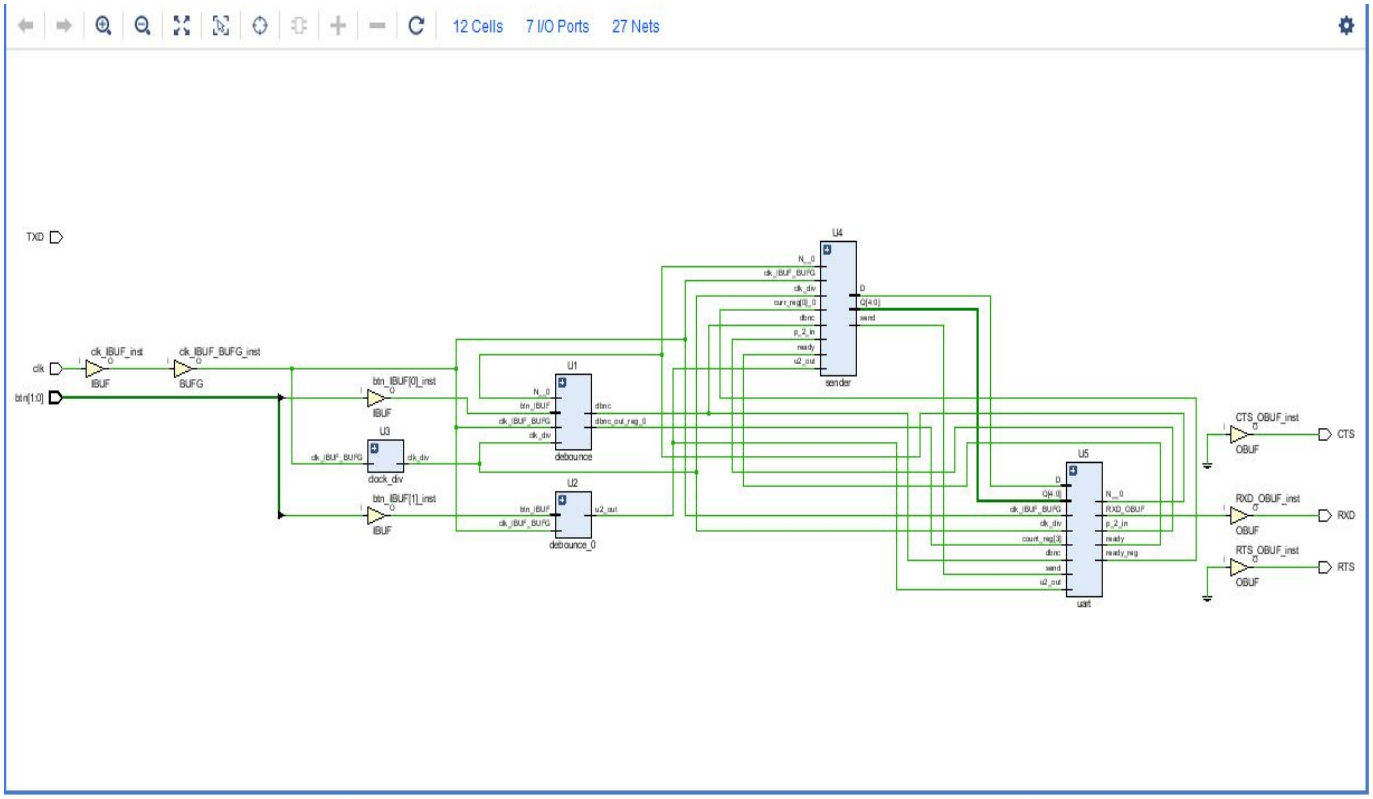
RTL Schematic



Simulation Waveform



Synthesis Schematic:



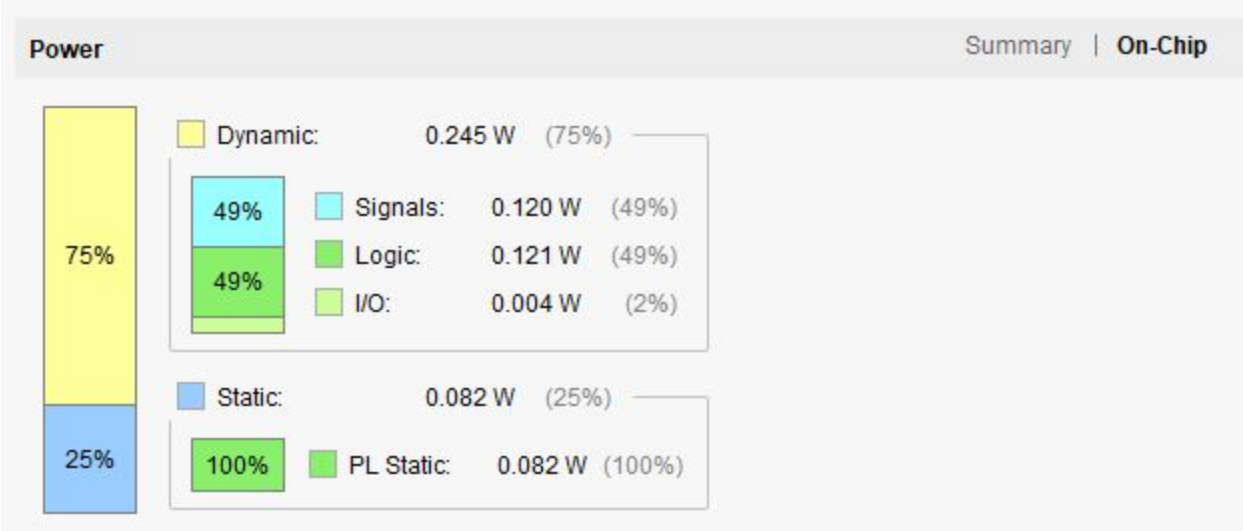
Post Synthesis Utilization Table

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization %
LUT	47	41000	0.11
FF	64	82000	0.08
IO	6	300	2.00
BUFG	1	32	3.13

On Chip Power Graph



I learned how to successfully implement a UART communication device, and using my first PMOD in a project (‘sort of’).