Embedded Systems Design

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Lab 0: Introduction to Vivado

1 Introduction

In this lab, we will be introducing the concepts of counters and constraints through the study an manipulation of a simple vhdl entity called "blinker." Blinker behaves in a similar fashion as the directional light in a car. When Switch 0 (sw0) is flipped, LED 0 (led0) begins blinking at a rate of 1Hz.

Please download the following files from Sakai

- blinker.vhd
- blinker_tb.vhd
- zybo_blinker.xdc

2 Setup and Analysis

To open the Vivado GUI inside Linux, type the following commands into the terminal:

```
cd /opt/Xilinx/Vivado/2016.4
source settings64.sh
./bin/vivado
```

1. Create a Vivado project called "blinker."
2. Import the files downloaded from Sakai.
3. Inspect the imported vhdl.
4. Simulate. Set the simulation run time as 2.5 seconds. Inspect the simulation waveforms.
5. Elaborate. Inspect the RTL schematic.
6. Synthesize. Inspect the schematic.
7. Implement and generate the bitstream.
8. Program the ZYBO.

Note: For help creating a Vivado project and performing the above tasks, please refer to the first introductory lab

Questions

Please answer the following questions:

1. Why did we simulate the design for such a long period of time?
2. What was the counter doing before the switch went high? What was it doing after the switch went high?
3. Why do you think the count value was set to 124999999?
4. Comparing the imported vhdl code and simulation results, do you think the simulation behaves as expected? Why or why not?

3 Modification

For this next section, you will modifying the xdc and vhd files to alter the behavior of the design as follows:

1. Change the vhd file so that the led blinks at a rate of 2 Hz as opposed to 1 Hz.
2. Make any necessary changes to the vhd and XDC files so that the LED 3 blinks as opposed to LED 0.
3. Make any necessary changes to the vhd and XDC files so that the Switch 3 is used to control the blinking as opposed to Switch 0.
4. Simulate. Inspect the simulation waveforms. If your modified design does not meet the new design criteria, repeat the above steps until you are successful.
5. Elaborate. Inspect the RTL schematic.
6. Synthesize. Inspect the schematic.
7. Implement and generate the bitstream.
8. Program the ZYBO.

Questions

Please answer the following questions:

1. What is the new counter value? Why?
2. Besides the count value, what else (if anything) did you have to change in the design to successfully complete the design modifications?
3. In what ways (if any) did the RTL and Synthesis schematics change?