EE493 Embedded Systems Hardware/Software Fall 2017

Lab Report Format

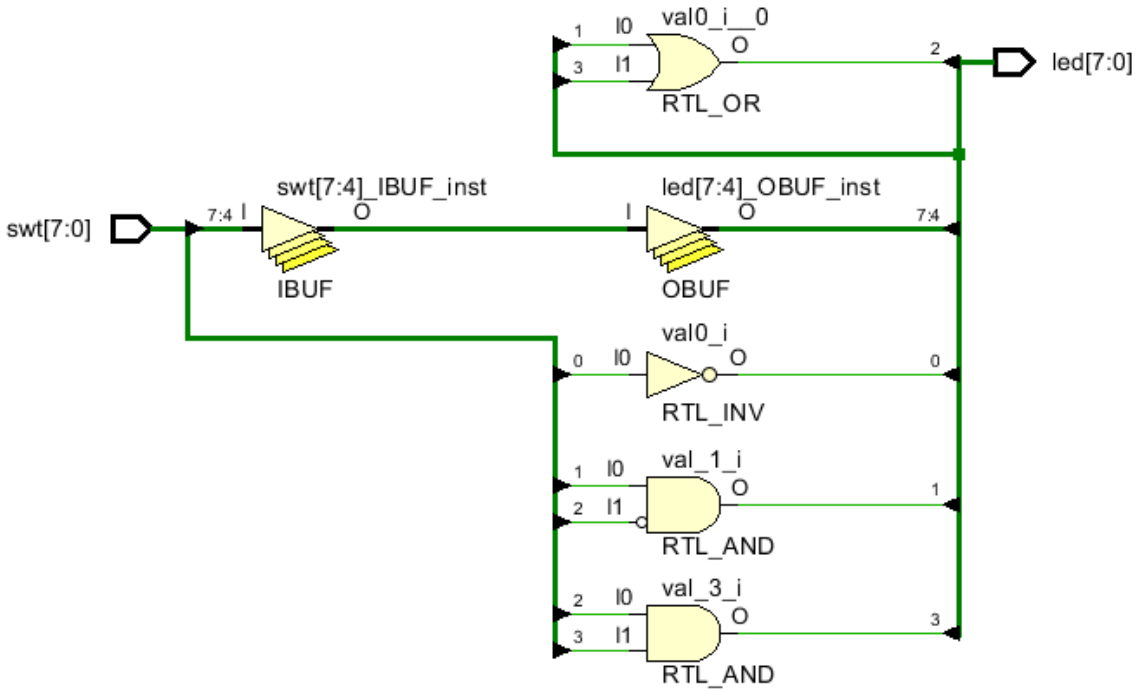
Using your favorite desktop publishing tool, write a report with the following sections. Save your work as a PDF and submit using Sakai. Length will vary by lab and student's effort.

- Title
  - Class Name
  - Lab Report #
  - Student Name
  - Submission Date
- Purpose
  - What is the intent of the lab, to design, test or implement a/an xyz?
- For Each Part
  - Theory of Operation
    - How will or should the circuit behave?
    - What do you expect to happen?
  - Truth Table (as needed)
  - Schematic Diagram (as desired)
  - Design
    - VHDL Code
  - Test
    - Test bench VHDL (if required)
    - simulation results (screen shots)
  - Implementation (If required to demo on board)
    - Vivado Elaboration Schematic - Screenshot
      - See Example Below
    - Vivado Synthesis Schematic - Screenshot
      - See Example Below
    - Vivado Project Summary Images
      - Post-Synthesis Utilization Table
      - On-chip Power Graphs
    - XDC file
      - Explain what had to be changed and why
- Discussion
  - Answers to specific Lab Manual questions
  - Observations / Discoveries
    - What did you learn?
  - Questions / Follow Up
    - Which concepts do you completely understand?
    - Any concept you're unsure of?

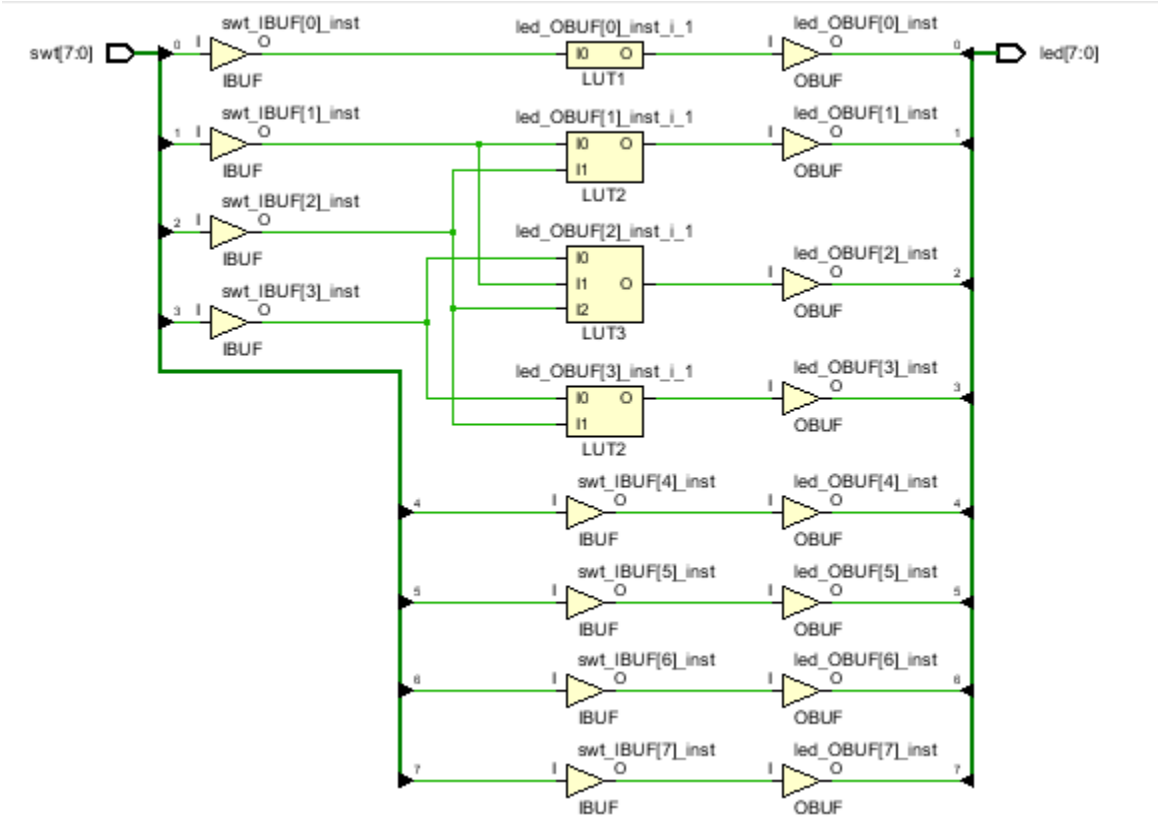
Phil Southard

PTL EE493 - Fall 2017

Elaboration Schematic



Synthesis Schematic



Power Graphs and Utilization Table

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	3	17600	0.02
IO	16	100	16.00