Lab 5 - It's all about the Processors

Embedded Systems 1
Lab Report 5
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Purpose

In this lab, we are going to use almost everything we have learned and created thus far in order to make the most recognizable design in all of ECE; a processor. Our design is a general purpose processor with some application specific instructions for video and communications. In this way, it is similar to a simplified Application-Specific Instruction-Set Processor (ASIP)

Notes:

All vhd, xcd, coe, tb and all other files needed to complete the lab including the bit file is on github.

Part 1

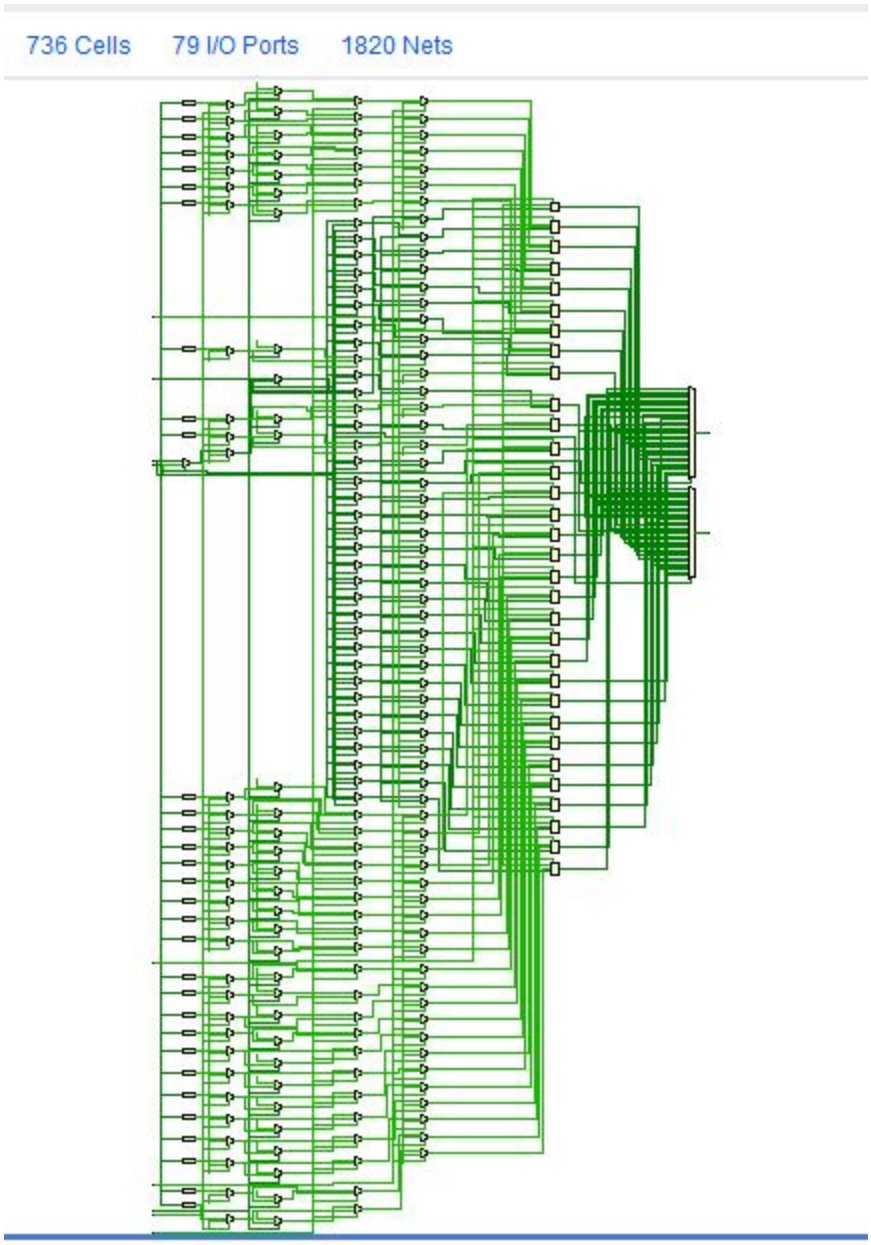
Coe files are attached on Github
Modified txt file is attached on Github

Part 2

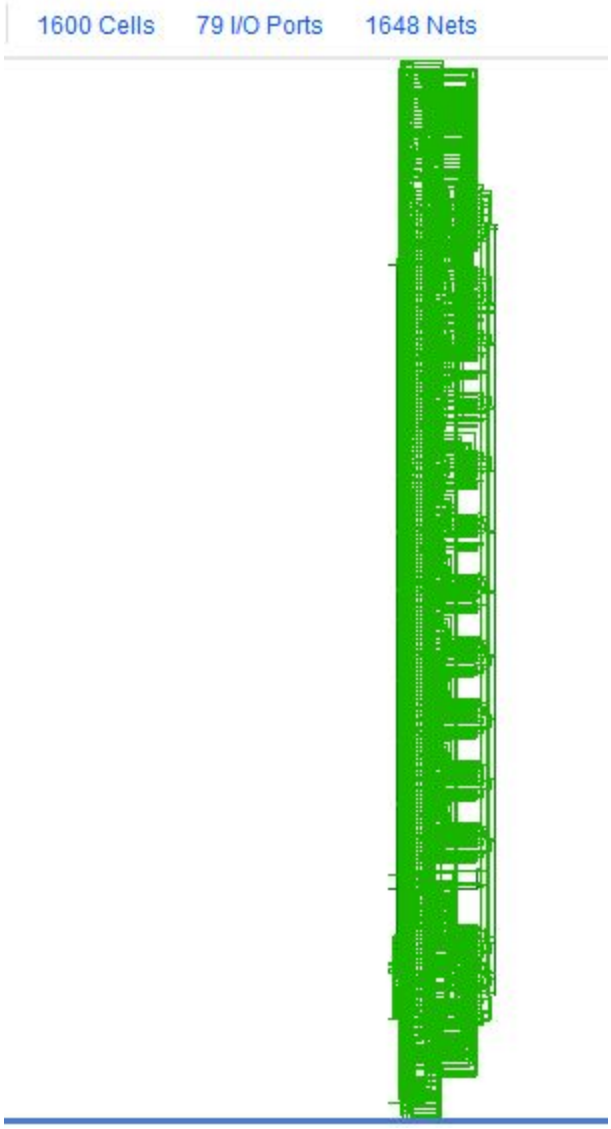
Regs

Code is on Github

RTL Schematic



Synthesis Schematic



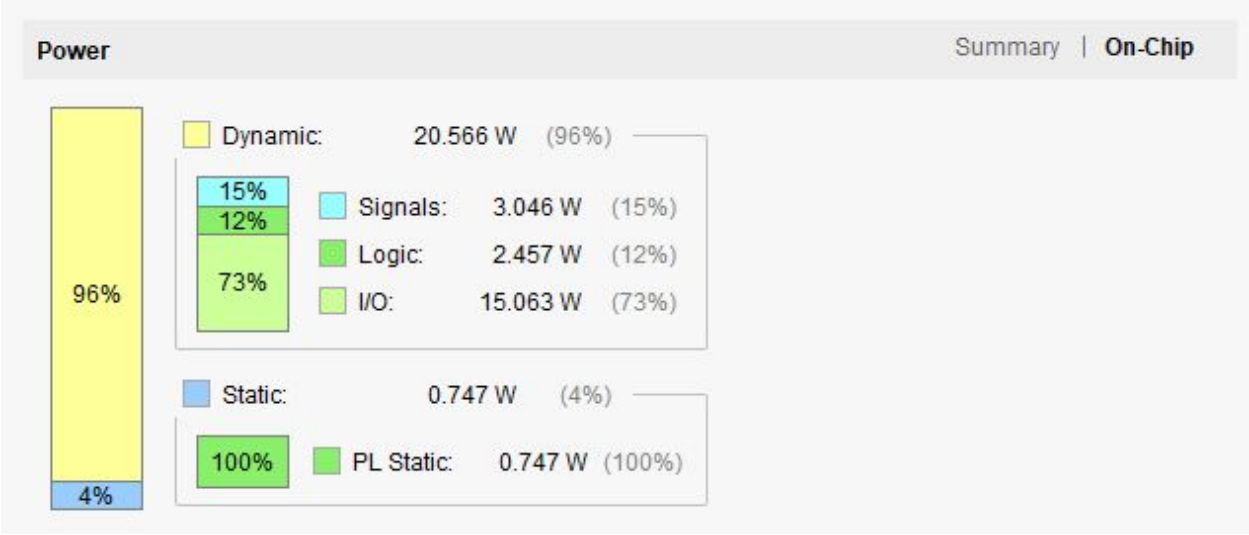
Post Synthesis Utilization Table

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization %
LUT	834	17600	4.74
FF	512	35200	1.45
IO	79	100	79.00
BUFG	1	32	3.13

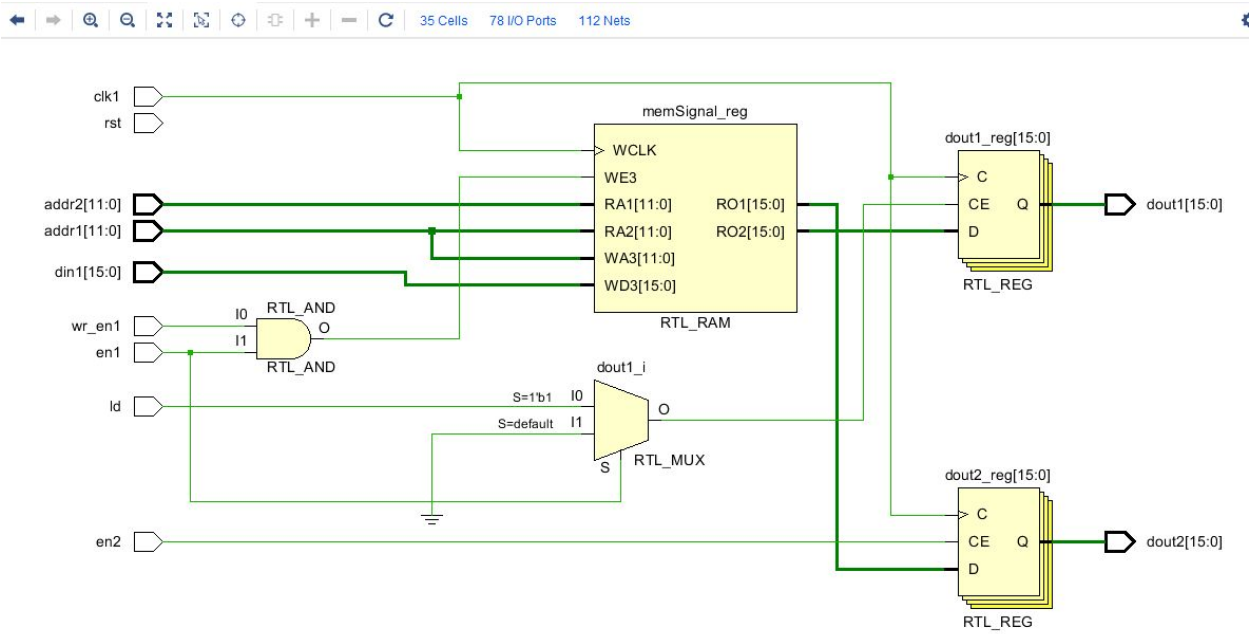
On Chip Power Graph



Framebuffer

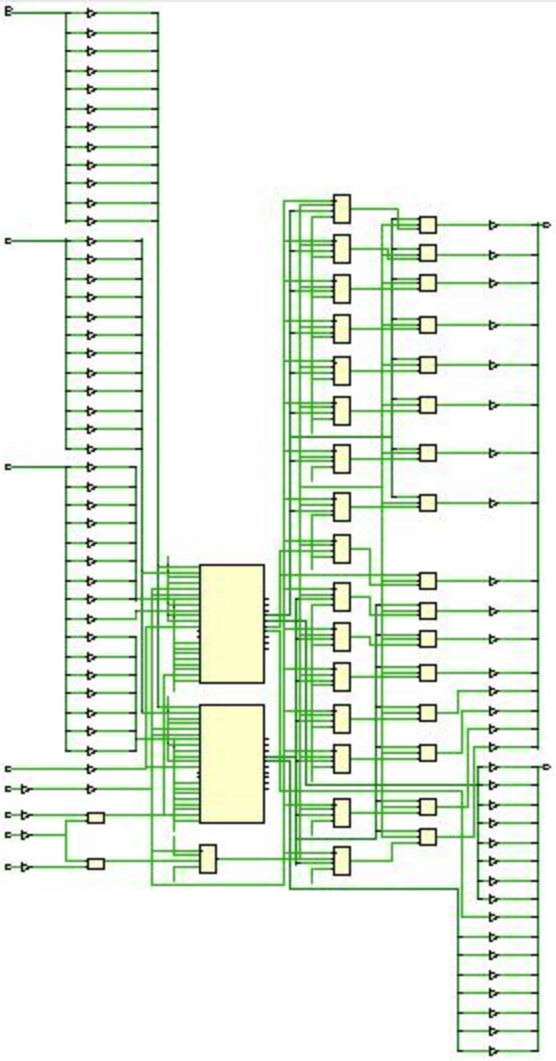
Code is on Github

RTL Schematic



Synthesis Schematic

115 Cells 78 I/O Ports 192 Nets



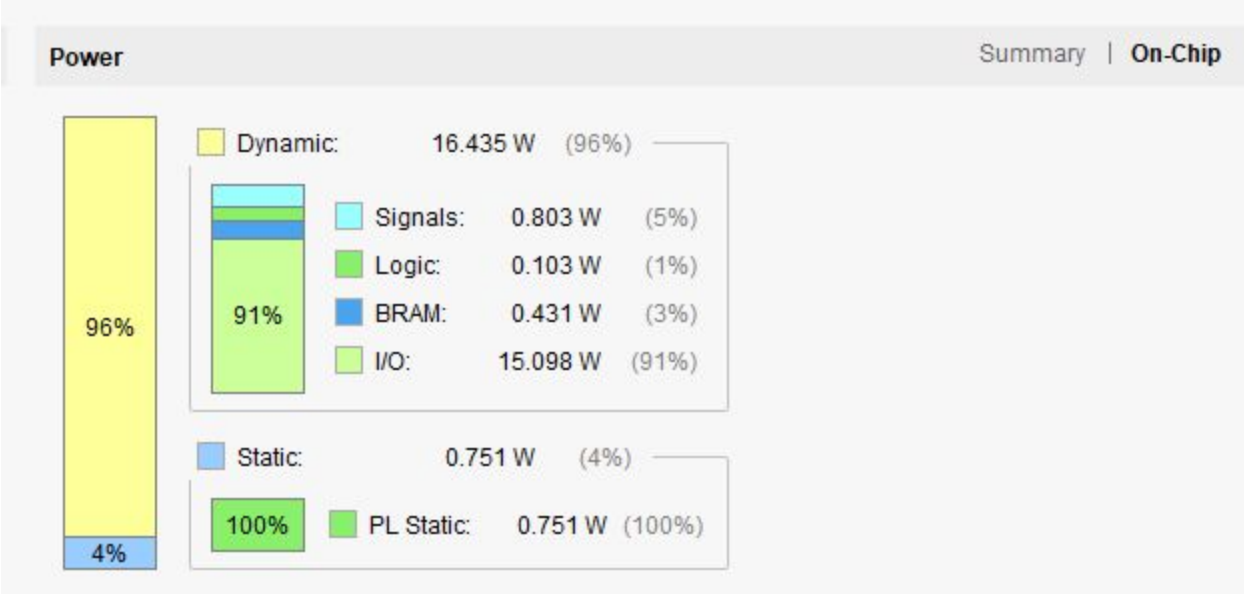
Post Synthesis Utilization Table

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization %
LUT	10	17600	0.06
FF	17	35200	0.05
BRAM	2	60	3.33
IO	77	100	77.00
BUFG	1	32	3.13

On Chip Power Graph

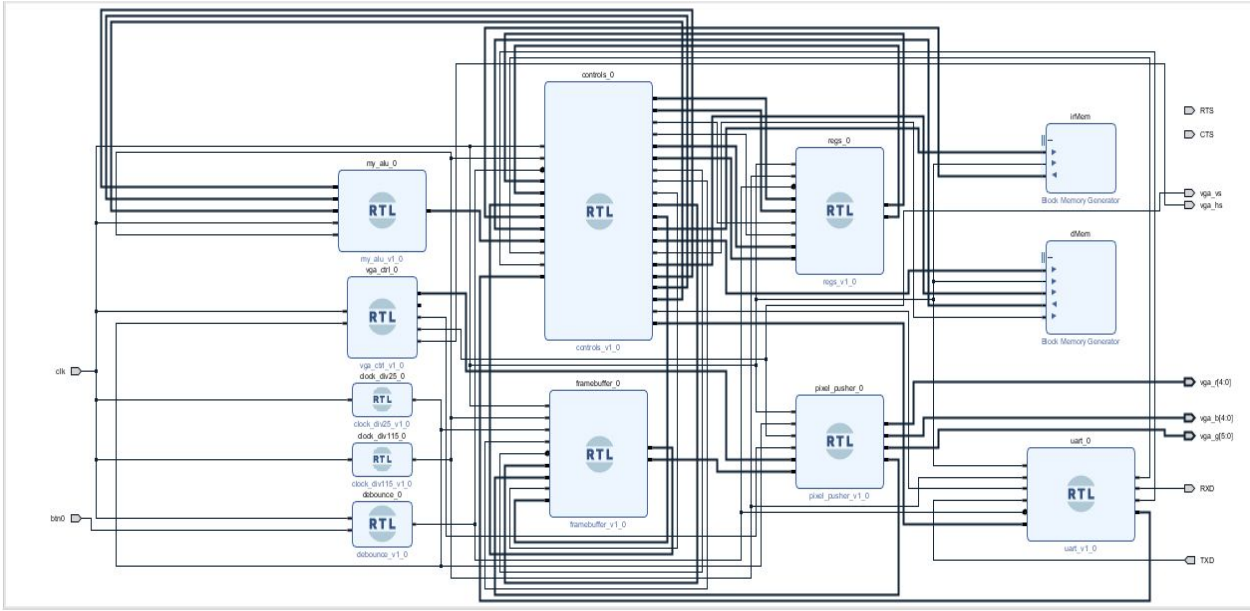


Part 3

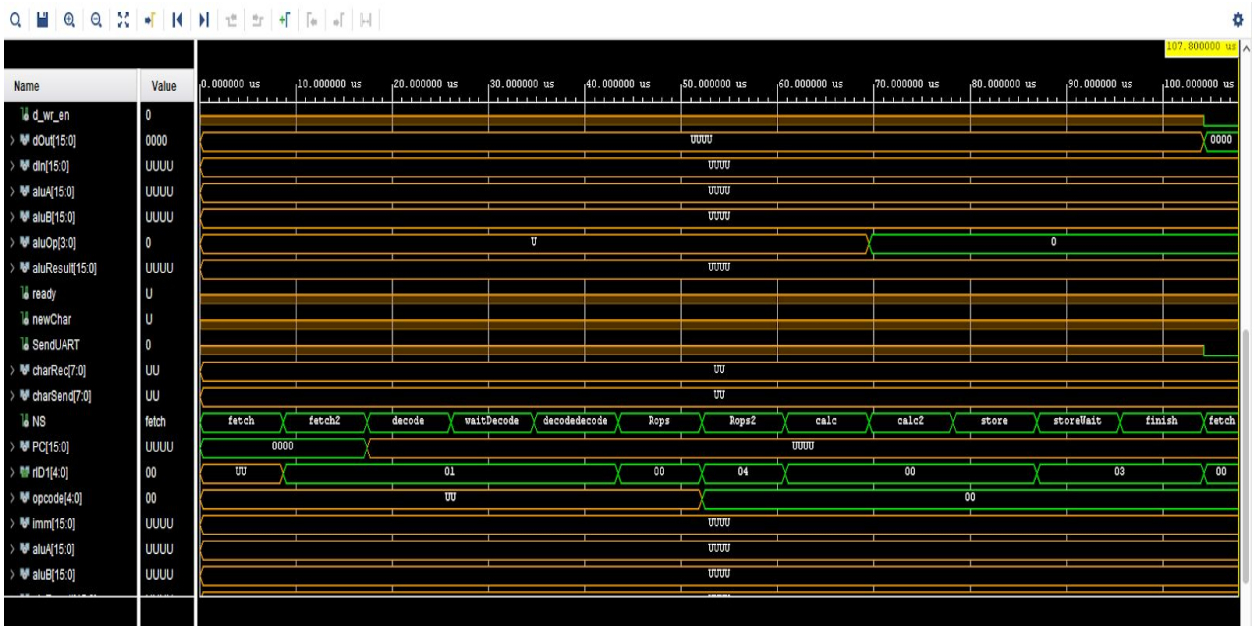
Top

Code is on Github

Block Diagram



Simulation Waveform of just Controls.vhd



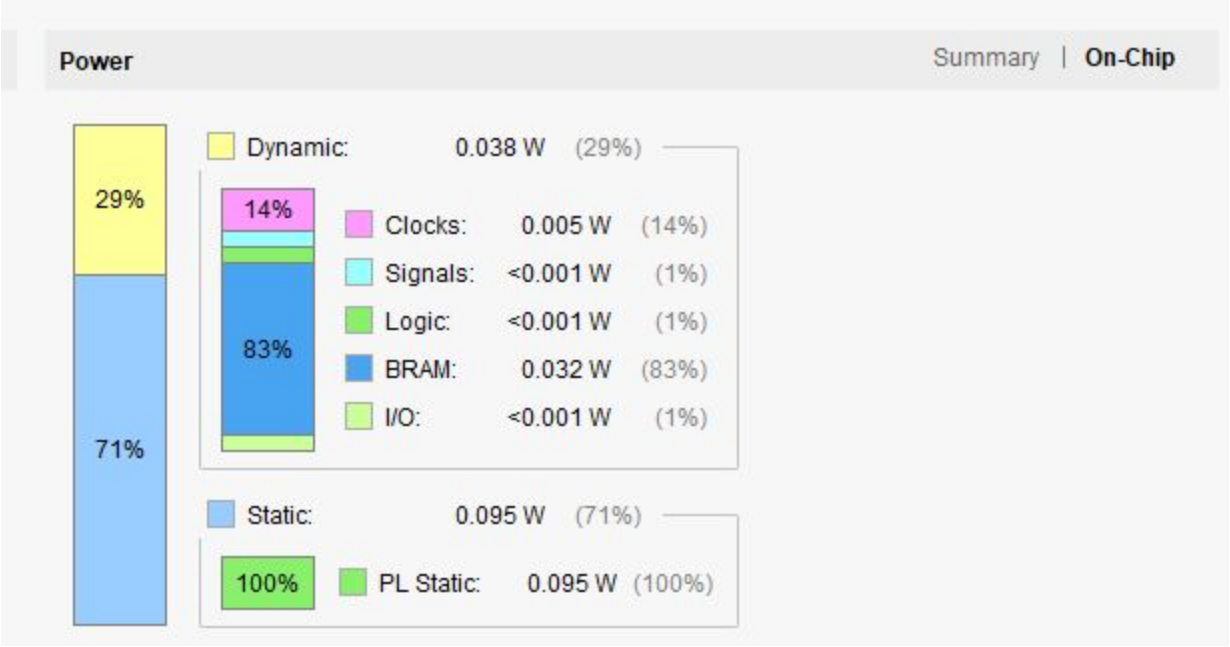
Post Synthesis Utilization Table

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization %
LUT	4	17600	0.02
IO	24	100	24.00

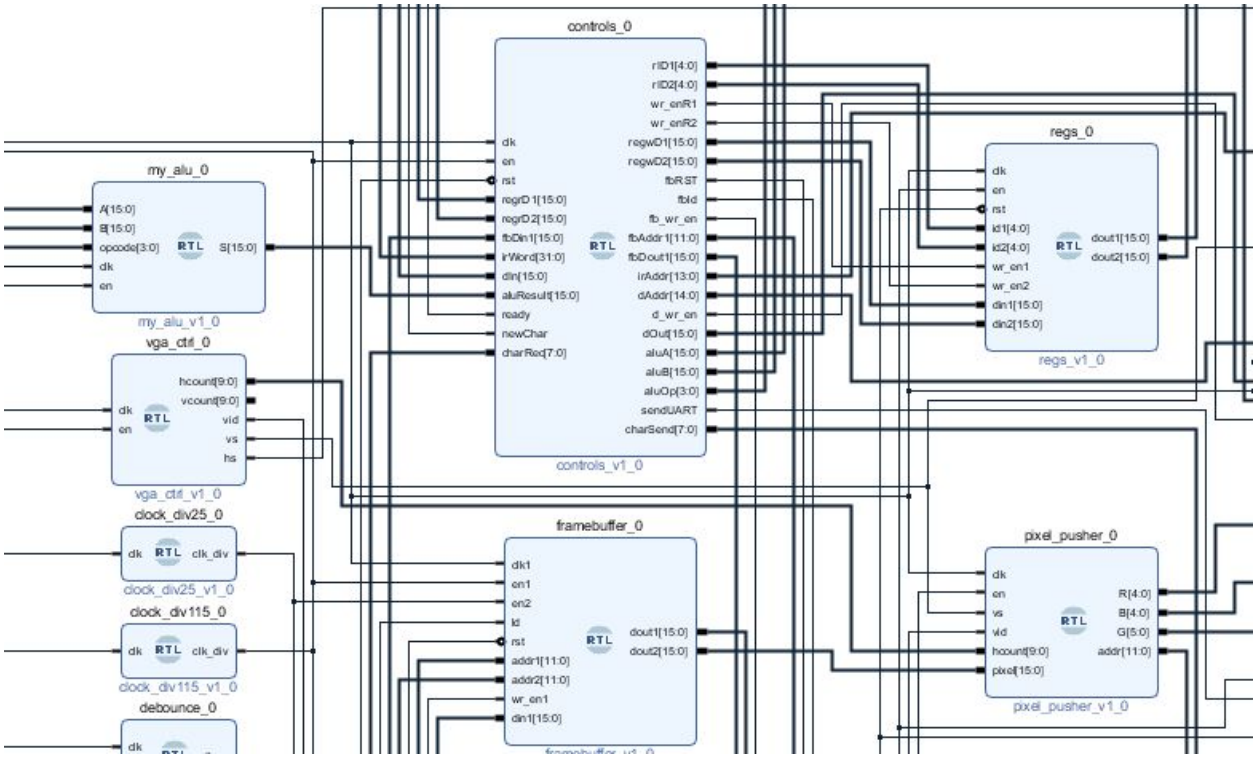
On Chip Power Graph



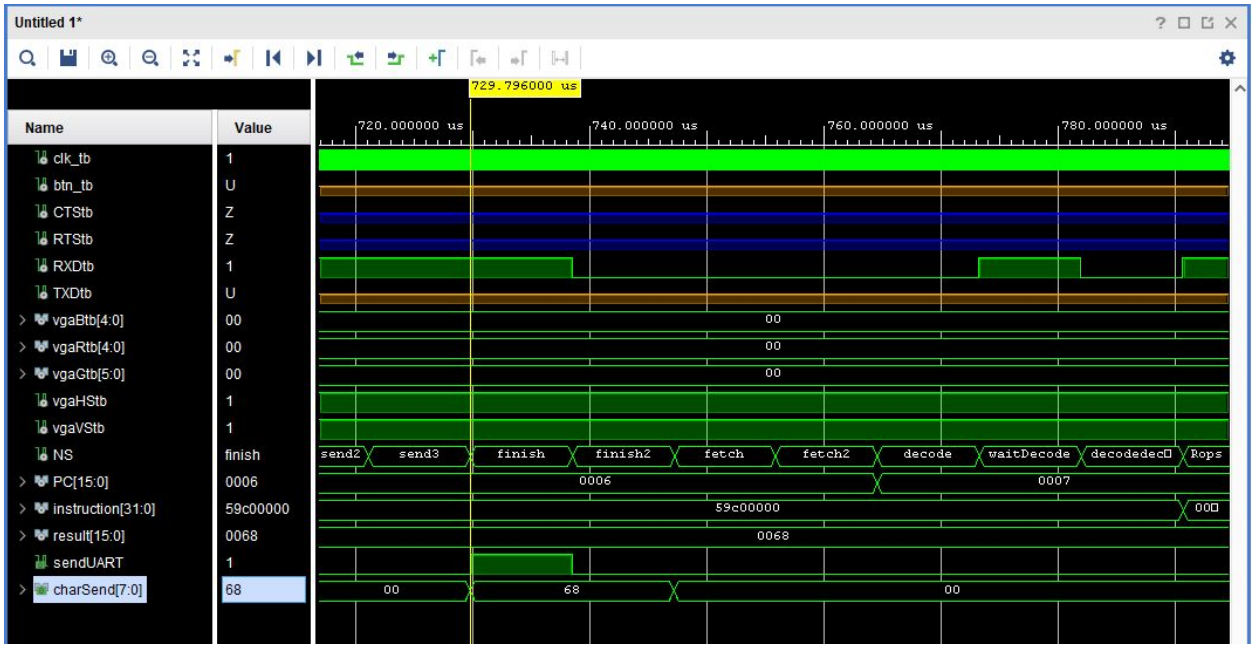
Part 4

HDL Wrapper code is on Github
XDC file on Github

Close up of Controls on the block design



Top Level Simulation:



This lab was very cool. Never thought I would ever get to implement an actual processor. Took so many hours of troubleshooting, but it sent over the UART.