University of Victoria

CENG 241

Digital Design I

Lab 7: RAM System

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A01 - B03

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1 Introduction

2 Discussion

Description of how the RAM read and write operations are implemented in the system of Fig. 1.

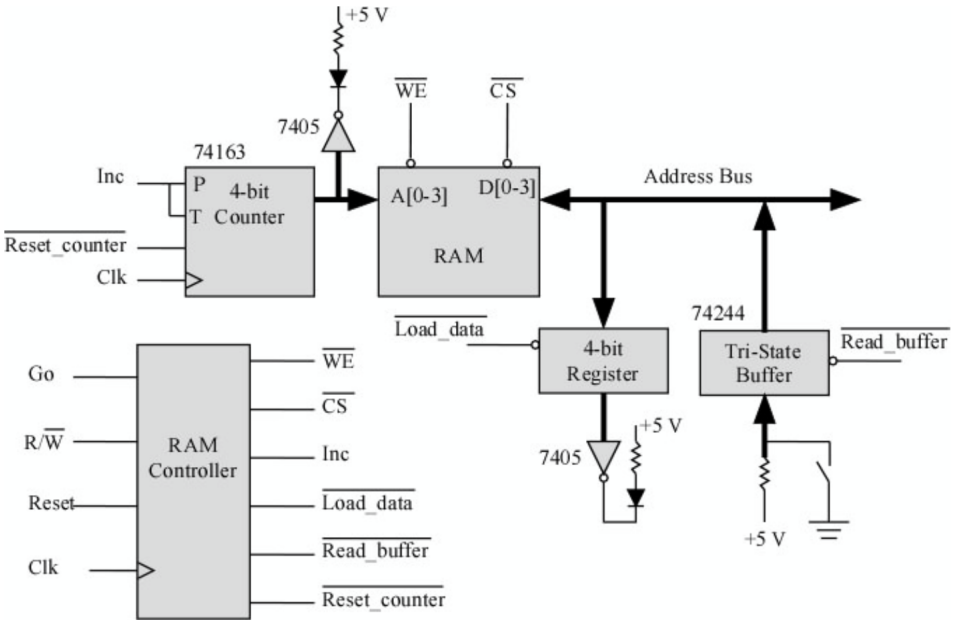


Figure 1: RAM controller and memory system

2.1 Timing considerations

Explanation of the read and write timing diagrams

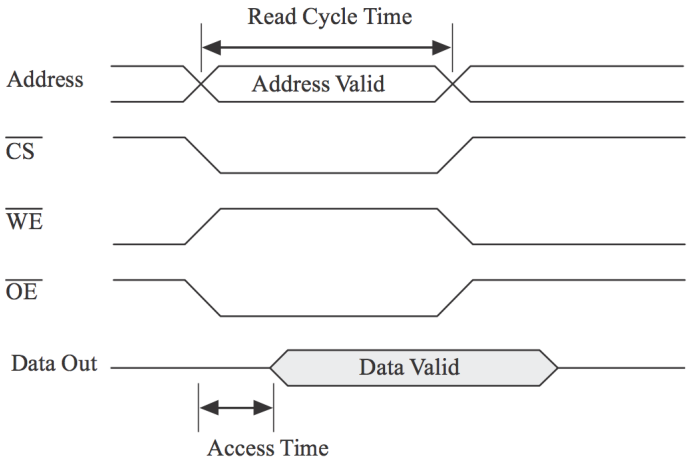


Figure 2: Timing diagram for the RAM read operation

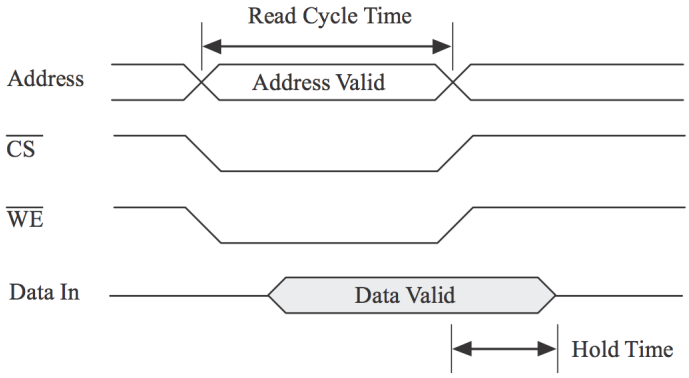


Figure 3: Timing diagram for the RAM write operation

S_2	S_1	S_0	$\overline{OE}$	$\overline{WE}$	$Load$	$\overline{Read}$	$Incr$
0	0	0	1	1	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	1	1	1	0
0	1	1	1	1	0	X	1
1	0	0	X	0	0	0	0
1	0	1	X	0	0	0	0
1	1	0	-	-	-	-	-
1	1	1	-	-	-	-	-

Table 1: State output

3 RAM controller design process

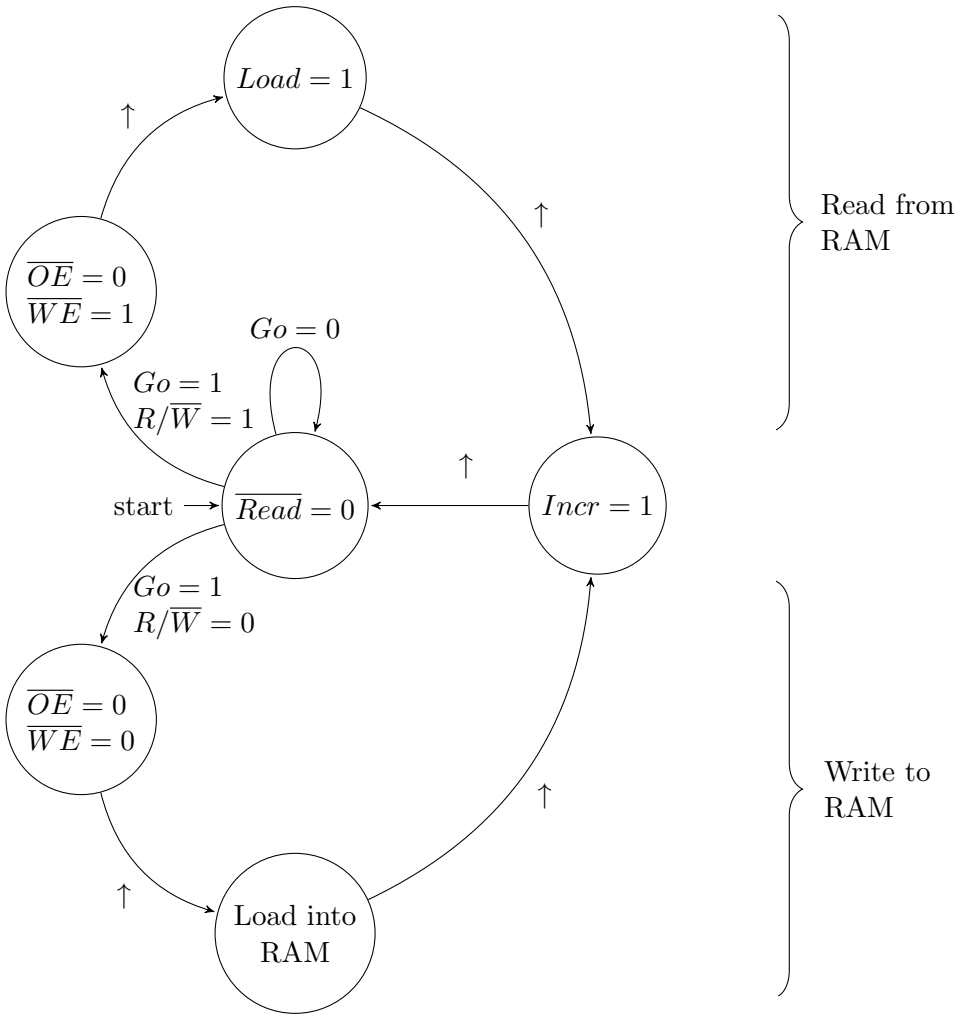
3.1 State diagram

State diagram of the controller

3.2 Controller logic

The logic design of the controller using D-FF

$$S_2^+ = S_2S_0' + S_1'S_0' \; Go \; R/\overline{W}$$
$$S_1^+ = S_1 \text{ XOR } S_0$$
$$S_0^+ = S_2 + S_1S_0' + S_0' \; Go \; R/\overline{W}$$


$Load = 1$
$\overline{OE} = 0$
$\overline{WE} = 1$
$Go = 0$
$Go = 1$
$R/\overline{W} = 1$
start
$\overline{Read} = 0$
$Incr = 1$
$Go = 1$
$R/\overline{W} = 0$
$\overline{OE} = 0$
$\overline{WE} = 0$
Load into RAM
Read from RAM
Write to RAM

State	S_2	S_1	S_0
a	0	0	0
b	0	0	1
c	0	1	0
d	0	1	1
e	1	0	0
f	1	0	1
-	1	1	0
-	1	1	1

(a) State enumeration

S_2	S_1	S_0	Go	$R/\overline{W}$	S_2^+	S_1^+	S_0^+
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0
0	0	1	0	1	0	1	0
0	0	1	1	0	0	1	0
0	0	1	1	1	0	1	0
0	1	0	0	0	0	1	1
0	1	0	0	1	0	1	1
0	1	0	1	0	0	1	1
0	1	0	1	1	0	1	1
0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
1	0	0	0	0	1	0	1
1	0	0	0	1	1	0	1
1	0	0	1	0	1	0	1
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1
1	0	1	1	0	0	1	1
1	0	1	1	1	0	1	1
1	1	0	0	0	-	-	-
1	1	0	0	1	-	-	-
1	1	0	1	0	-	-	-
1	1	0	1	1	-	-	-
1	1	1	0	0	-	-	-
1	1	1	0	1	-	-	-
1	1	1	1	0	-	-	-
1	1	1	1	1	-	-	-

(b) Next state

Figure 4: Transition tables for the Moore machine

$$\overline{OE} = S_1' S_0' + S_1 S_0$$
$$\overline{WE} = S_2'$$
$$Load = S_1 S_0'$$
$$\overline{Read} = S_1 + S_2' S_0$$
$$Incr = S_1 S_0$$

4 Conclusion