University of Victoria

CENG 241

Digital Design I

Lab 5 - Sequential Circuits: Flip-Flops and Counters

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A01 - B03

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1 Introduction

Sequential logic depends on present and past signals to determine the system's next state, hence sequential circuits have memory. The SR latches, D flip flops, T flip flops, and counters are examples of sequential circuits; they will be explored in this lab.

2 555 Timer

The required duty cycle of 50% and frequency of a few hertz were obtained using resistors $R_a = 330\,\Omega$, $R_b = 1\,\text{M}\Omega$ and a capacitor $C = 0.1\,\mu\text{F}$. From the following formulas,

$$\text{Clock frequency} = \frac{1.44}{(R_a + 2R_b)\,C} \qquad \text{Duty cycle} = \frac{R_a + R_b}{R_a + 2R_b}$$

the expected clock frequency and duty cycle were calculated to be 7.2 Hz and 50% respectively. Figure 1 shows the experimental frequency of 8.2 Hz with a duty cycle of 54.08%. Resistance and capacitance in the leads may account for these discrepancies.

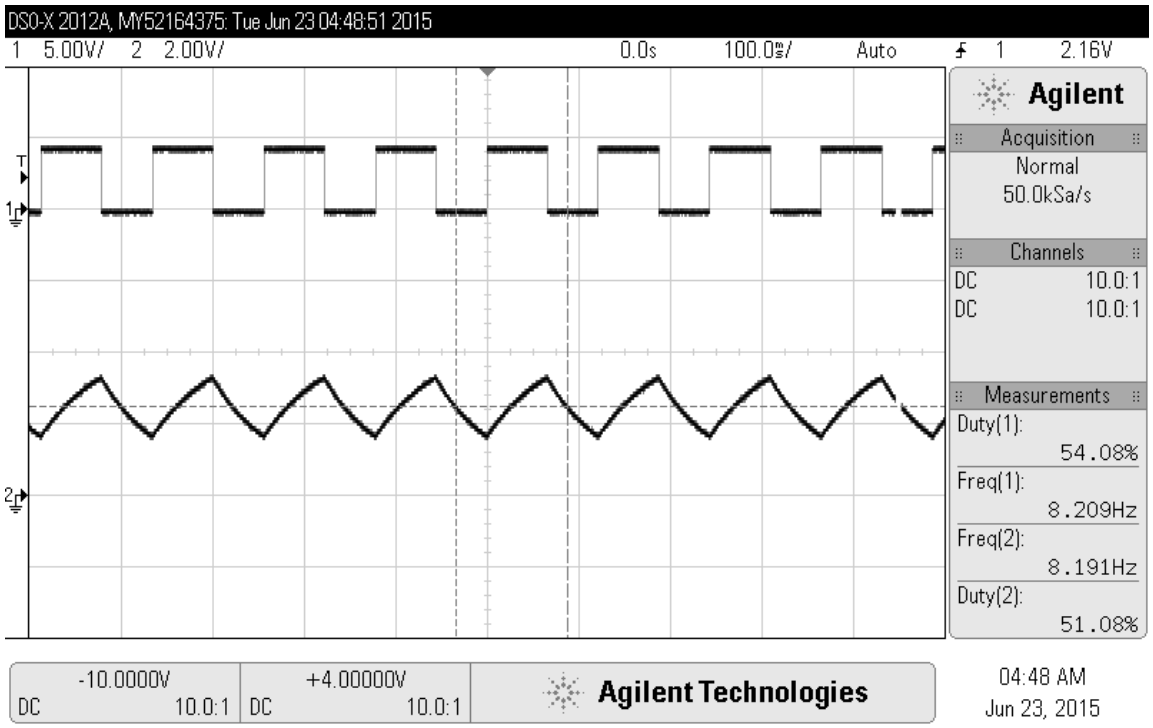

Figure 1: Output of the timer pin (top) and capacitor pin (bottom) for a 555 timer

3 RS Latch

Figure 2 shows an undebounced oscillation resulting from the response of switching RS = 00 to RS = 11. A period of 130 ns is obtained from measuring the peak to peak distance from the graph in this figure. Two 74C04 inverters were added to the RS latch circuit to extend the propagation delay enough to capture its effects. The 74C04 inverters advertise a typical 50 ns delay with a maximum value of 90 ns. Each 74LS00 NAND gates advertise a minimum 3 ns to a maximum 15 ns propagation delay. The total manufactured propagation delay for this circuit would be a minimum of 106 ns to a maximum of 210 ns, which confirms our result of 130 ns.

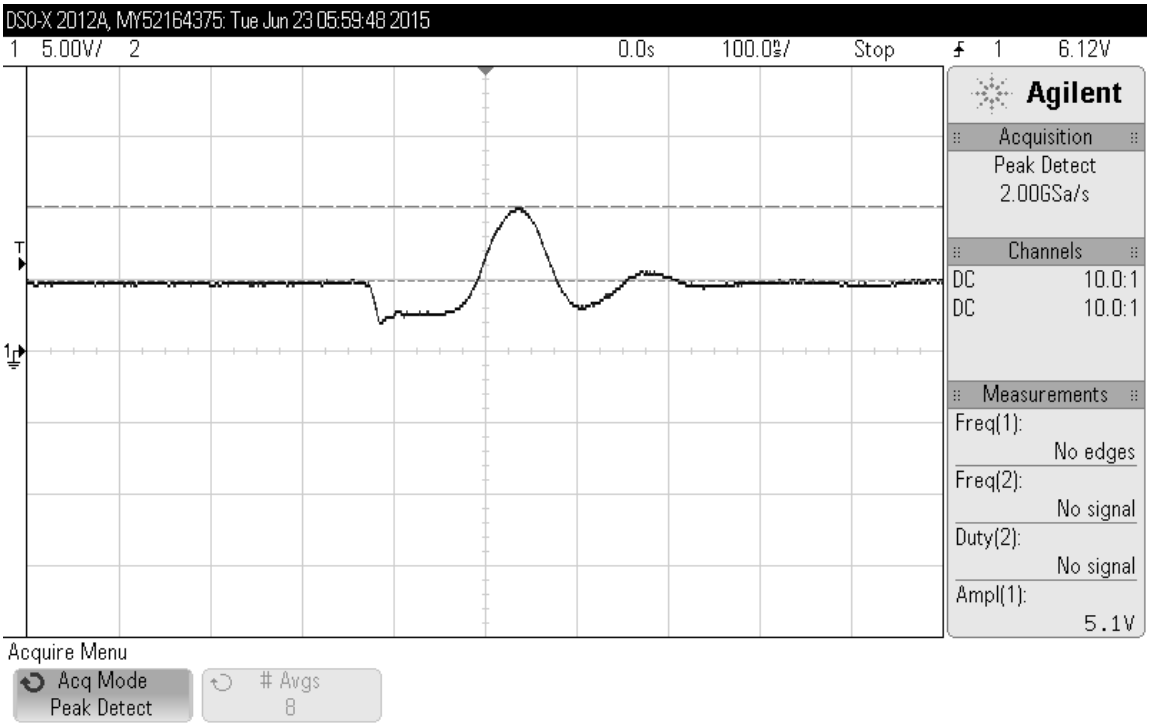

Figure 2: Oscillatory output of an RS latch in the indeterminate state

4 D Flip-Flop

Figure 3 shows the negative edge triggered D flip-flop. The D flip-flop has two inputs: a clock signal, and an input signal. The output reflects the input only during the brief moment of the falling edge of the clock and keeps that state until the next falling edge where it reevaluates its state from the input.

5 T Flip-Flop

A T flip-flop is similar to the D flip-flop except this flip-flop's input is the T signal XOR with its output Q_t to give the next state Q_{t+1}. Unlike the D flip-flop, the T flip-flop is triggered on the rising edge of the clock. With $T = 1$, the flip-flop will change its value at every rising edge. This behavior is shown in the bottom trace in Figure 4.

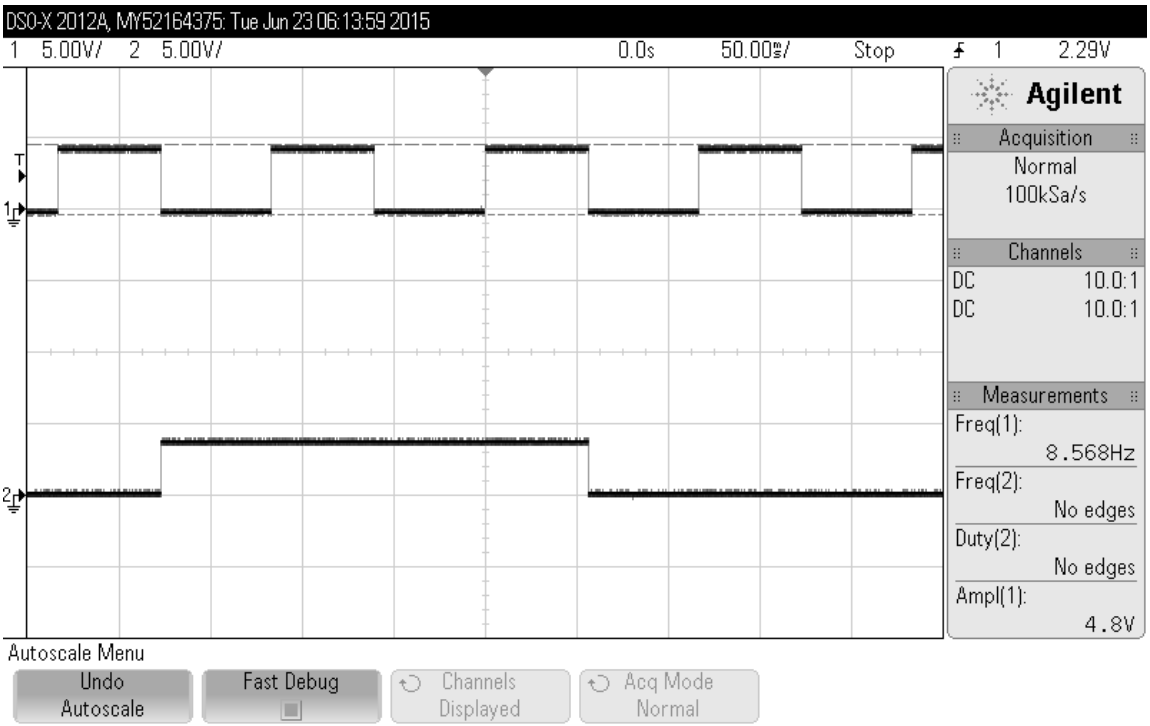

Figure 3: The D flip-flop only updates its value on the falling edge

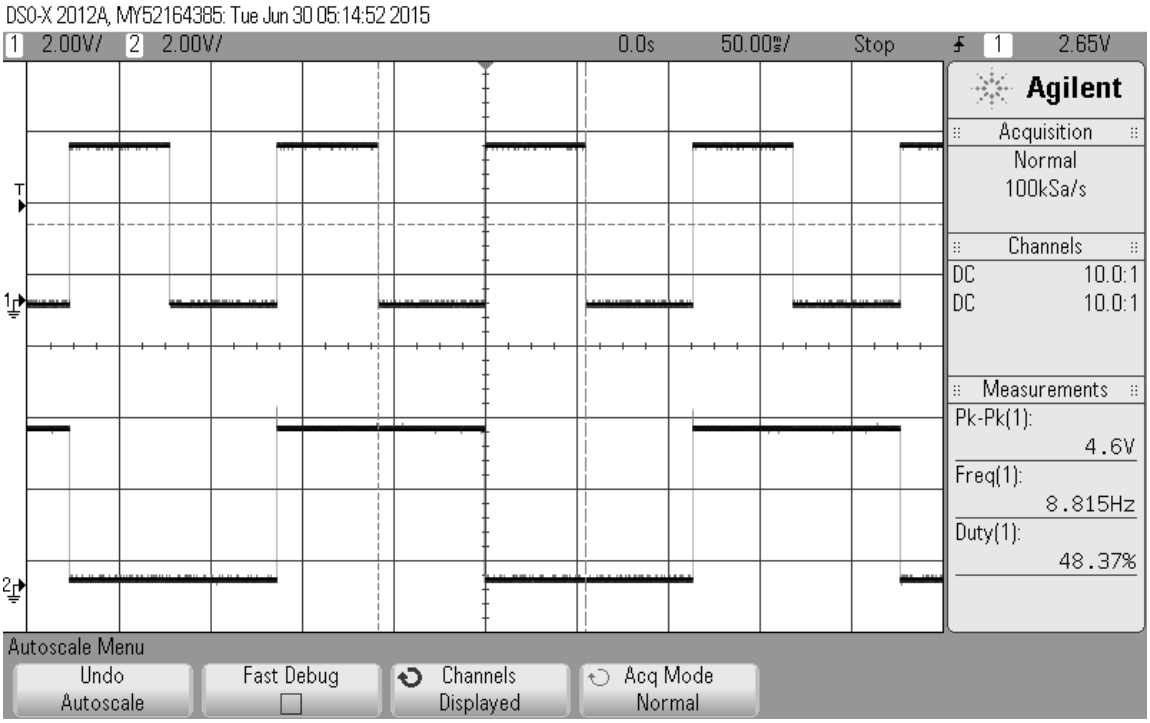

Figure 4: Output of a T flip-flop for $T = 1$

6 Counter

Figure 5 is a schematic of the counter circuit built to count from 3 to 12. The input signal P is preset to 3 (0011): P_0 and P_1 are connected to V_{cc} (high), while P_2 and P_3 are connected to ground (low). $\overline{Pe}$, the enable, is activated on a low signal. The first time this happens is when the counter reaches 12 (1100). At this point, the input to $\overline{Pe}$ is low and the values from P_i are loaded. The default values disable $\overline{Pe}$ on the next clock cycle and the count resumes.

The circuit initially displayed 0 for the first few clock cycles. This occurs because it takes a non-zero amount of clock cycles to fully load the sequential circuits internal to the 74LS163. Once the circuits are loaded, each clock cycle will allow the inputs (Q_t or P_i) to propagate directly to the output Q_{t+1}.

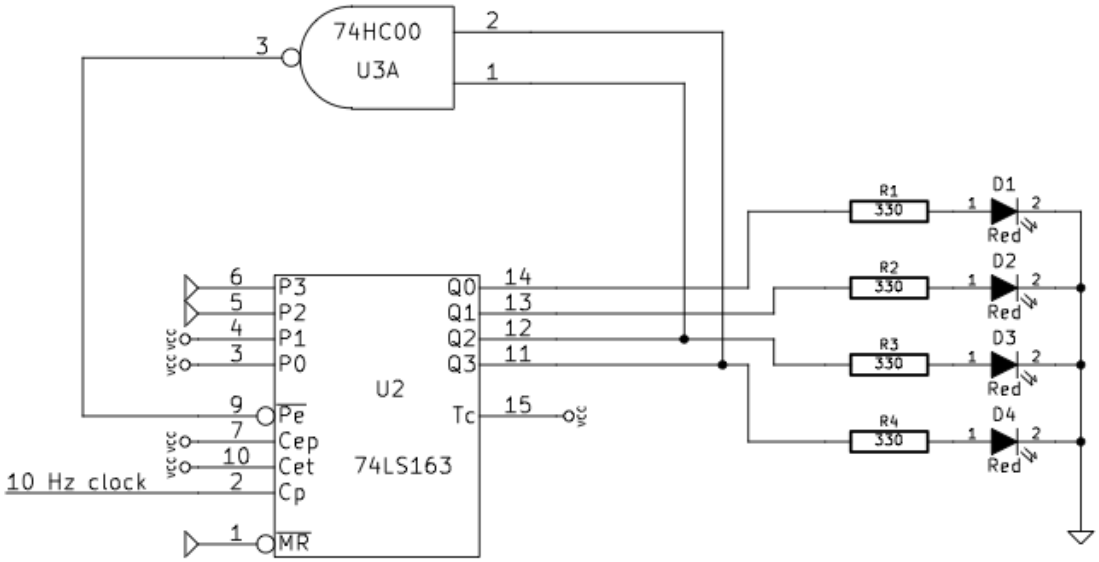

Figure 5: 74LS163 used to count 3 to 12 before resetting

7 Conclusion

Sequential logic was explored in this lab. A common relationship between these circuits is that they require the present output to determine its next state; in a sense, these circuits have memory.