University of Victoria

CENG 241

Digital Design I

Lab 2 - Using Xilinx ISE Tutorial

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1 Introduction

The second lab serves as a learning environment for the Xilinx ISE (integrated software environment). This software enables simulation of digital circuits which can facilitate the design and troubleshooting of such circuits. Two digital design entry methods were explored: the schematic method, and the Verilog HDL (hardware description language).

2 Results

The following figures are snapshots obtained during this lab. A half adder is illustrated by the schematic in Figure 1. The functional simulation in Figure 2 shows the expected output from the circuit based on user-defined input. Outputs S and C are shown for all combinations of binary inputs X and Y.

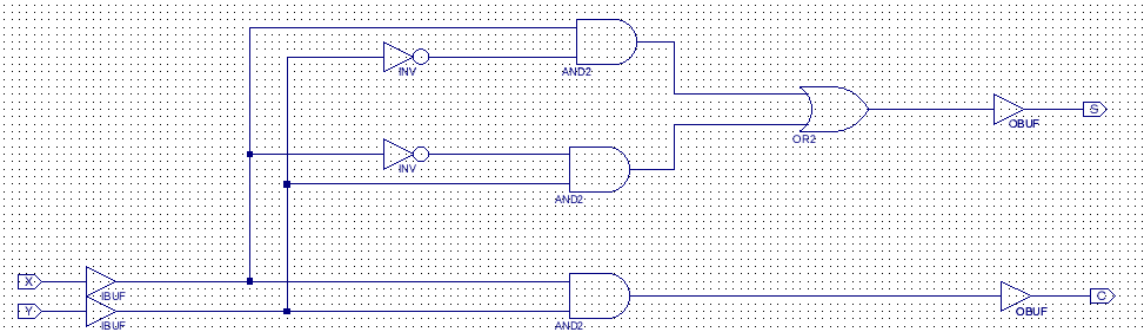

Figure 1: Complete schematic of a half adder

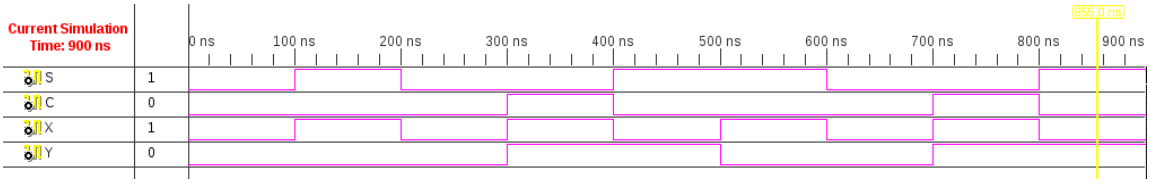

Figure 2: Functional simulation of a half adder

The Verilog HDL code for a half adder is shown in the code block below, while the post place-and-route timing simulator is shown if Figure 3. An FPGA is programmed according to the verilog module, which is used to determine the runtime delay of the half adder. Figure 3 indicates that both outputs will arrive 8.9 ns after the inputs.

```
module ha(X, Y, S, C);
  input X;
  input Y;
  output S;
  output C;

assign S = (X & (!Y)) | ((!X) & Y); // S = X XOR Y
assign C = X & Y;                   // C = X AND Y

endmodule
```

Verilog implementation of a half adder

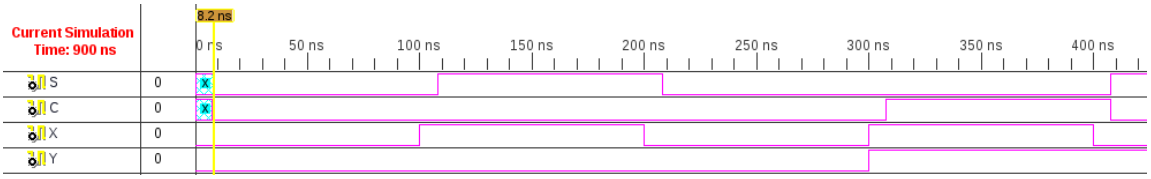

Figure 3: Post place and route timing indicates a delay of 8.9 ns in the half adder

3 Discussion

The digital design entry methods explored were the schematic and Verilog HDL. The Verilog HDL seemed to be more efficient testing logic assuming a proper boolean function was available. This method produces quick results for any size circuit, but could be prone to error due to not being able to visualize the circuit. The schematic method is tedious for anything but few component circuits, but enables visualization which may help troubleshooting.

A functional simulation tests the logic of a circuit with no consideration on circuit timing and delays. Timing simulations, meanwhile, test the functionality of circuits with any routing and logic delay considered to give proper results. Functional simulations can only ensure that the logic of the circuit is correct but give no insight about delays arising from timing problems.

4 Conclusion

The two digital design methods explored in this lab offer their individual strengths with their weaknesses. The schematic design is more user friendly, but tedious, while the Verilog HDL is quick and efficient, but could be prone to error.