# University of Victoria

# **CENG 241**

DIGITAL DESIGN I

# Lab 6 Finite state machines: Mealy and Moore circuits

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# 1 Introduction

# 2 Discussion

A brief description about what the circuit will do.

Difference between Moore and Mealy?

Method for generating circuits? State machine  $\rightarrow$  Truth table  $\rightarrow$  Kmap  $\rightarrow$  Boolean  $\rightarrow$  circuits

Input 1001101101001101 Output 0000001001000001

#### 2.1 State diagrams

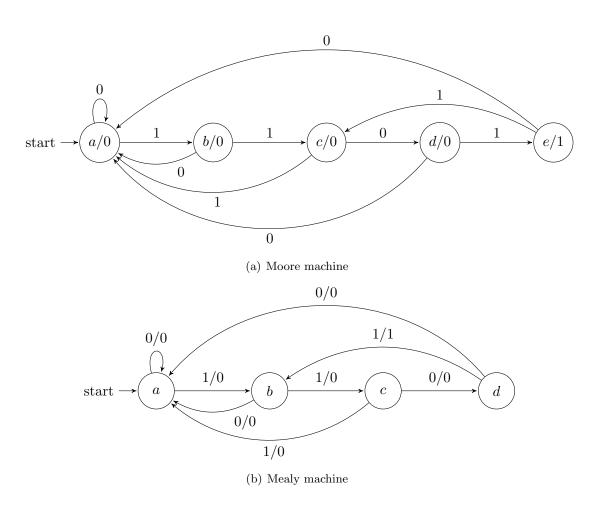


Figure 1: State machines to detect sequence "1101" with overlap

				$S_2$	$S_1$	$S_0$	X	$S_2^+$	$S_1^+$	$S_0^+$					
				0	0	0	0	0	0	0					
				0	0	0	1	0	0	1					
				0	0	1	0	0	0	0					
State	$S_2$	$S_1$	$S_0$	0	0	1	1	0	1	0	$S_2$	$S_1$	$S_0$	Z	
$\overline{a}$	0	0	0	0	1	0	0	0	1	1	0	0	0	0	
b	0	0	1	0	1	0	1	0	0	0	0	0	1	0	
c	0	1	0	0	1	1	0	0	0	0	0	1	0	0	
d	0	1	1	0	1	1	1	1	0	0	0	1	1	0	
e	1	0	0	1	0	0	0	0	0	0	1	0	0	1	
-	1	0	1	1	0	0	1	0	1	0	1	0	1	-	
-	1	1	0	1	0	1	0	-	-	-	1	1	0	-	
-	1	1	1	1	0	1	1	-	-	-	1	1	1	-	
(a) State enumeration				1	1	0	0	-	-	-	(c) Output				
				1	1	0	1	_	-	-					
				1	1	1	0	_	-	-					
				1	1	1	1	_	-	-					
(b) Next state															

Figure 2: Transition tables for the Moore machine

			$S_1$	$S_0$	X	$S_1^+$	$S_0^+$		$S_1$	$S_0$	X	Z
			0	0	0	0	0		0	0	0	0
State	$S_0$	$S_1$	0	0	1	0	1		0	0	1	0
$\overline{a}$	0	0	0	1	0	0	0		0	1	0	0
b	0	1	0	1	1	1	0		0	1	1	0
c	1	0	1	0	0	1	1		1	0	0	0
d	1	1	1	0	1	0	0		1	0	1	0
(a) State enumeration			1	1	0	0	0		1	1	0	0
			1	1	1	0	1		1	1	1	1
		(b) Next state					(c) Output					

Figure 3: Transition tables for the Mealy machine

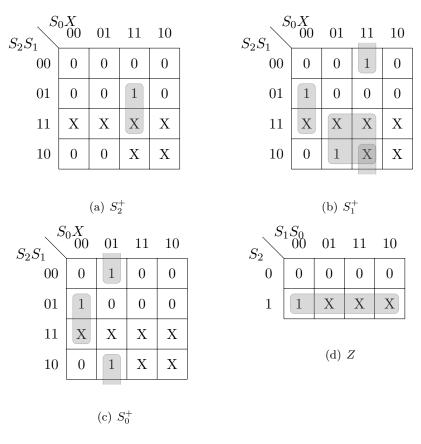


Figure 4: Karnaugh maps for the Moore machine

#### 2.2 Transition tables

#### 2.3 Karnaugh maps

The optimal boolean functions for the Moore machine are

$$S_{2}^{+} = S_{1}S_{0}X$$

$$S_{1}^{+} = S_{1}S'_{0}X' + S'_{1}S_{0}X + S_{2}X$$

$$S_{0}^{+} = S_{1}S'_{0}X' + S'_{1}S'_{0}X$$

$$Z = S_{2}$$

The optimal boolean functions for the Mealy machine are

$$S_1^+ = S_1 S_0' X' + S_1' S_0 X$$
  

$$S_0^+ = S_1 S_0' X' + S_1' S_0' X + S_1 S_0 X$$
  

$$Z = S_1 S_0 X$$

# 3 Xilinx simulation

Include schematic for Mealy machine and functional output

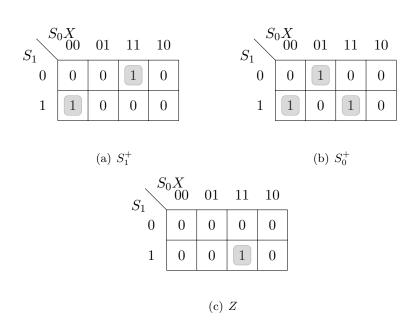


Figure 5: Karnaugh maps for the Mealy machine

# 4 Conclusion