University of Victoria

CENG 241

Digital Design I

Lab 5 - Sequential Circuits: Flip-Flops and Counters

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A01 - B03

June 29, 2015

1 Introduction

2 555 Timer

- Values for Ra, Rb, C
- Expected values for duty cycle and frequency based on formula
- screenshot of two clock cycles

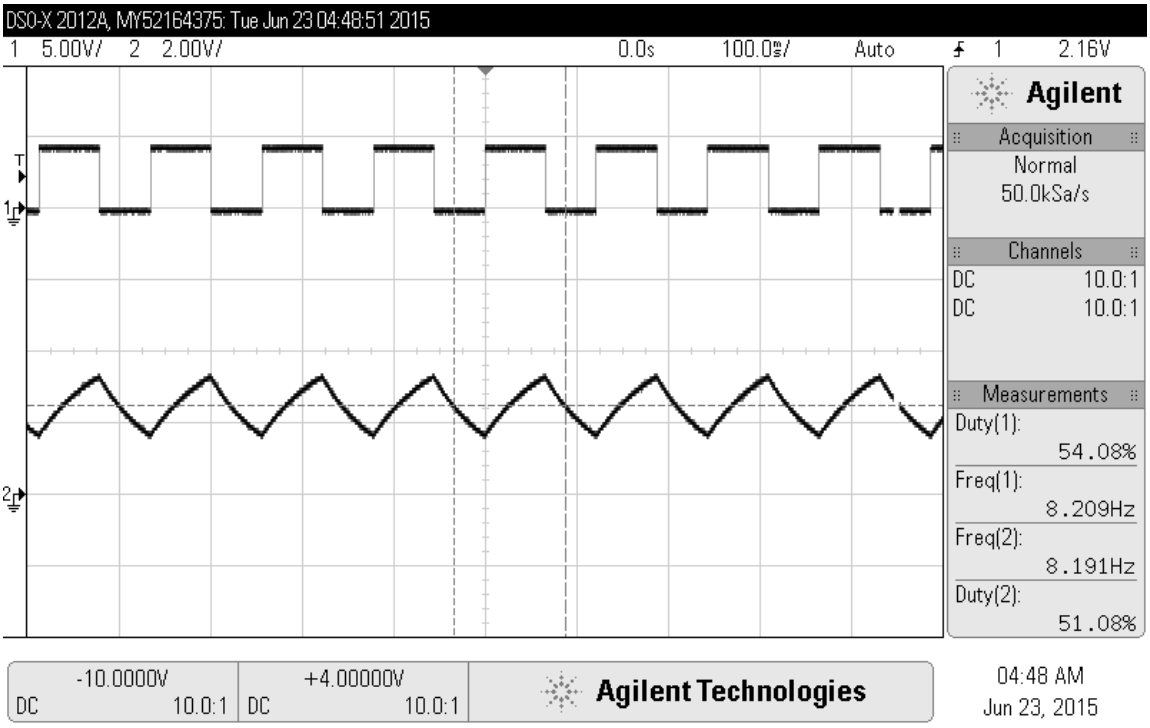

Figure 1: Output of the timer pin (top) and capacitor pin (bottom) for a 555 timer

3 RS Latch

- schematic of latch with two inverters on output
- screenshot of oscillations at 00/11
- how does frequency of oscilations relate to delay in circuit?

4 D Flip-Flop

- screenshot of D-FF changing on negative edge
- description of how D-FF works

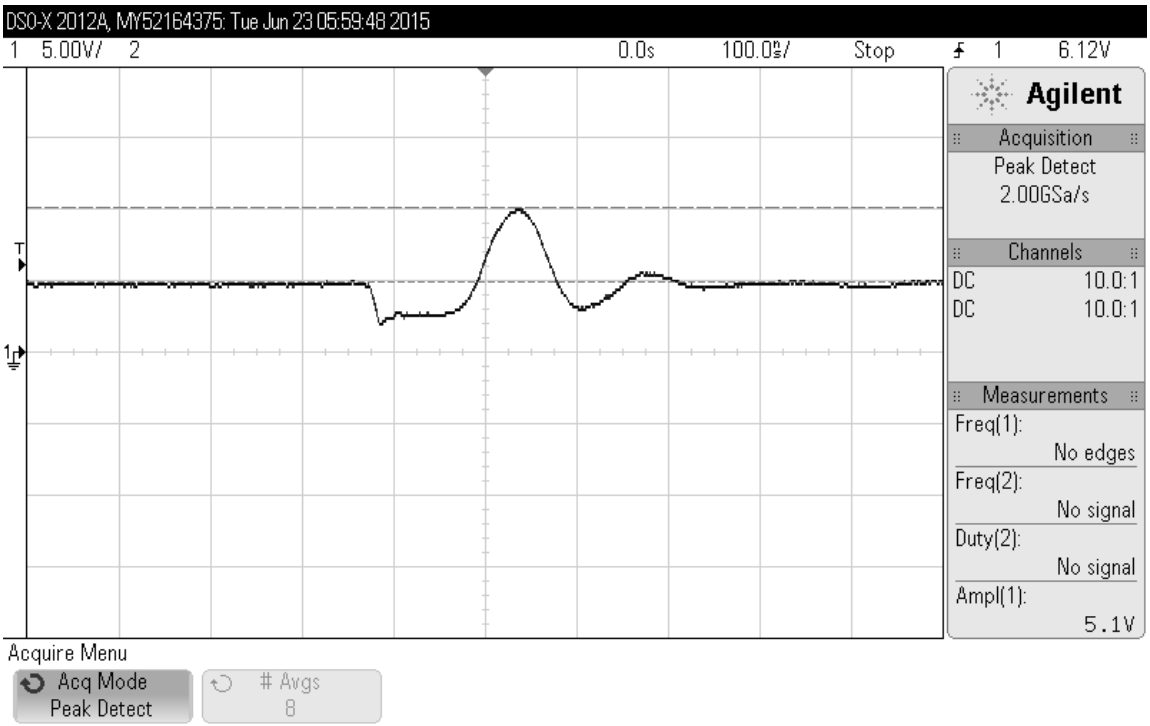

Figure 2: Oscillatory output of an RS latch in the indeterminate state

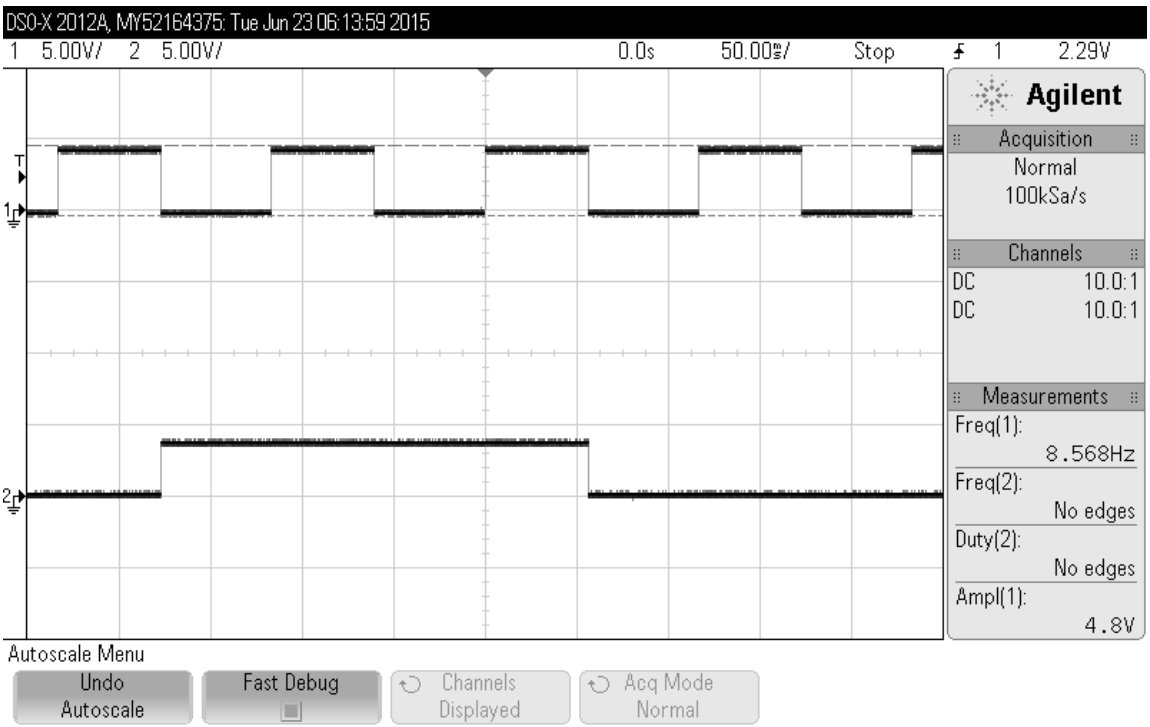

Figure 3: The D flip-flop only updates its value on the falling edge

5 T Flip-Flop

- screenshot for T=1

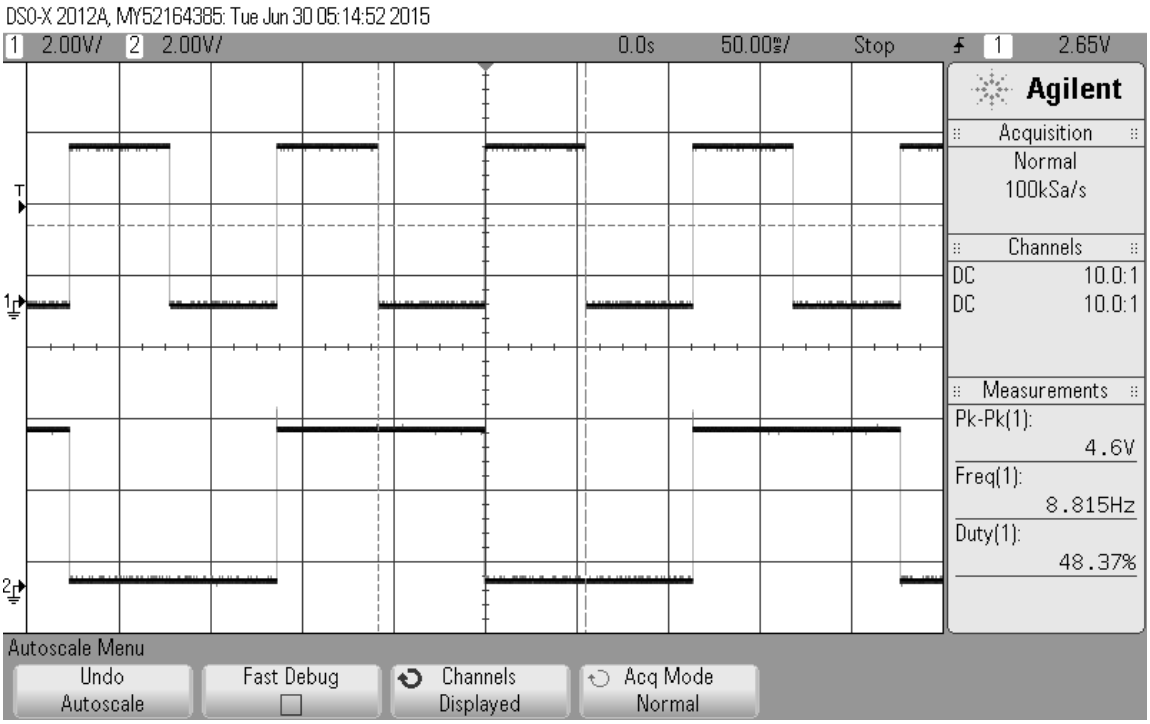

Figure 4: Output of a T flip-flop for $T = 1$

6 Counter

- schematic of circuit as built in lab
- Explain why the output of the circuit is not in the range of 3 to 12 in the first few clock cycles.

7 Conclusion

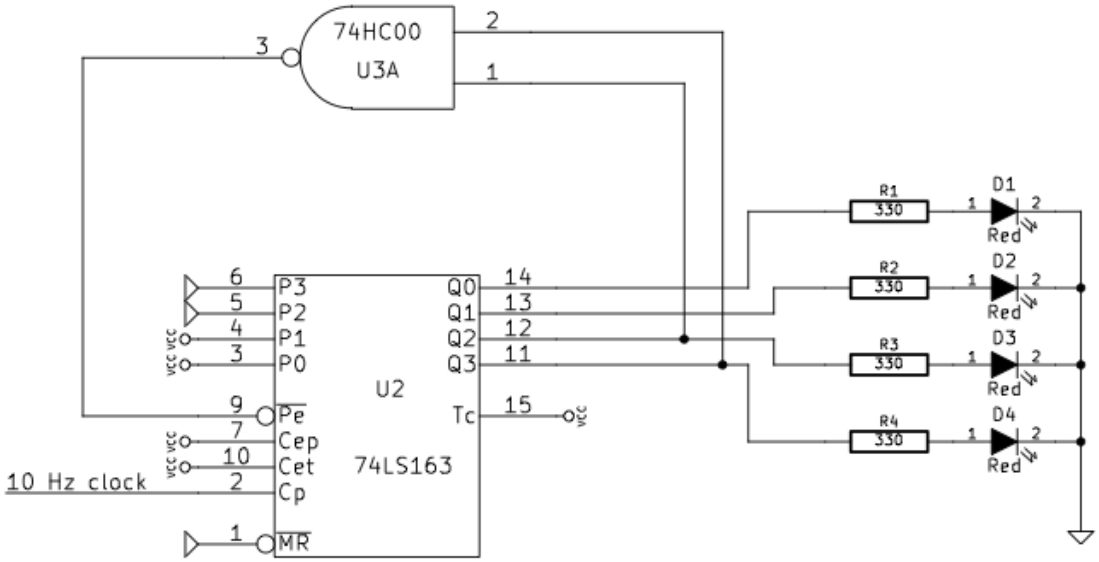

Figure 5: 74LS163 used to count 3 to 12 before resetting