University of Victoria

CENG 241

Digital Design I

Lab 2 - Using Xilinx ISE Tutorial

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1 Introduction

2 Discussion

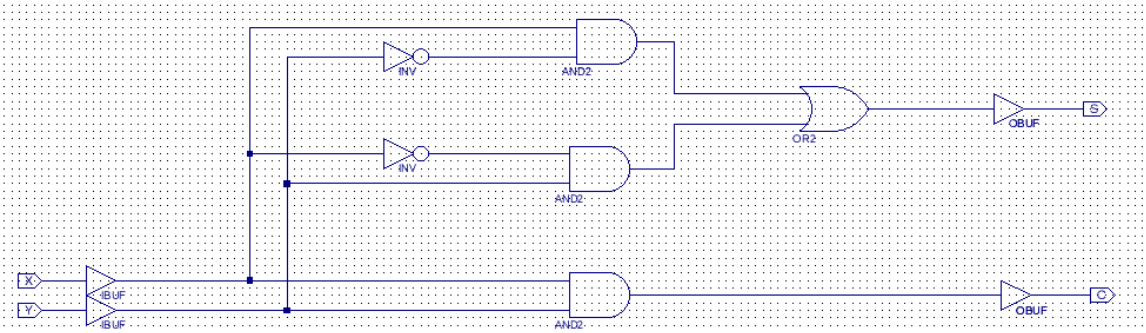

Figure 1: Complete schematic of a half adder

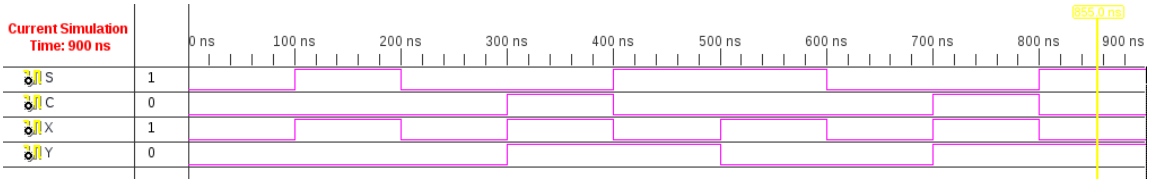

Figure 2: Functional simulation of a half adder

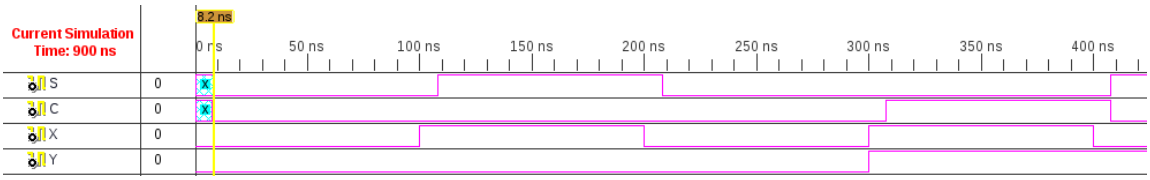

Figure 3: Post place and route timing indicates a delay of 8.9 ns in the half adder

```
module ha(X, Y, S, C);
  input X;
  input Y;
  output S;
  output C;

assign S = (X & (!Y)) | ((!X) & Y); // S = X XOR Y
assign C = X & Y;                   // C = X AND Y

endmodule
```

Verilog implementation of a half adder

What are the digital design entry methods? Form your opinion, which one is the most efficient? Why?

What is the difference between a functional simulation and a timing simulation? Is a functional simulation sufficient enough to ensure the correctness of the design?

3 Conclusion