University of Victoria

CENG 241

Digital Design I

Lab 1 - Digital Instrumentation, Basic Digital Components and Circuits

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A01 - B03

June 1, 2015

1 Introduction

2 Voltage Regulators

V_{in} (V)	V_{out} (V)	I_{in} (mA)	I_{out} (mA)	P (mW)	T (°C)
0.0	2×10^{-5}	2×10^{-4}	2×10^{-4}		22.9
1.0	1.5×10^{-5}	2×10^{-4}	2×10^{-4}		22.9
2.0	4.3×10^{-4}	6×10^{-4}	6×10^{-4}		23.3
3.0	1.5913	1.599	1.599		23.0
4.0	2.5057	2.5143	2.5143		23.2
5.0	3.662	3.6758	3.6758		23.4
6.0	4.689	4.7083	4.7083		23.8
7.0	4.992	5.0129	5.0129		24.1
8.0	4.904	4.9252	4.9252		24.8
9.0	4.845	4.8655	4.8655		25.7
10.0	4.815	5.053	5.053		25.8
11.0	4.777	5.050	5.050		26.3
12.0	4.759	5.0217	5.0127		27.2

Table 1: Voltage, current and temperature response of LM7805 5V regulator

The range of voltages where the regulator voltage output is constant

What happens when the regulator is short circuited?

3 Signal damping

waveforms of under, over, critically damped waves

rise and fall time of critically damped wave

4 LEDs and Inverters

When is the LED lit?

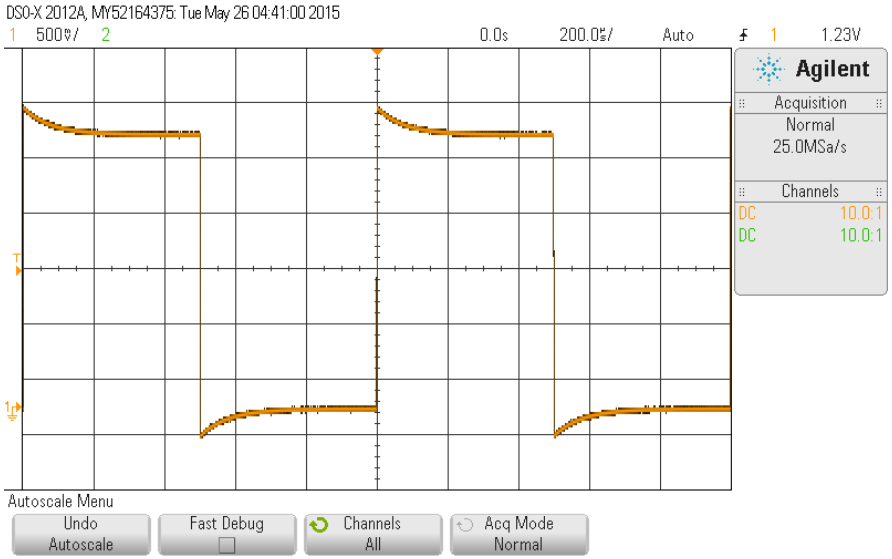
Why use a 7405, not a 7404? (ordinary inverter v. open collector inverter)

5 Push button debouncing

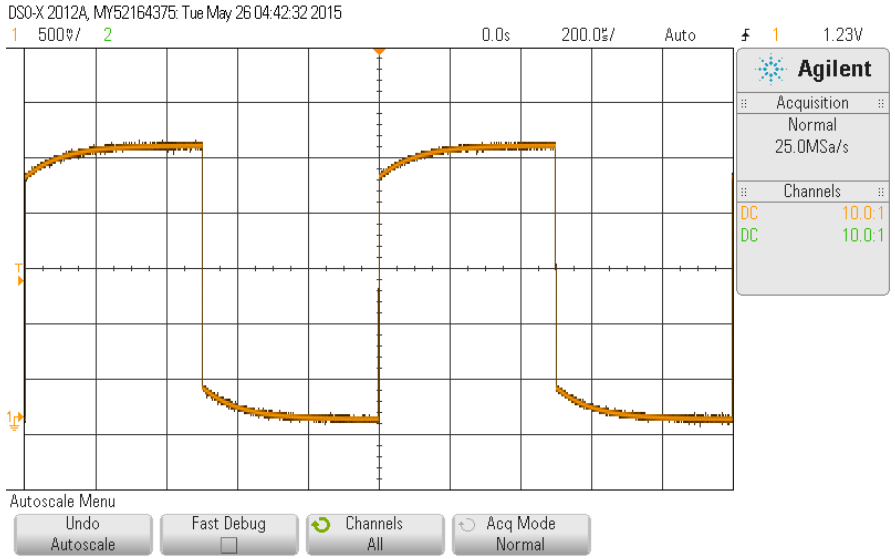
Display the debounced and non-debounced waveforms

Draw a debouncer with NOR gates

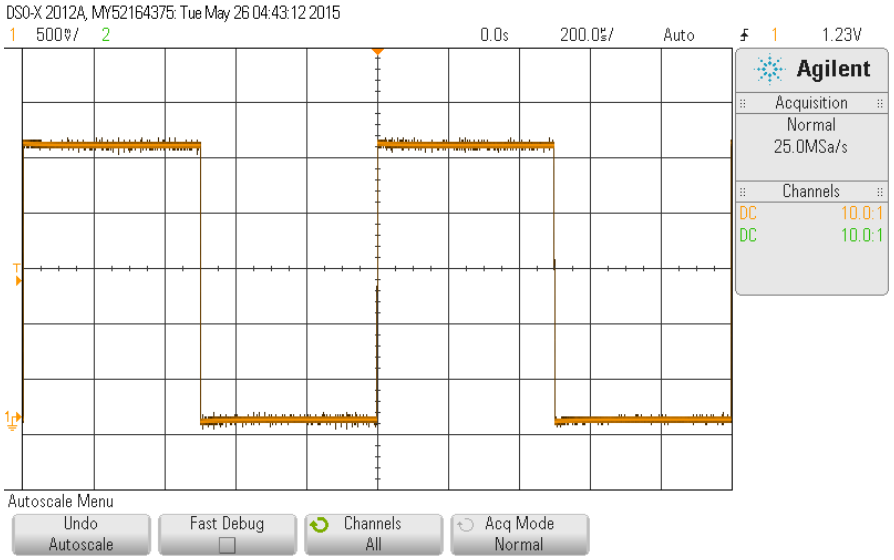
6 Conclusion



(a) Over damping

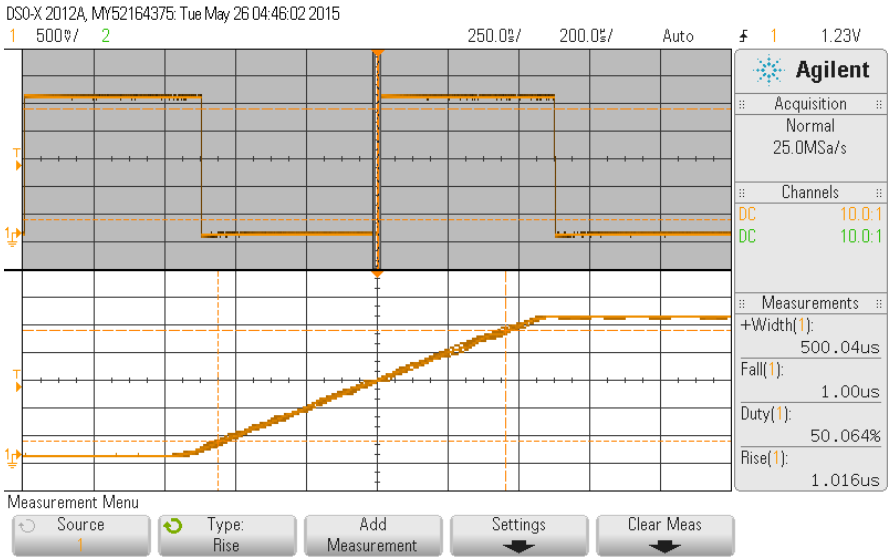


(b) Under damping

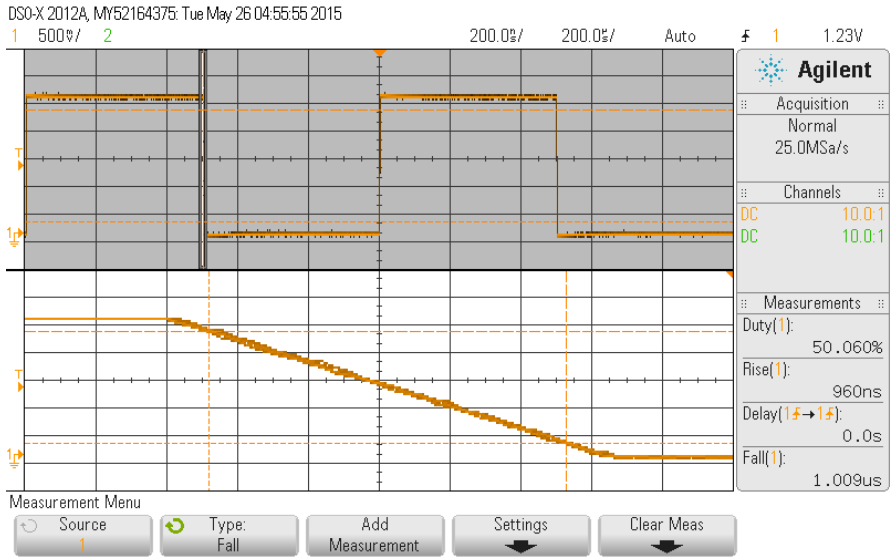


(c) Critical damping

Figure 1: Waveforms representative of different levels of damping for a square wave



(a) Rise time



(b) Fall time

Figure 2: Opposite edges of a critically damped square wave

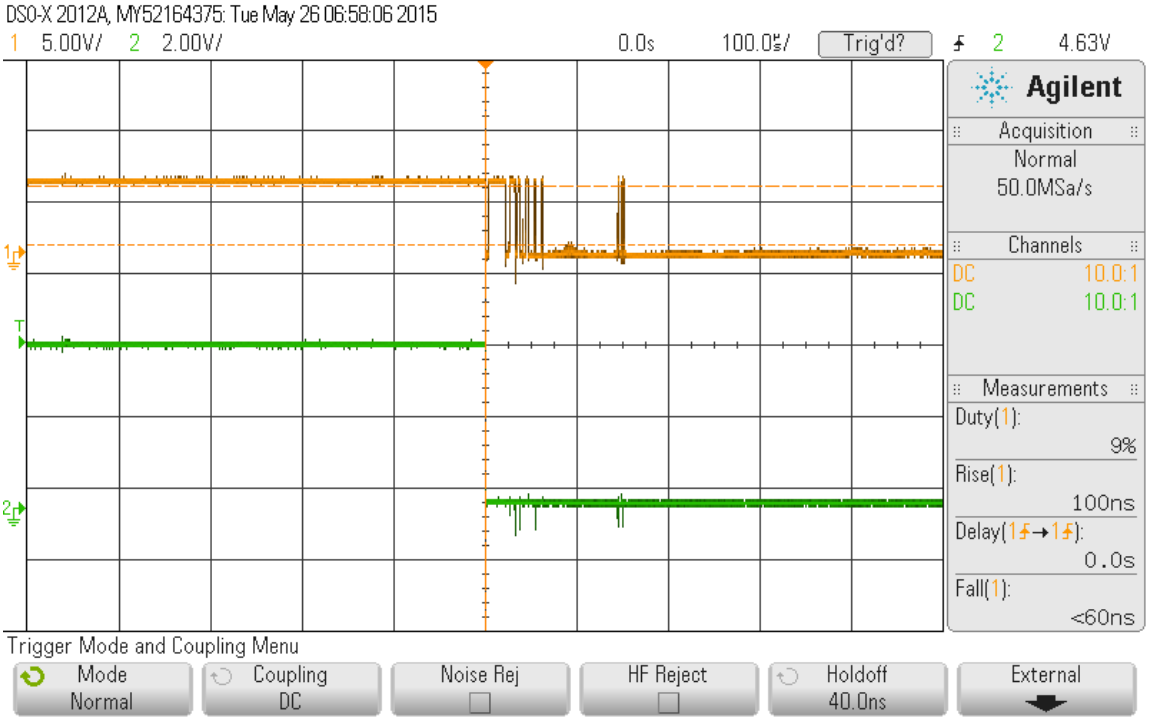


Figure 3: Waveforms of non-debounced (top) and debounced (bottom) SPDT presses

graphics/nor_gates.png

Figure 4: An SPDT debouncer constructed from NOR gates