University of Victoria

CENG 241

Digital Design I

Lab 1 - Digital Instrumentation, Basic Digital Components and Circuits

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A01 - B03

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1 Introduction

This lab serves as an introduction to basic digital components and circuits. The following is a list of items explored throughout this lab:

- voltage regulator
- power supply
- oscilloscope
- pulse generator
- digital multimeter
- SPDT switch
- push button debouncer
- and various electrical components.

2 Voltage Regulators

V_{in} (V)	V_{out} (V)	I_{in} (mA)	I_{out} (mA)	P (mW)	T (°C)
0.0	2×10^{-5}	2×10^{-4}	2×10^{-4}	N/A	22.9
1.0	1.5×10^{-5}	2×10^{-4}	2×10^{-4}	N/A	22.9
2.0	4.3×10^{-4}	6×10^{-4}	6×10^{-4}	N/A	23.3
3.0	1.5913	1.599	1.599	2.25	23.0
4.0	2.5057	2.5143	2.5143	3.76	23.2
5.0	3.662	3.6758	3.6758	4.92	23.4
6.0	4.689	4.7083	4.7083	6.17	23.8
7.0	4.992	5.0129	5.0129	10.1	24.1
8.0	4.904	4.9252	4.9252	15.2	24.8
9.0	4.845	4.8655	4.8655	20.2	25.7
10.0	4.815	5.053	5.053	26.2	25.8
11.0	4.777	5.050	5.050	31.4	26.3
12.0	4.759	5.0217	5.0217	36.4	27.2

Table 1: Voltage, current and temperature response of LM7805 5V regulator

The voltage regulator regulated the output voltage to $5V +/- .3V$ for input voltages between $6.0V$ and $12.0V$. As we can see in Table 1, when the power supply was set to below $3.0V$ only stray voltages and currents were present; the voltage regulator blocked insufficient voltages and currents. As the regulator worked to regulate the voltage its power consumption increased, which was evident by the heat dissipated.

Next, the output of the voltage regulator was shorted to ground. Initially, the power supply was set to $8V$ and $200mA$; however, the power supply limited the voltage and current to $2.7V$ and $130mA$ due to its short circuit protection. The regulator controlled the output to $64.47mV$ and $136mA$, while increasing its operating temperature from room temperature to 44.8 °C

3 Signal damping

Figure 1 displays examples of over-damped, under-damped, and critically damped waveforms. Properly tuned oscilloscope probes will display a critically damped waveform when tested, and they should be tested prior to every use.

Figure 2 illustrates the rise and fall time of critically tuned probes. The rise and fall times were both calculated to be $1\mu s +/- .04\mu s$.

4 LEDs and Inverters

The LED illuminated in the absence of the signal voltage, while it extinguished at the presence of it. Since the signal voltage was inverted, the LED was connected to the source voltage and the circuit was completed only at the absence of a signal.

******** I'm not sure about the following one Tyler. Does my reasoning make sense? **********

The 7405 inverter features open collector outputs, while the 7404 does not. The 7404 inverter connects internally the V_{cc} to the output by way of an internal transistor through a 130Ω resistor. Our circuit configuration would then place a parallel run with the LED and external 1kΩ resistor. Since the current will chose the path of least resistance, there would not be enough current to power the LED.

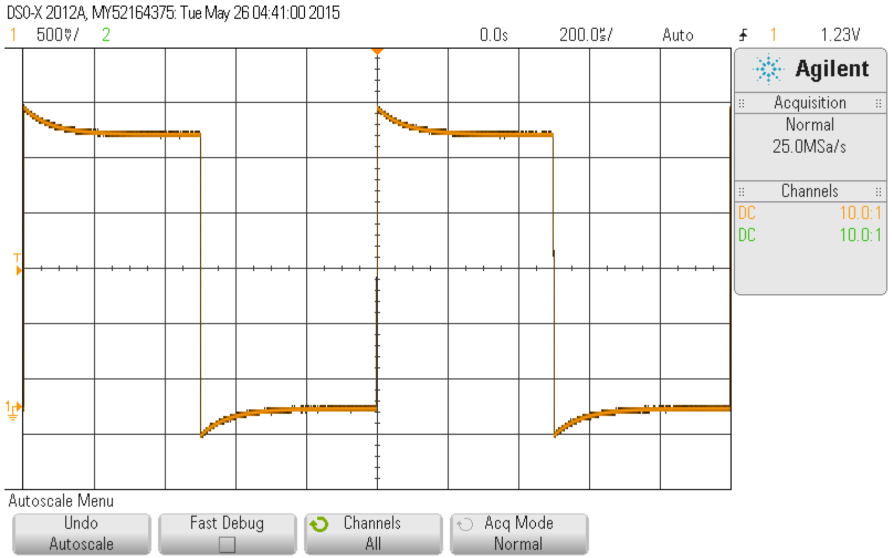
5 Push button debouncing

Figure 4 displays the debounced and non-debounced waveforms from activating the push button debouncer. The debounced signal appears cleaner than the non-debounced signal which would lead to more accurate circuit performance and results.

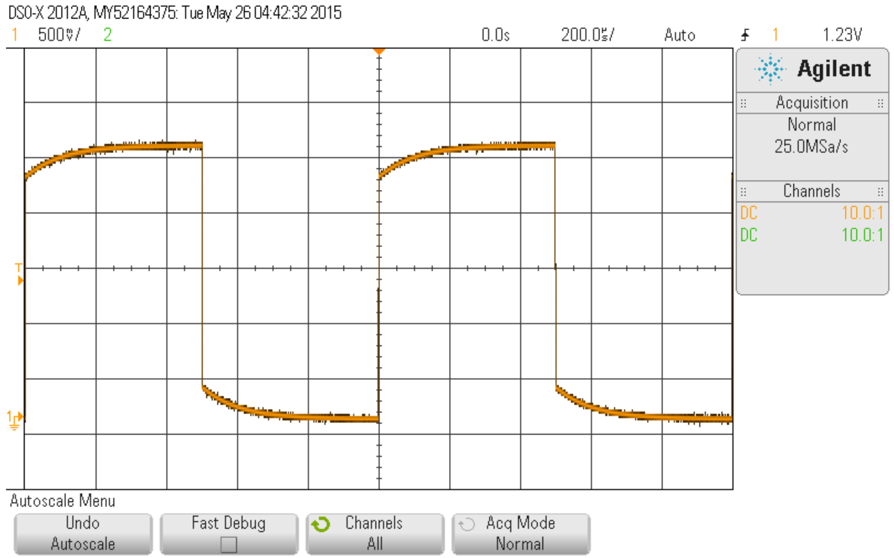
A debouncer can be implemented using NOR gates, figure 5 illustrates such a circuit.

6 Conclusion

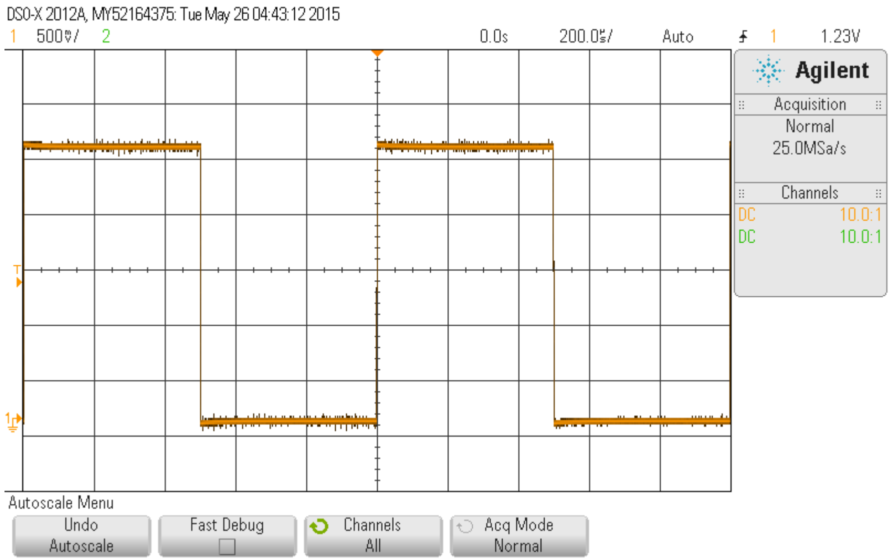
While being introductory, the circuits explored in this lab performed as expected. The voltage regulator dissipates heat fast under extreme circumstances, but its temperature only increases gradually when used under normal conditions. Also, circuits can be analyzed cleanly with properly tuned oscilloscope probes, an status circuit with LED, and a debouncer. These items help to expedite and facilitate troubleshooting.



(a) Over damping

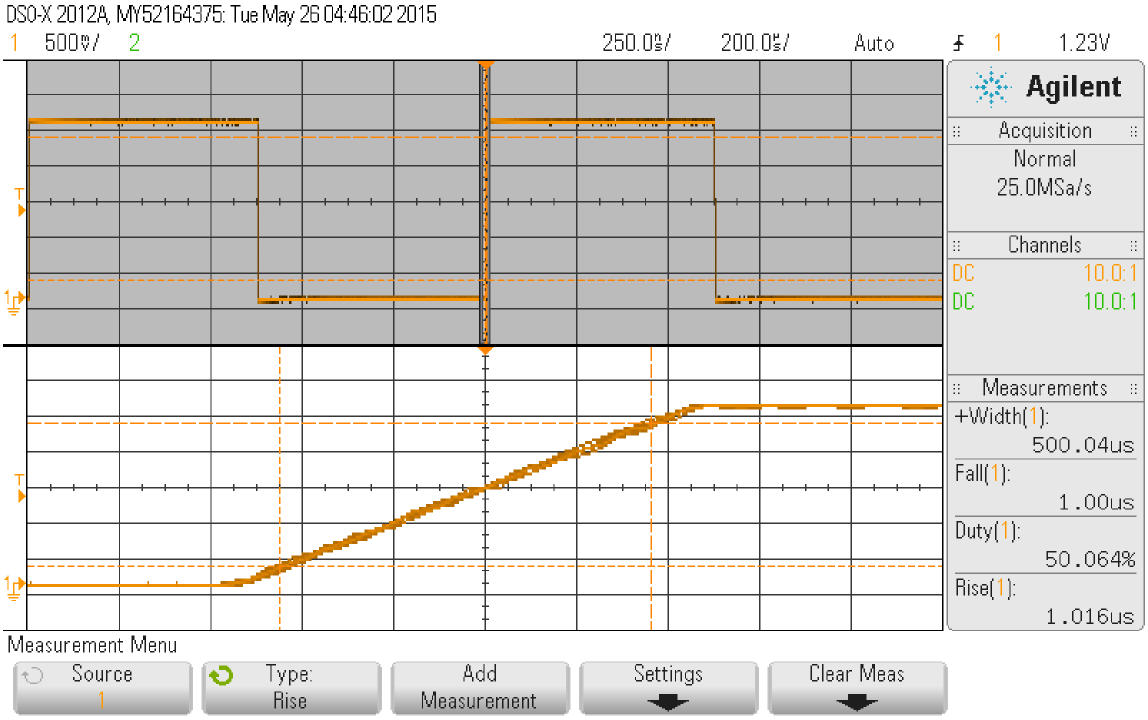


(b) Under damping

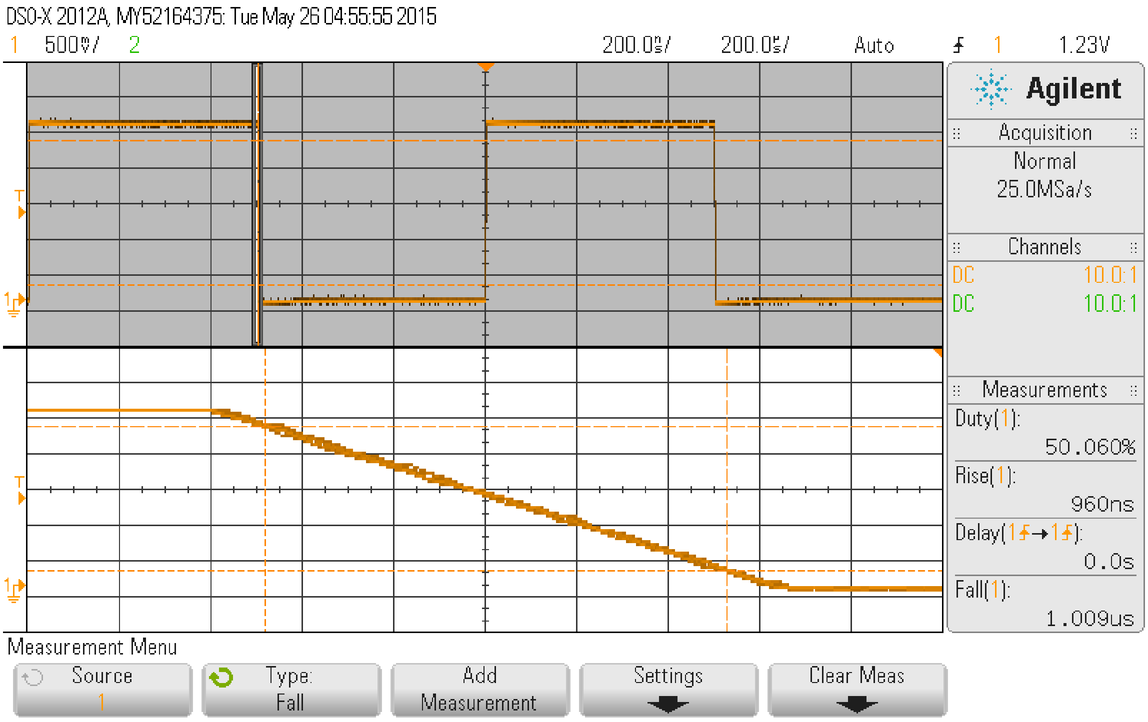


(c) Critical damping

Figure 1: Waveforms representative of different levels of damping for a square wave



(a) Rise time



(b) Fall time

Figure 2: Opposite edges of a critically damped square wave

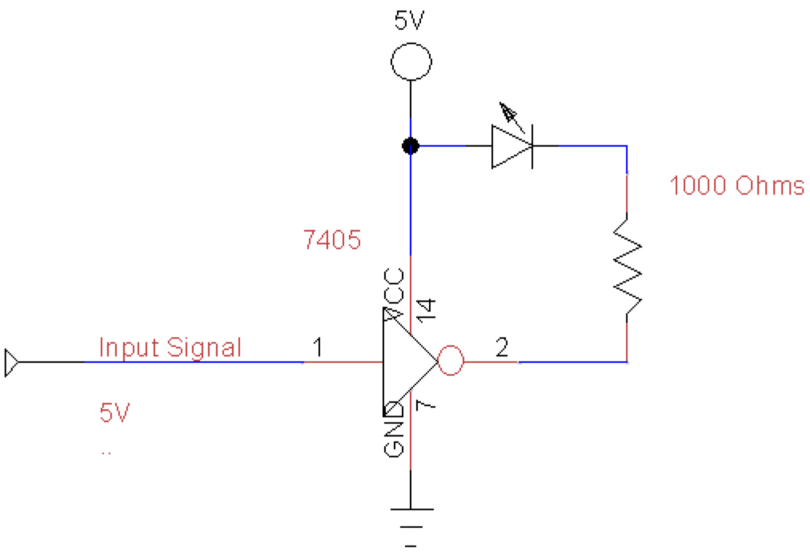


Figure 3: Controlling an LED with a LS7405 inverter.

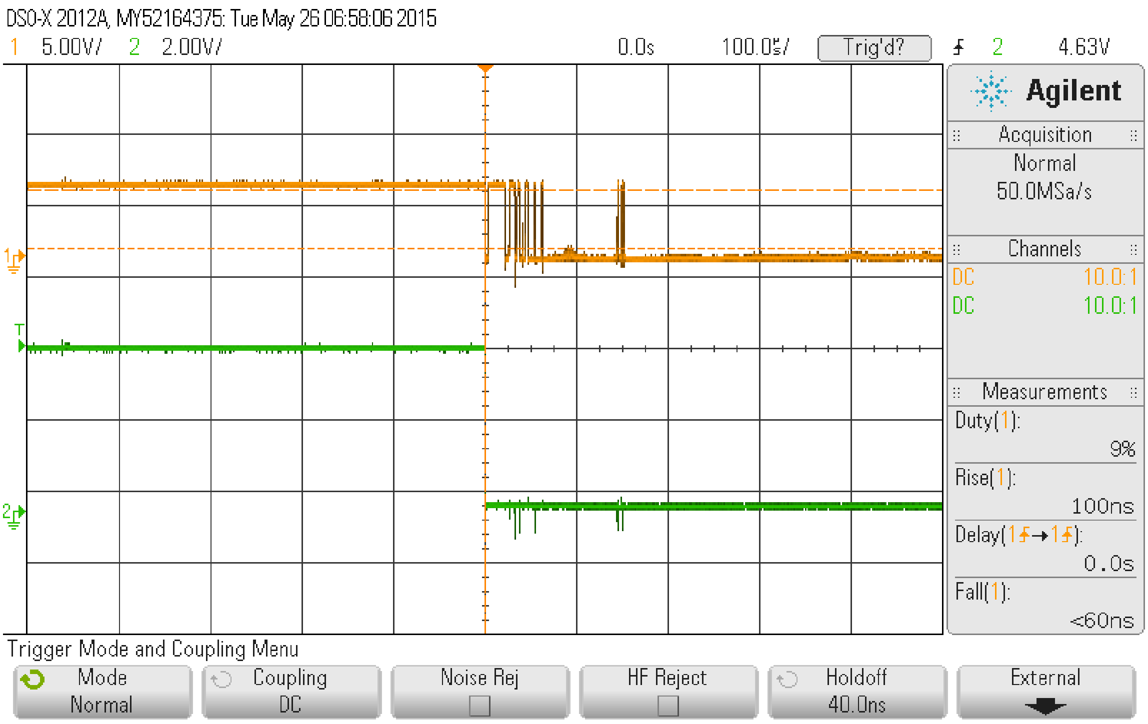


Figure 4: Waveforms of non-debounced (top) and debounced (bottom) SPDT presses

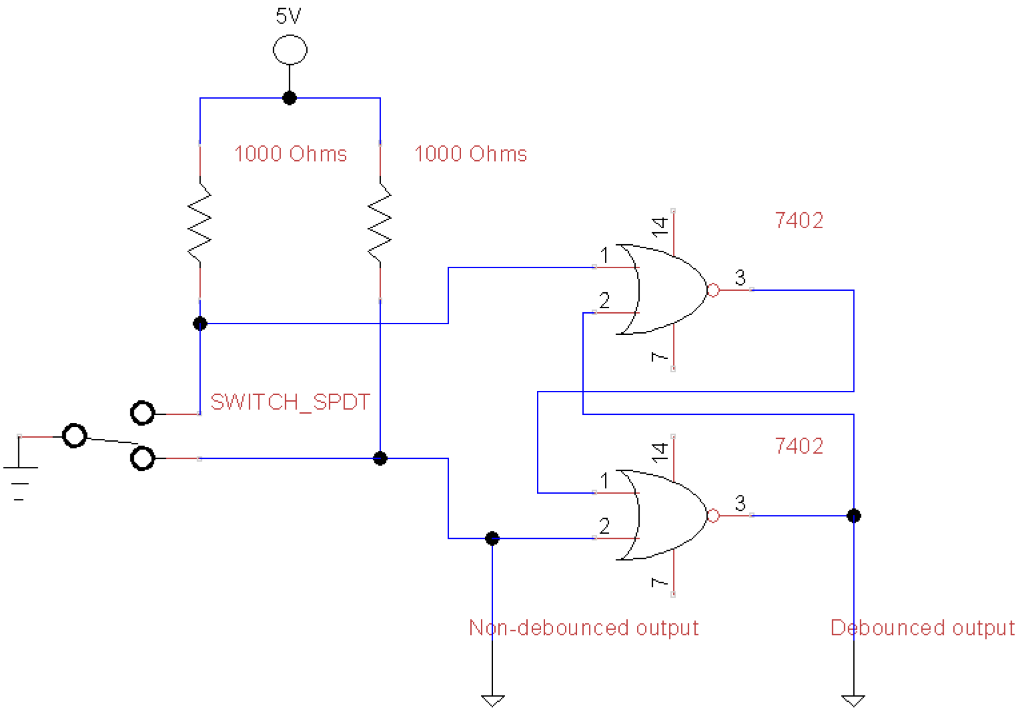


Figure 5: An SPDT debouncer constructed from NOR gates. For clarity, VCC and ground for gates are not connected in figure.