University of Victoria

CENG 241

Digital Design I

Lab 5 - Sequential Circuits: Flip-Flops and Counters

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A01 - B03

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1 Introduction

Sequential logic depends on present and past signals to determine the system's next state, hence sequential circuits have memory. The SR latches, D flip flops, T flip flops, and counters are examples of sequential circuits; they will be explored in this lab.

2 555 Timer

The required duty cycle of 50% and frequency of a few hertz were obtained from using resistors $R_a = 330\Omega$, $R_b = 1M\Omega$ and a capacitor $C = 0.1\mu\Omega$. From the following formulas,

$$Clock\ frequency = \frac{1.44}{(R_a + 2R_b)C}$$

$$Duty\ cycle = \frac{R_a + R_b}{R_a + 2R_b}$$

the expected clock frequency and duty cycle was calculated to be 7.2Hz and 50% respectfully. Figure 1 shows the experimental frequency of 8.2Hz with a duty cycle of 54.08%. Resistance and capacitance in the leads may account for these discrepancies.

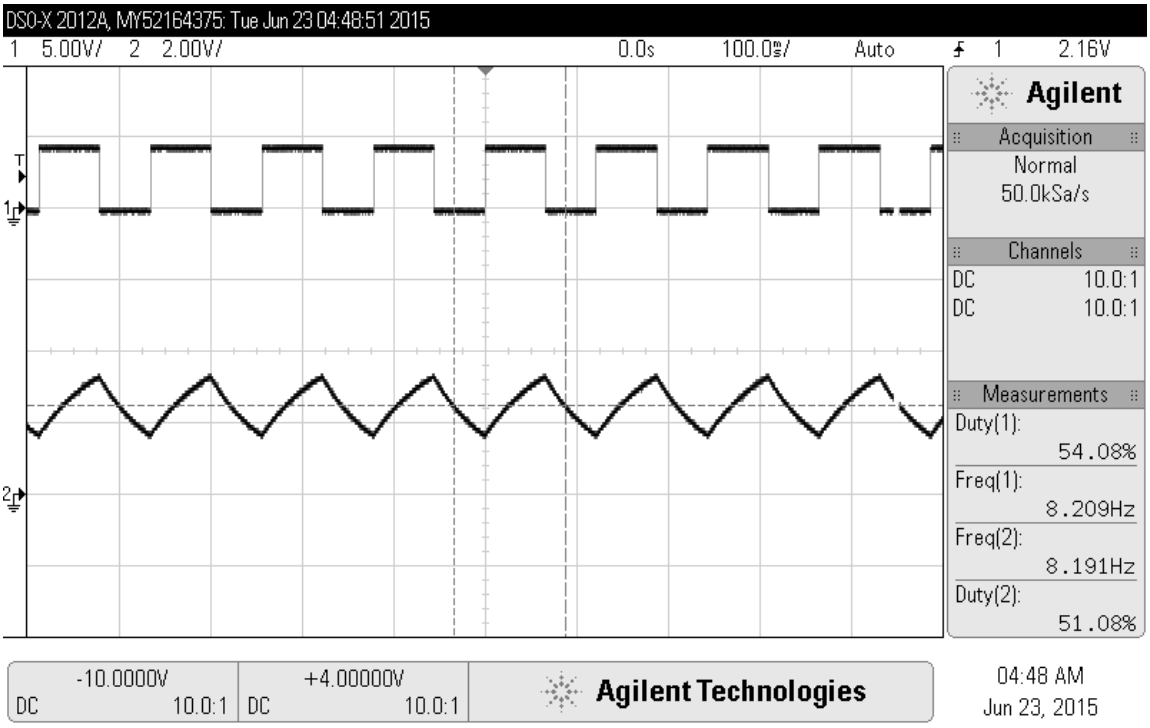

Figure 1: Output of the timer pin (top) and capacitor pin (bottom) for a 555 timer

3 RS Latch

- schematic of latch with two inverters on output

Figure 2 shows an undebounced oscillation resulting from the response of switching RS = 00 to RS = 11. A value of 130ns is obtained from measuring the peak to peak period from the

graph in this figure. Two 74C04 inverters were added to the RS latch circuit to extend the propagation delay enough to capture its effects. The 74C04 inverters advertise a typical 50ns delay with a maximum value of 90ns. Each 74LS00 NAND gates advertise a minimum 3ns to a maximum 15ns propagation delay. The total manufactured propagation delay for this circuit would be a minimum of 106ns to a maximum of 210ns, which confirms our result of 130ns.

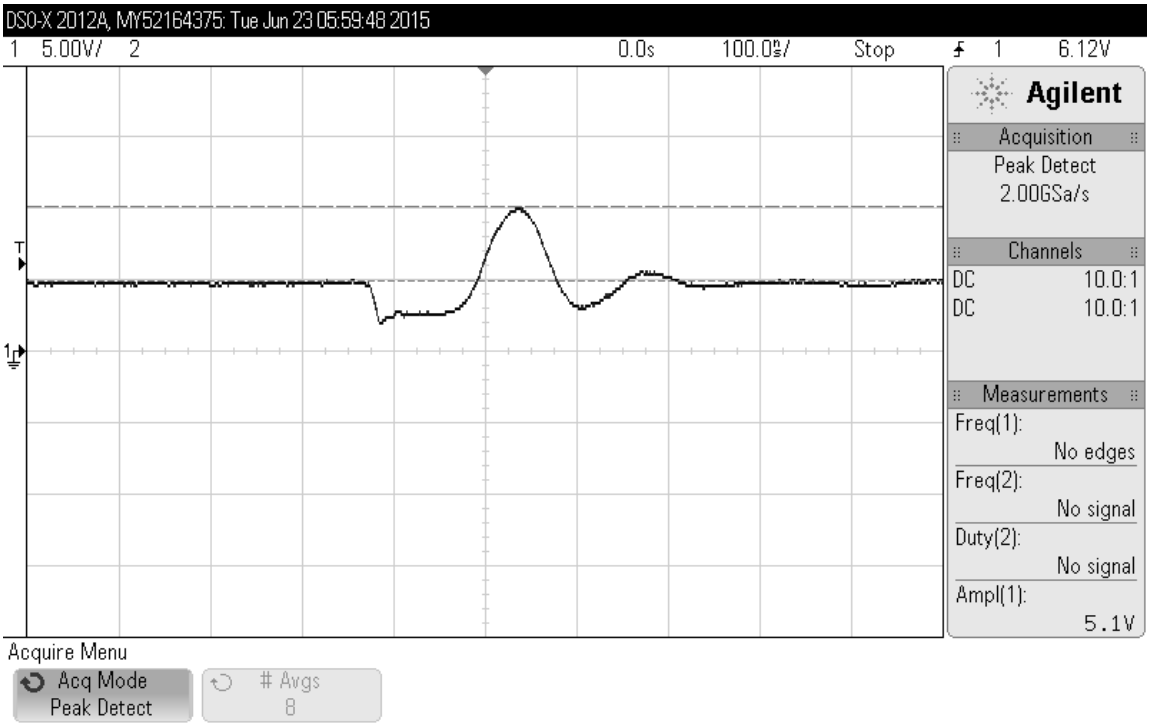

Figure 2: Oscillatory output of an RS latch in the indeterminate state

4 D Flip-Flop

Figure 3 shows the negative edge triggered D flip-flop. The D flip-flop has two inputs: a clock signal, and an input signal. The output reflects the input only during the brief moment of the falling edge of the clock and keeps that state until the next falling edge where it reevaluates its state from the input.

5 T Flip-Flop

The T flip-flop is shown in figure 4. It performs analogously to the D flip-flop except this flip-flop's input is the T signal XOR with the output Q(t) to give the next state Q(t+1). Also, similar to the D flip-flop above, this flip-flop is triggered on falling edges only. With the input signal $T = 1$, the output will alternate between 1 and 0.

6 Counter

**** Tyler you might need to help me with this one. I don't understand it enough to explain it properly. Why is it not in the range 3-12 in the first few cycles??

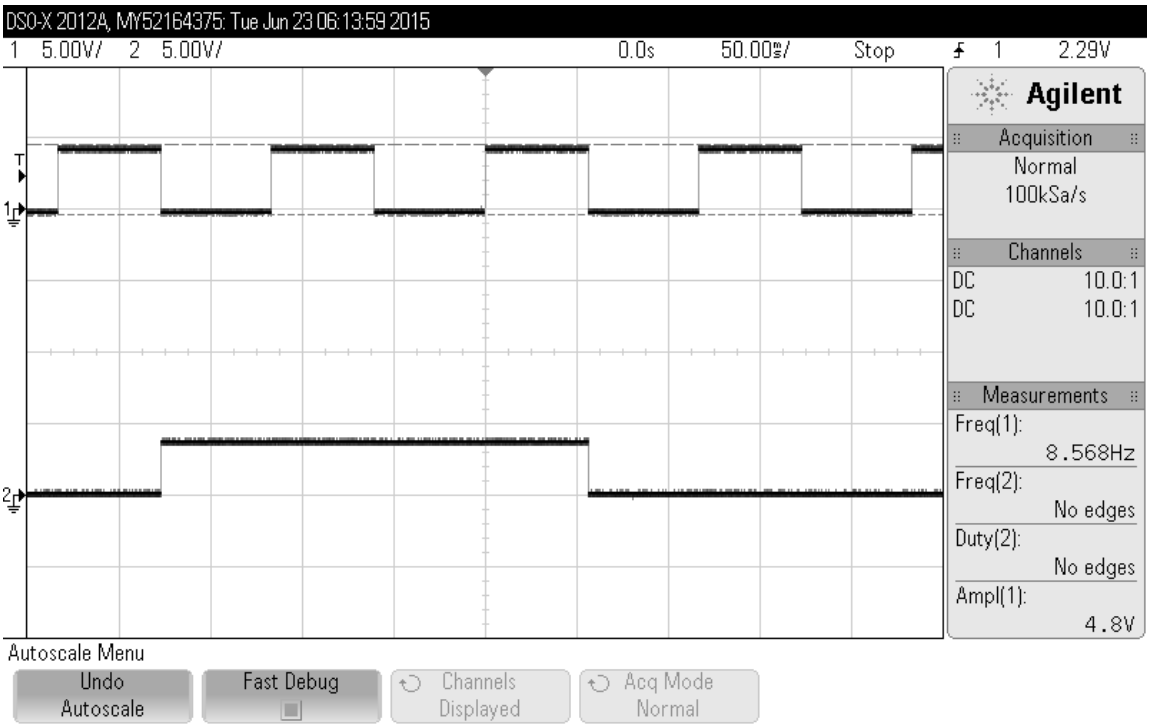

Figure 3: The D flip-flop only updates its value on the falling edge

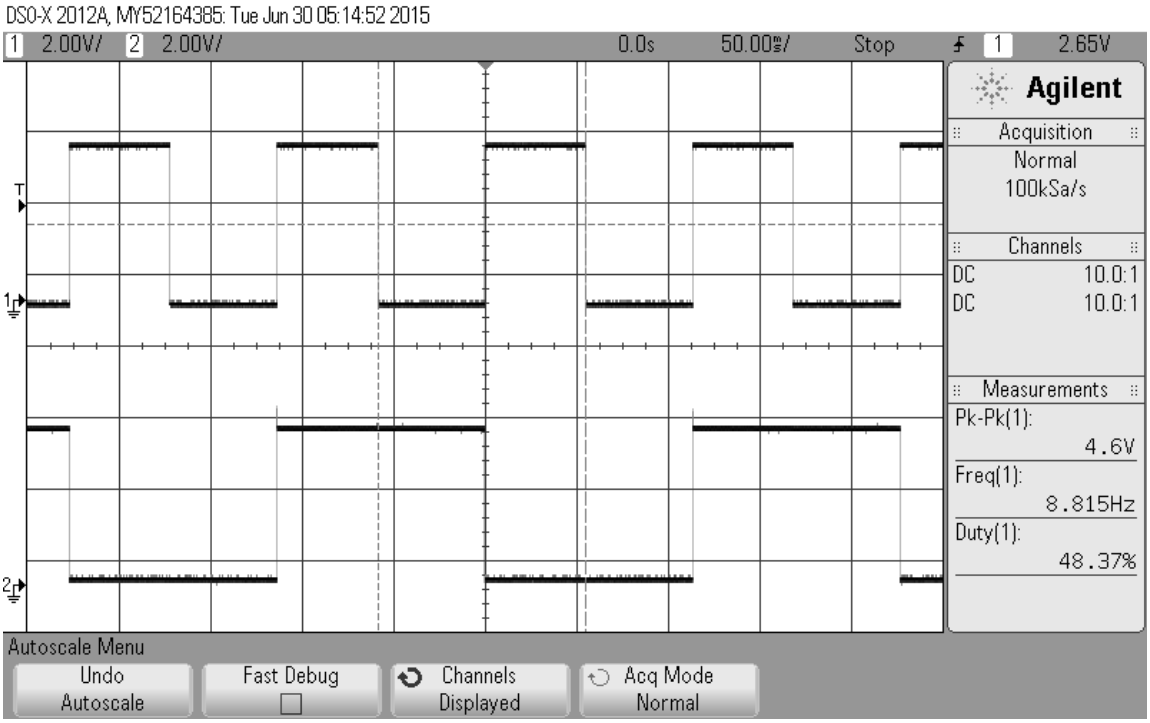

Figure 4: Output of a T flip-flop for $T = 1$

Figure 5 is a schematic of the counter circuit built which counts from 3 to 12. The input signal P is preset to 3 (0011): P_0 and P_1 are connected to V_{cc} (high), while P_2 and P_3 are connected to ground (low). P_e, the enable, is activated on a low signal, which happens at the value of 12: $P_2 = 1$ and $P_3 = 1$. When this occurs, the counter is reset to its preset input 0011.

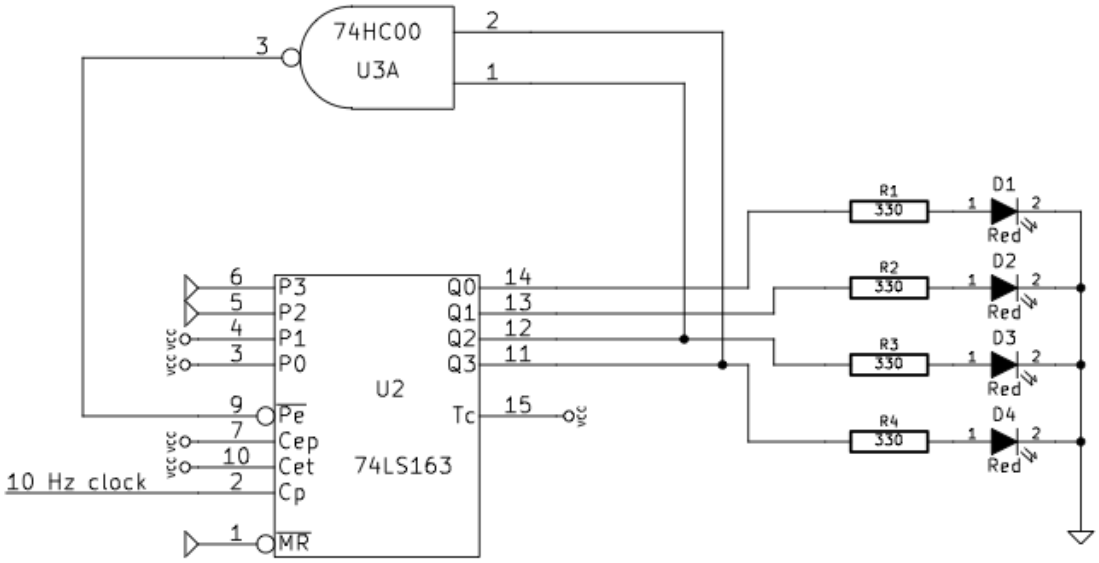

Figure 5: 74LS163 used to count 3 to 12 before resetting

7 Conclusion

Sequential logic was explored in this lab. A common relationship between these circuits is that they require the present output to determine its next state; in a sense, these circuits have memory.