University of Victoria

CENG 241

DIGITAL DESIGN I

Lab 4 - 4-bit Binary Adder / Subtractor

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1 Introduction

2 Discussion

2.1 Binary addition and subtraction using ones complement representation

A detailed discussion of how the 4-bit adder can be changed into 4-bit subtractor using XOR gates and only one control signal.

2.2 Building the hierarchical adder / subtractor

A general discussion of the design and the lab.

2.2.1 Half adder

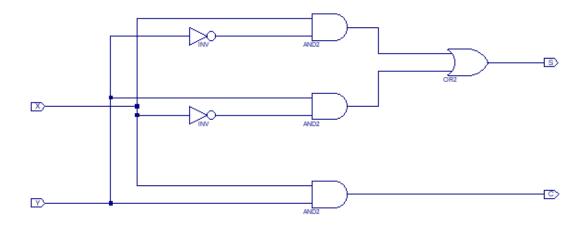


Figure 1: Schematic of the half adder

													426.	8 ns	S		
Current Simulation Time: 1000 ns		0 ns I I	ı	100 ns	I	2 	00 ns	1 1	300	ns		40 I	ns	ı	ı	500 I	ns
≩ ∏ COUT	1																
ઢ ∏ SOUT	0																
MIX 🕰	1																
MY 🛴	1																

Figure 2: Test results of the half adder

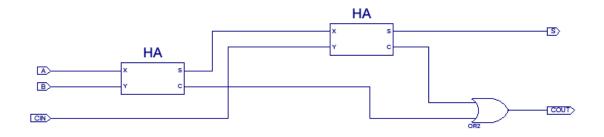


Figure 3: Schematic of the full adder

																													840.	2 ns
Current Simulation Time: 900 ns		0 ns I I	1	100 r	is I	1 1	200 I	ns	ı	3 1 1	1 008	ns I	L	400 I	ns	ı	5 I I	00 ns	5 	1	600	ns	ı	ı	700 I	ns	8	300 n	s I	900 ns
AIN II	1																													
∛ ∬ BIN	1																													
∳ ∬ CIN_IN	1																													
∛ ∬ SOUT	1																													
3 ∬ COUT_OUT	1																													

Figure 4: Test results of the full adder

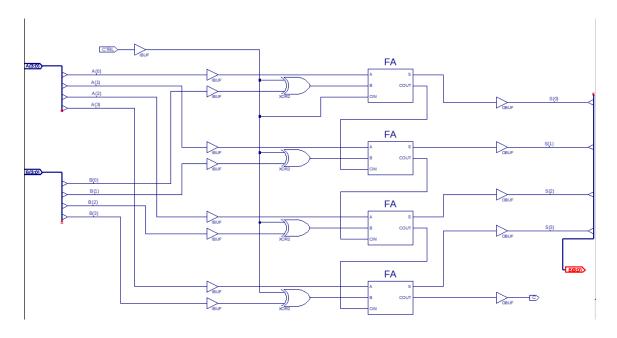


Figure 5: Schematic of the adder / subtractor



Figure 6: Test results of the adder / subtractor

CTRL	A	В	S	С
0	1	4	5	0
0	-3	2	-1	0
0	-5	-1	-6	1
0	7	6	-3	0
0	-5	-5	7	1
1	4	2	2	1
1	4	-1	5	0
1	-2	3	-5	1
1	-3	-4	1	1
1	4	-6	-6	0
1	-5	4	7	1

Table 1: Output of the adder / subtractor for several test cases, in decimal

- 2.2.2 Full adder
- 2.2.3 Adder / subtractor
- 2.3 Verilog hierarchical adder / subtractor

2.3.1 Listings

```
module FA(A, B, CIN, S, COUT)
input A, B, CIN;
output S, COUT;

HA U0(A, B, S0, C0);
HA U1(S0, CIN, S, C1);

assign COUT = C0 | C1;
```

FA.v

```
module AddSub(A0, A1, A2, A3, B0, B1, B2, B3, CTRL, S0, S1, S2, S3, C)
input A0, A1, A2, A3, B0, B1, B2, B3, CTRL;
output S0, S1, S2, S3, C;

FA U0(A0, B0 ^ CTRL, CTRL, S0, COUT0);
FA U1(A1, B1 ^ CTRL, COUT0, S1, COUT1);
FA U2(A2, B2 ^ CTRL, COUT1, S2, COUT2);
FA U3(A3, B3 ^ CTRL, COUT2, S3, C);
```

AddSub.v

2.3.2 Simulation results and delay times

3 Conclusion

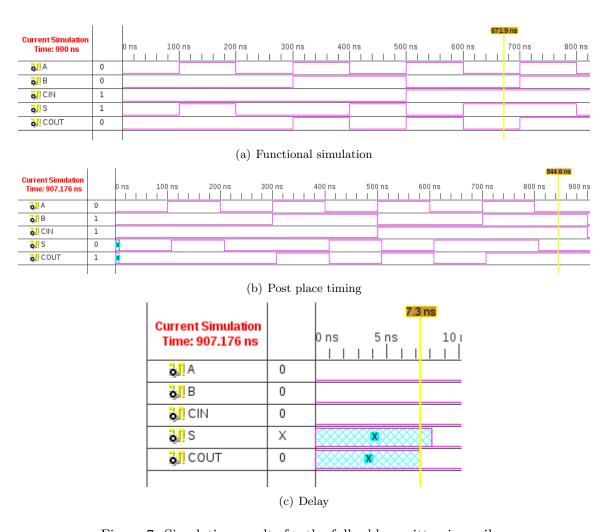


Figure 7: Simulation results for the full adder written in verilog

													725	i.2 ns
Current Simulation Time: 800 ns		0 ns 50 n	s 100 n	s 150 ns	200 ns	250 ns 30	0 ns 350 ns	400 ns	450 ns 5	500 ns 55	0 ns 600	ns 650 ns	700 ns	750 n 8 00 ns
≩ ∏ A0	1													
ઢ ∏ A1	1													
ઢ ∏ A2	0													
3 ∏ A3	1													
ઢ ∭ B0	0													
ઢ ∏ B1	0													
ढे ∏ B2	1													
ò ∏ B3	0													
3 ∏ CTRL	1													
3 ,∏ S0	1													
ઢ ∏ S1	1													
ઢ ∏ S2	1													
3 € S3	0													
∂ ∬ C	1													

Figure 8: Functional simulation results for adder / subtractor written in verilog