University of Victoria

CENG 241

Digital Design I

Lab 3
Combinational Circuits: 2-bit multiplier

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1 Introduction

Combinational circuits can be used to multiply binary numbers. One method is to chain full adders to reproduce the bit-wise multiplication of the numbers. The full adder uses some logic gates, such as XOR, which may not be readily available. This lab will explore the creation of a 2×2 bit multiplier using only NAND and INV gates.

2 Discussion

2.1 Determining logical expressions for multiplication output

Table 1 contains the truth table for multiplication where X_0 is the LSB. The expressions for C_i can be represented as Karnaugh maps, as shown in Figure 1.

A_1	A_0	B_1	B_0	C_3	C_2	C_1	C_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

Table 1: Truth table for 2×2 bit multiplier

Grouping the minterms in the Karnaugh maps gives the following boolean expressions for C_i:

$$
\begin{aligned}
C_0 &= A_0 B_0 \\
C_1 &= A_1 B_1' B_0 + A_1 A_0' B_0 + A_1' A_0 B_1 + A_0 B_1 B_0' \\
C_2 &= A_1 B_1 B_0' + A_1 A_0' B_1 \\
C_3 &= A_1 A_0 B_1 B_0.
\end{aligned}
$$

2.2 Designing and testing the schematic

The key to designing the schematic is to recognize that a NAND gate and an OR gate with inverted inputs are identical. Hence, the AND and OR gates in C_1 and C_2 are replaced with NAND gates. Since C_0 and C_3 have no corresponding OR, the output of the NAND is passed through an inverter to make the output equivalent to an AND. Figure 2 shows the complete schematic of the multiplier.

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	0	1	1	0
10	0	0	0	0

(a) C_0

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	1	0	1
10	0	1	1	0

(b) C_1

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	1
10	0	0	1	1

(c) C_2

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	1	0
10	0	0	0	0

(d) C_3

Figure 1: Karnaugh maps and term groupings for product terms C_i

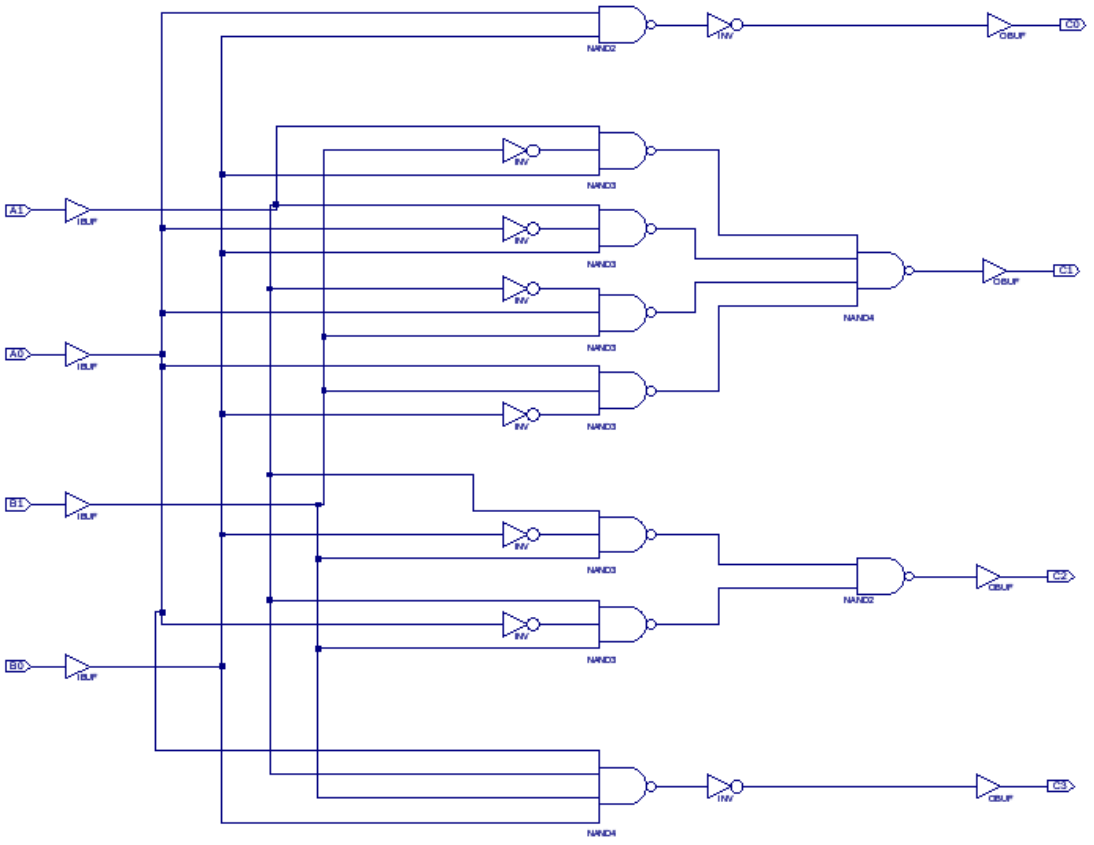

Figure 2: Complete schematic of 2-bit multiplier

This schematic was tested in Xilinx to confirm that its output matched Table 1. The functional simulation in Figure 3 confirms that the schematic will give the desired output.

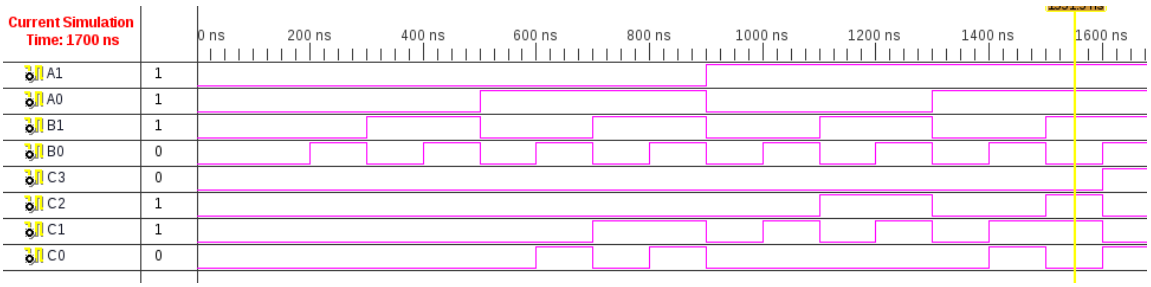

Figure 3: Functional simulation of a 2-bit multiplier

2.3 Building the multiplier

Since each expression for C_i is independent, the circuits were built one at a time. This simplified testing the design by reducing the number of ICs and wires on the board at one time. The smaller circuit was easier to construct and to debug.

The output of the multiplication term was passed through an LED where an illumination indicated logic high. Building each of the circuits in sequence and testing it with the sixteen possible input combinations confirmed the results of the functional simulation.

3 Conclusion

This lab confirmed that it is possible to built a 2×2 bit multiplier with only NAND and INV gates. Due to the large number of connections between ICs, building the circuit out of actually existing gates is exceedingly difficult without confirmation of intermediary results.