University of Victoria

CENG 241

Digital Design I

Lab 3
Combinational Circuits: 2-bit multiplier

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A01 - B03

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1 Introduction

2 Discussion

A_1	A_0	B_1	B_0	C_3	C_2	C_1	C_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

Table 1: Truth table for 2-bit by 2-bit multiplier

$$
\begin{aligned}
C_0 &= A_0 B_0 \\
C_1 &= A_1 B_1' B_0 + A_1 A_0' B_0 + A_1' A_0 B_1 + A_0 B_1 B_0' \\
C_2 &= A_1 B_1 B_0' + A_1 A_0' B_1 \\
C_3 &= A_1 A_0 B_1 B_0
\end{aligned}
$$

A general discussion of the design and the lab

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	0	1	1	0
10	0	0	0	0

(a) C_0

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	1	0	1
10	0	1	1	0

(b) C_1

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	1
10	0	0	1	1

(c) C_2

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	1	0
10	0	0	0	0

(d) C_3

Figure 1: Karnaugh maps and term groupings for product terms C_i

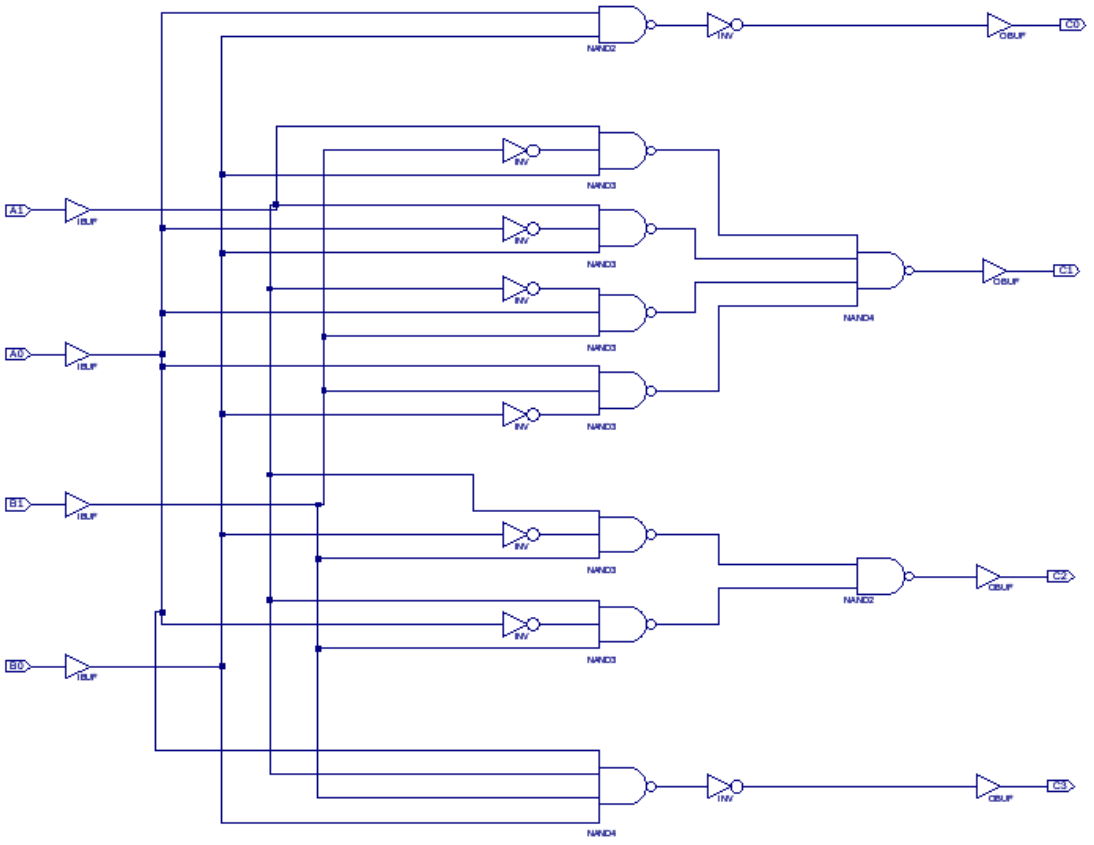

Figure 2: Complete schematic of 2-bit multiplier

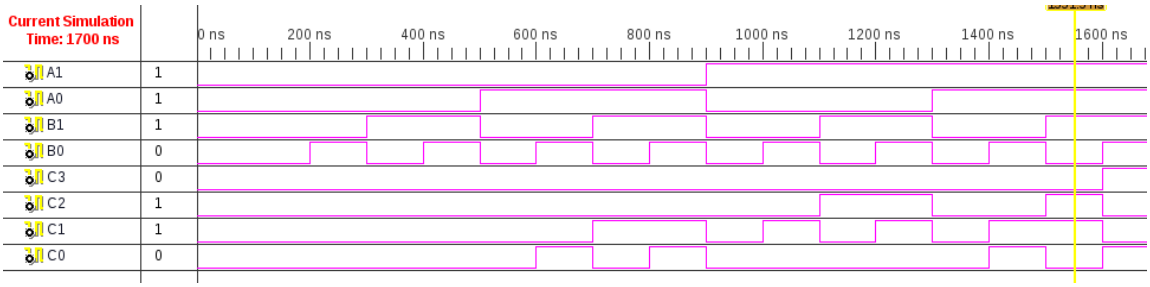

Figure 3: Functional simulation of a 2-bit multiplier