University of Victoria

CENG 241

Digital Design I

Lab 5 - Sequential Circuits: Flip-Flops and Counters

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A01 - B03

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1 Introduction

Sequential logic depends on present and past signals to determine the system's next state, hence sequential circuits have memory. The SR latches, D flip flops, T flip flops, and counters are examples of sequential circuits; they will be explored in this lab.

2 555 Timer

The required duty cycle of 50% and frequency of a few hertz were obtained from using resistors $R_a = 330\Omega$, $R_b = 1M\Omega$ and a capacitor $C = 0.1\mu\Omega$. From the following formulas,

$$Clock\ frequency = \frac{1.44}{(R_a + 2R_b)C}$$

$$Duty\ cycle = \frac{R_a + R_b}{R_a + 2R_b}$$

the expected clock frequency and duty cycle was calculated to be 7.2Hz and 50% respectfully. Figure 1 shows the experimental frequency of 8.2Hz with a duty cycle of 54.08%. Resistance and capacitance in the leads may account for these discrepancies.

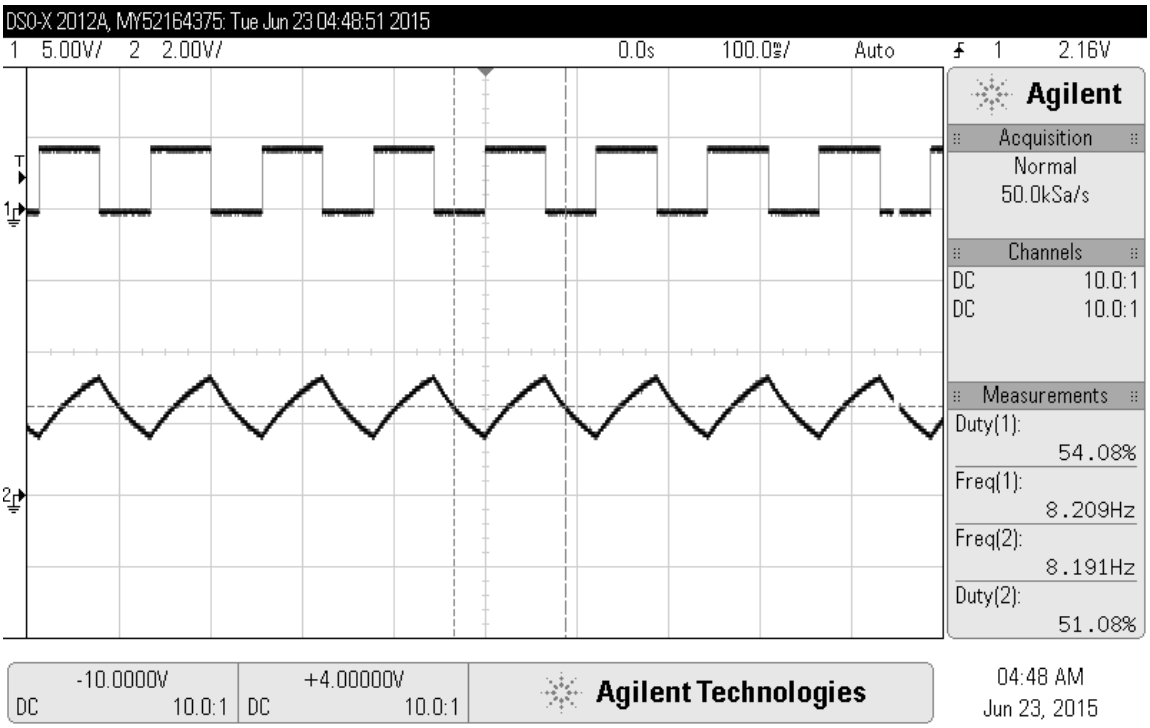

Figure 1: Output of the timer pin (top) and capacitor pin (bottom) for a 555 timer

3 RS Latch

- schematic of latch with two inverters on output
- screenshot of oscillations at 00/11
- how does frequency of oscilations relate to delay in circuit?

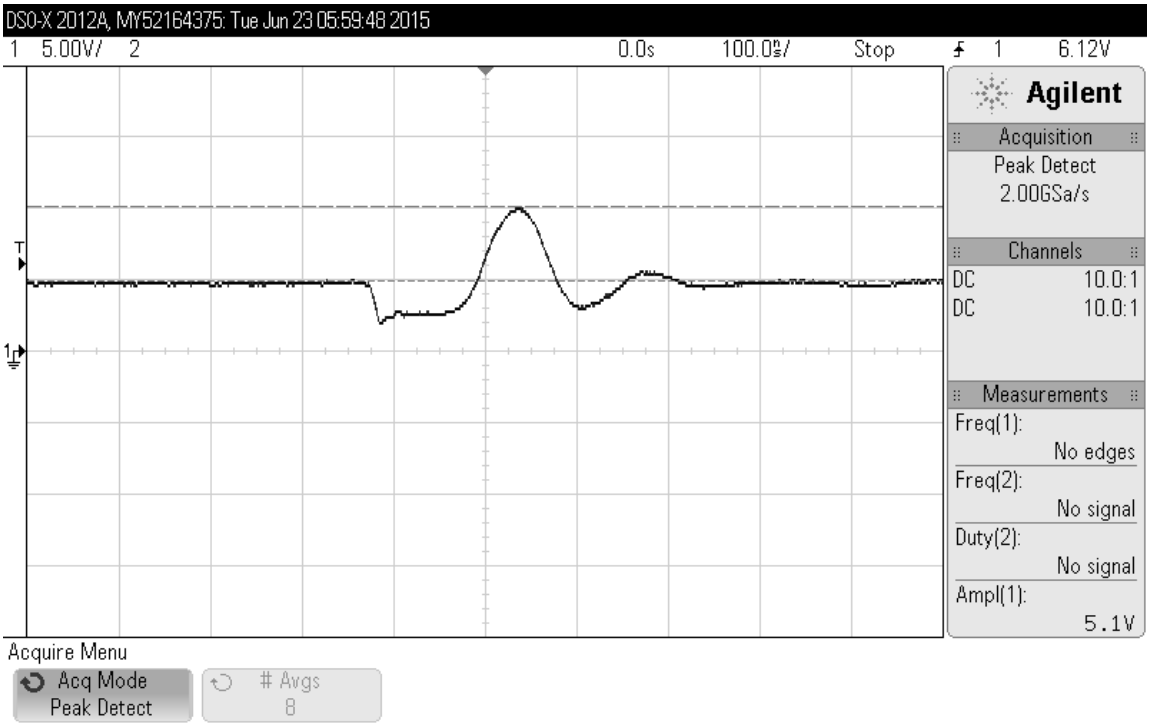

Figure 2: Oscillatory output of an RS latch in the indeterminate state

4 D Flip-Flop

- screenshot of D-FF changing on negative edge
- description of how D-FF works

5 T Flip-Flop

- screenshot for T=1

6 Counter

- schematic of circuit as built in lab
- Explain why the output of the circuit is not in the range of 3 to 12 in the first few clock cycles.

7 Conclusion

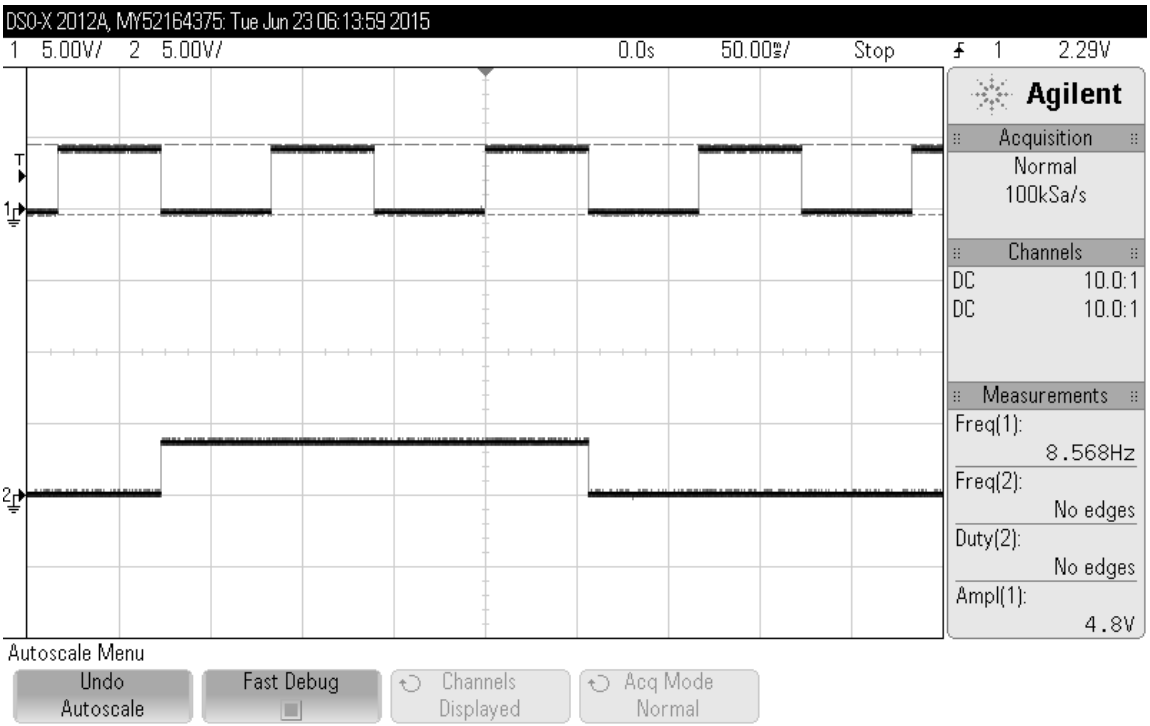

Figure 3: The D flip-flop only updates its value on the falling edge

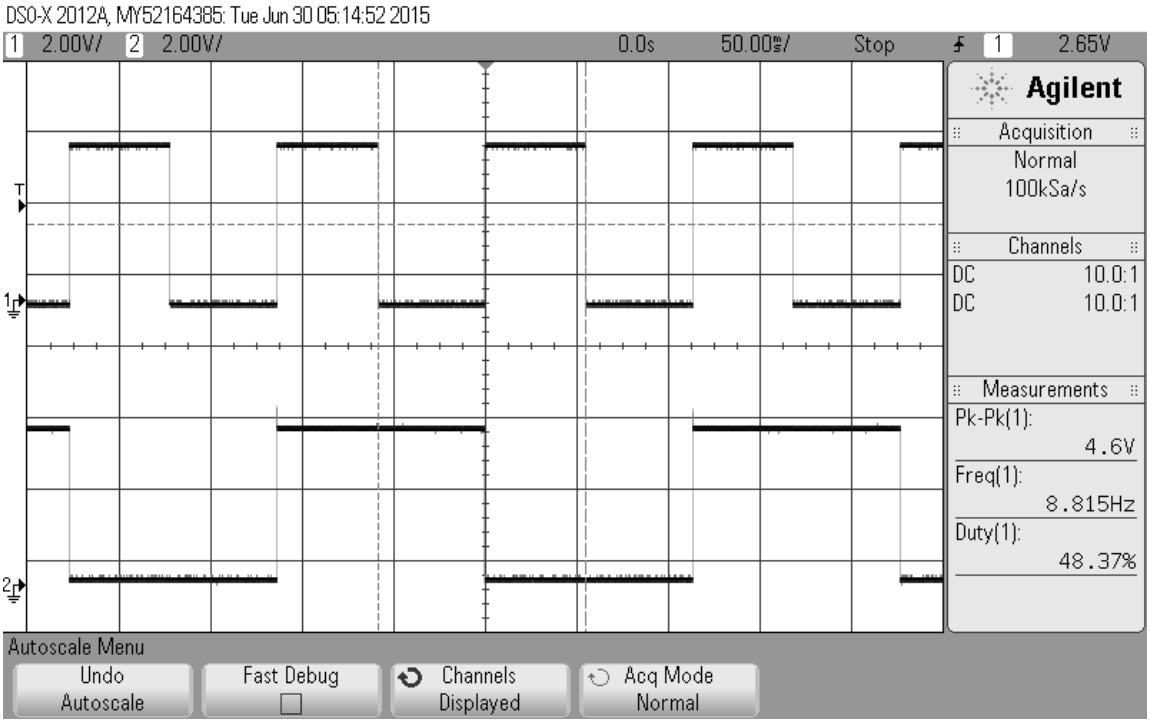

Figure 4: Output of a T flip-flop for $T = 1$

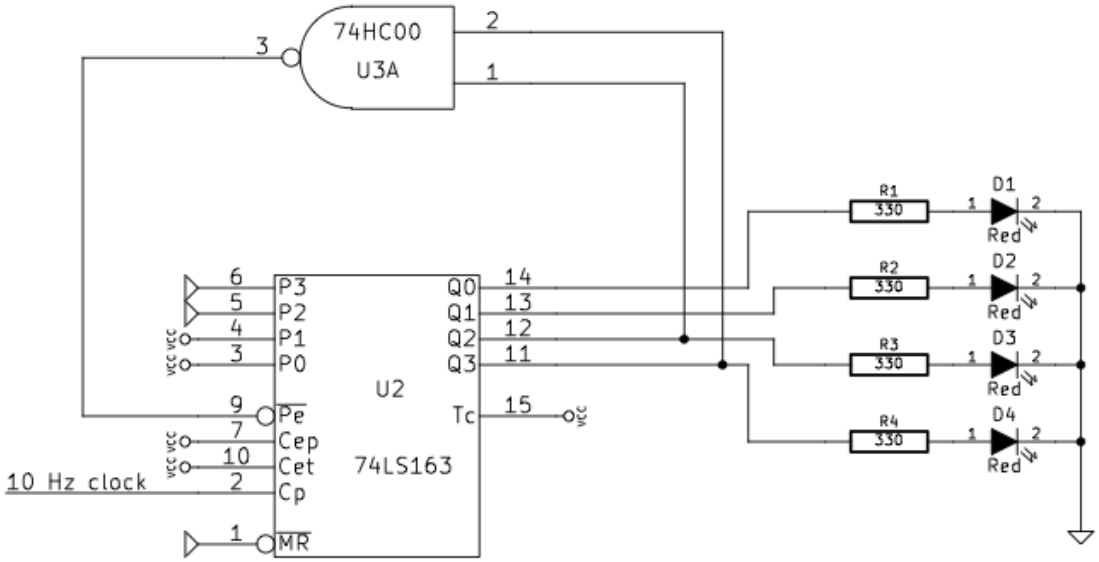

Figure 5: 74LS163 used to count 3 to 12 before resetting