Department of Electrical and Computer Engineering

University of Victoria

ELEC 300 - Linear Circuits II

# Laboratory Report

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| Experiment No.: | 2 |
| Title: | Frequency response of linear systems |
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| To: | TA, B07 |
| Names: | M. Drinnan (V00755525) |
| | T. Mulligan (V00819591) |
| | T. Stephen (V00812021) |

# 1 Objective

This experiment will create a type of RC circuit called a *phase lag circuit*. The circuit's transfer function will be used to determine the component values in the circuit for pre-defined frequency responses. The magnitude and phase responses of the circuit will be examined for a range of input frequencies.

# 2 Introduction

The transfer function of an electric circuit holds important information about the circuit's response to excitation by different frequencies. A transfer function has the form of:

$$H(s) = K\frac{s-z}{s-p} \tag{1}$$

where the values of $K$, $p$ and $z$ are determined the the circuit configuration. The values of $s = z$ and $s = p$ are the *poles* and *zeros* of the transfer function and correspond to frequencies that will alter the frequency response of the circuit.

This experiment examines the frequency response of the circuit shown in Fig. 1

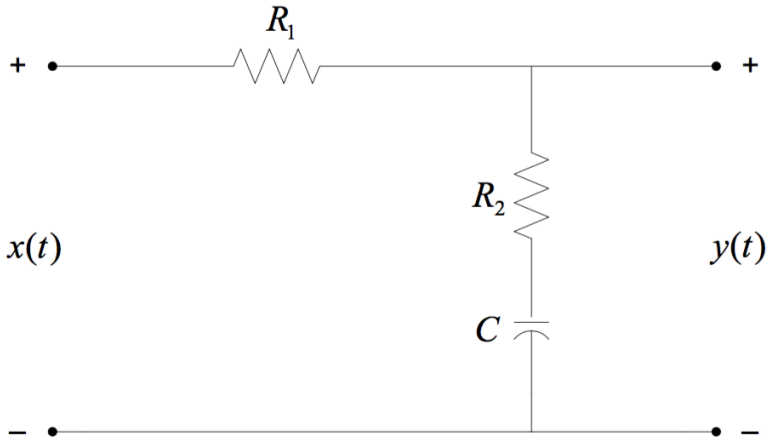



Figure 1: Schematic of a phase lag circuit

The transfer function of this circuit is:

$$H(s) = \frac{R_2 + \frac{1}{sC}}{R_1 + R_2 + \frac{1}{sC}} = \frac{R_2}{R_1 + R_2}\frac{s + \frac{1}{CR_2}}{s + \frac{1}{C(R_1+R_2)}}. \tag{2}$$

Comparing (1) with (2) gives:

$$K = \frac{R_2}{R_1 + R_2}$$

$$|z| = \frac{1}{CR_2} \tag{3}$$

$$|p| = \frac{1}{C\left(R_1 + R_2\right)}. \tag{4}$$

The lab manual specified that the circuit would be designed such that there was a pole at $f = 1000\,\text{Hz}$ and a zero at $f = 10\,000\,\text{Hz}$. Using these values and the constraint $C = 0.01\,\text{nF}$, (3) and (4) yield $R_1 = 1.591\,\text{k}\Omega$ and $R_2 = 14.324\,\text{k}\Omega$. $R_1$ can be realized with a standard $1.6\,\text{k}\Omega$ resistor and $R_2$ can be realized from a $10\,\text{k}\Omega$ resistor in series with a $10\,\text{k}\Omega$ potentiometer tuned to $4324\,\Omega$.

## 3 Results

The circuit from Fig. 1 was constructed using $R_1$ and $R_2$ as determined in Section 2. The voltages were recorded for 500 Hz to 12.5 kHz and are recorded in Table 1.

| $f$ (kHz) | $V_y$ (V) | $\lvert H\left(j\omega\right)\rvert_{dB}$ | $\phi_{lag}$ (°) |
|---|---|---|---|
| 0.5 | 0.882 | −1.065 | −22.6 |
| 1.0 | 0.708 | −2.973 | −38 |
| 2.0 | 0.46 | −6.719 | −50.4 |
| 3.0 | 0.337 | −9.421 | −53.4 |
| 4.0 | 0.267 | −11.444 | −53 |
| 5.0 | 0.224 | −12.969 | −51.1 |
| 6.0 | 0.196 | −14.129 | −48.4 |
| 7.0 | 0.178 | −14.966 | −45.6 |
| 8.0 | 0.166 | −15.572 | −43 |
| 9.0 | 0.156 | −16.111 | −41 |
| 10.0 | 0.147 | −16.628 | −38 |
| 11.0 | 0.141 | −16.990 | −36 |
| 12.0 | 0.136 | −17.303 | −33 |

Table 1: Response of Fig. 1 to frequency change ($V_x = 1\,\text{V}$)

The magnitude of the frequency response is given by:

$$|H\left(j\omega\right)|_{dB} = 20 \times \log\left(\frac{V_y}{V_x}\right).$$

The phase response is given by:

$$\phi_{lag} = \phi_x - \phi_y.$$

The waveforms in Fig. 2, show the phase offset of the 2 waveforms, visible by the offset in vertical cursors demonstrating a time shift.

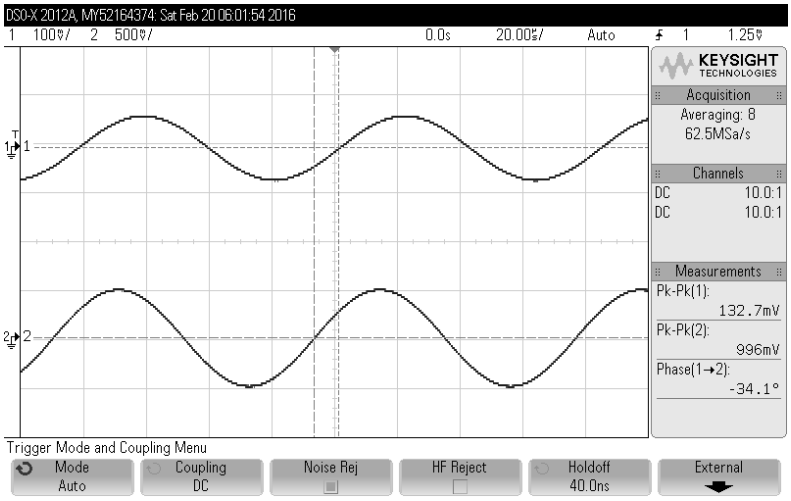
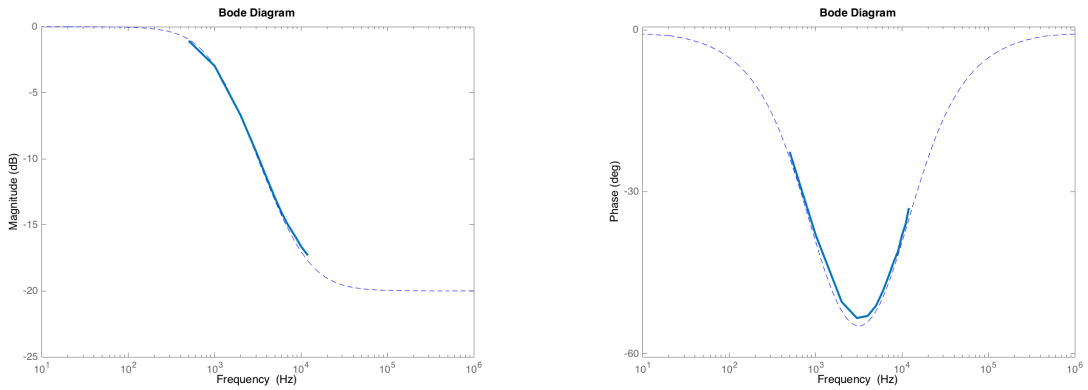



Figure 2: $V_y(t)$ (top) lags $V_x(t)$ (bottom) by 34.1° at 12 kHz

## 3.1 Analysis

Fig. 3 shows the data from Table 1 overlaying the ideal frequency response as predicted by (2).




(a) Magnitude response

(b) Phase response

Figure 3: Experimental data overlaying the ideal response

# 4 Discussion

In our pre-lab we simulated the phase and amplitude response of the phase-lag system. As can be seen in Fig. 3, the simulated results closely matched experimentally generated values. The phase plots in Fig. 3(b) both demonstrate a minimum phase of -55° occurring at  3kHz.

The measured phase response is slightly less negative than the simulated response, likely due to the ESR of the capacitors.

A phase-lag circuit receives its name from the characteristics exhibited by the circuit's transfer function. The output voltage's phase is shifted negatively by the circuit, resulting in a lagging phase.

# 5 Conclusion

Our results confirm a sinusoid is negatively shifted by a capacitor, as well as the low-pass filter nature of the voltage across a capacitor: when the frequency of the sinusoid across the capacitor the capacitor is low it acts similar to an open circuit, and when the frequency is high the capacitor acts like a short circuit. The negative phase shift behaviour of a capacitor justifies the circuit's *phase lag* denomination.