

Department of Electrical and Computer Engineering

University of Victoria

ELEC 300 - Linear Circuits II

LABORATORY REPORT

Experiment No.:	2
Title:	Frequency response of linear systems
Date of experiment:	19 February, 2016
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1 Objective

This experiment will create a type of RC circuit called a *phase lag circuit*. The circuit's transfer function will be used to determine the component values in the circuit for pre-defined frequency responses. The magnitude and phase responses of the circuit will be examined for a range of input frequencies.

2 Introduction

$$H(s) = K \frac{s - z}{s - p} \quad (1)$$

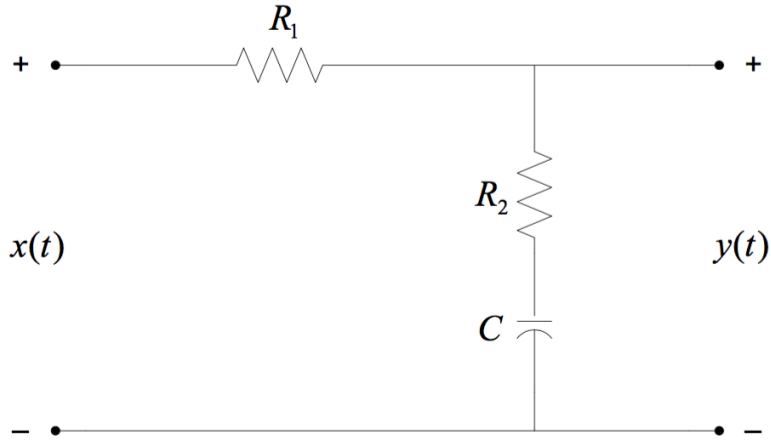


Figure 1: Schematic of a phase lag circuit

For the circuit in Fig. 1, the transfer function is:

$$H(s) = \frac{R_2 + \frac{1}{sC}}{R_1 + R_2 + \frac{1}{sC}} = \frac{R_2}{R_1 + R_2} \frac{s + \frac{1}{CR_2}}{s + \frac{1}{C(R_1 + R_2)}}. \quad (2)$$

Comparing (1) with (2) gives:

$$\begin{aligned} K &= \frac{R_2}{R_1 + R_2} \\ |z| &= \frac{1}{CR_2} \\ |p| &= \frac{1}{C(R_1 + R_2)}. \end{aligned}$$

3 Results

$$|H(j\omega)|_{dB} = 20 \times \log \left(\frac{V_y}{V_x} \right)$$

$$\phi_{lag} = \phi_x - \phi_y$$

f (kHz)	V_y (V)	$ H(j\omega) _{dB}$	ϕ_{lag} ($^\circ$)
0.5	0.882	-1.065	-22.6
1.0	0.708	-2.973	-38
2.0	0.46	-6.719	-50.4
3.0	0.337	-9.421	-53.4
4.0	0.267	-11.444	-53
5.0	0.224	-12.969	-51.1
6.0	0.196	-14.129	-48.4
7.0	0.178	-14.966	-45.6
8.0	0.166	-15.572	-43
9.0	0.156	-16.111	-41
10.0	0.147	-16.628	-38
11.0	0.141	-16.990	-36
12.0	0.136	-17.303	-33

Table 1: Response of Fig. 1 to frequency change ($V_x = 1$ V)

4 Discussion

A phase-lag circuit was built of an identical topology to that in Figure 1. The frequency of a 1V peak-to-peak input signal was varied over 12kHz in 1kHz increments. The input and output voltage and phase were measured using the in-lab oscilloscope. The recorded data can be seen in Table 1.

In our pre-lab, we simulated the phase and amplitude response of the phase-lag system. As can be seen by comparing Figures XXX and XXY, the simulated results closely matched experimentally generated values. Both phase plots show a minimum phase of -55° occurring at 3kHz. The capacitors used had an error of $\pm 20\%$. This might account for some of the difference between the simulated and experimental data.

A phase-lag circuit receives its name from the characteristics exhibited by the circuit's transfer function. The output voltage phase is always less than the input voltage phase, resulting in a constantly "lagging" phase.

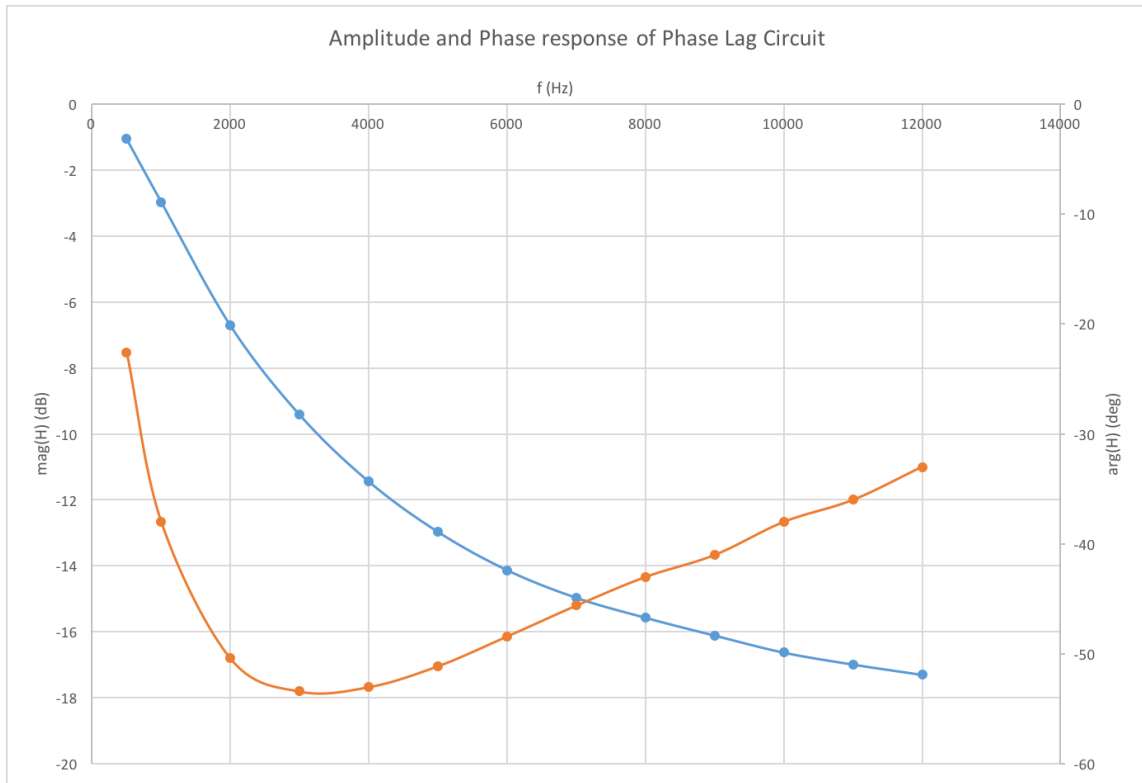


Figure 2: Response of Fig. 1 to frequency change ($V_x = 1\text{ V}$)

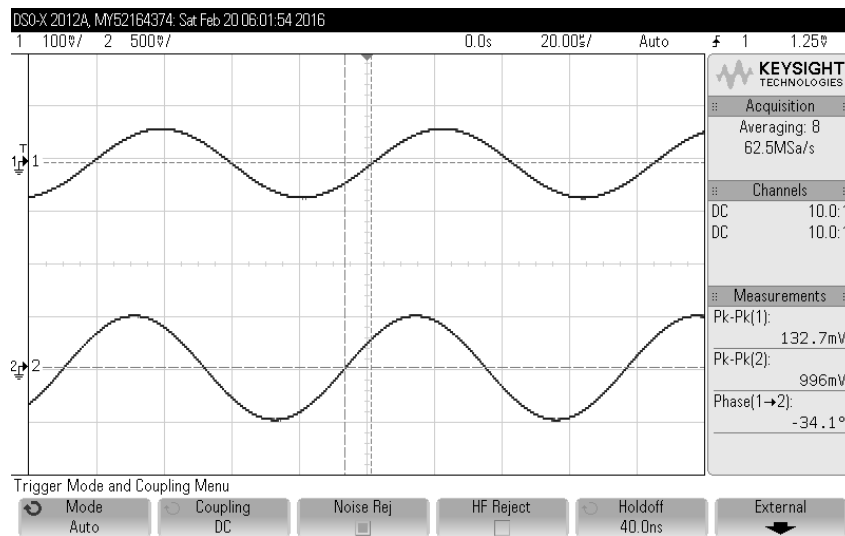


Figure 3: $V_y(t)$ (top) lags $V_x(t)$ (bottom) by 34.1° at 12 kHz

5 Conclusion

Justify conclusions and results.