Department of Electrical and Computer Engineering

University of Victoria

ELEC 300 - Linear Circuits II

Laboratory Report

Experiment No.:	4
Title:	Analysis and Applications of Active Networks
Date of experiment:	18 March, 2016
Report submitted on:	25 March, 2016
To:	H. Singh, B07
Names:	M. Drinnan (V00755525)
	T. Mulligan (V00819591)
	T. Stephen (V00812021)

1 Objective

This experiment will use active, first order circuits to explore s-domain network analysis.

2 Introduction

The Laplace transform, $X(s) = \mathscr{L}\{x(t)\}$, simplifies the analysis of complex networks by replacing network elements with their equivalent impedances. Integro-differential operations in the time-domain become algebraic operations in the Laplace s-domain.

A first order network with an active element can be generalized by the model shown in Fig. 1.

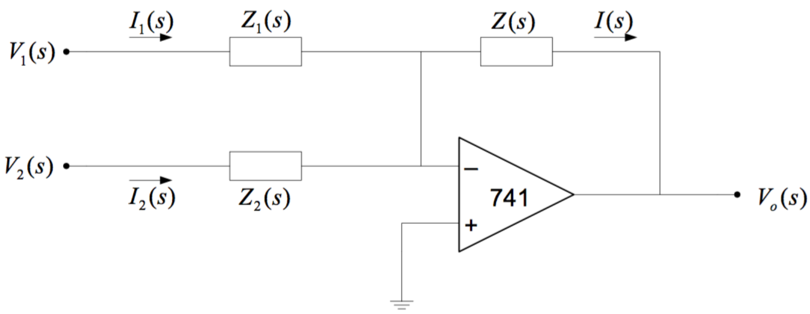


Figure 1: First order network in the s-domain

In the s-domain, the output is

$$V_o = -\left[\frac{Z}{Z_1}V_1 + \frac{Z}{Z_2}V_2\right] \tag{1}$$

This general configuration gives rise to many different circuits depending on the values of Z, Z_1 and Z_2.

Inverting Voltage Amplifier $Z = R$, $Z_1 = R_1$, $Z_2 = \infty$

$$V_o = -\frac{R}{R_1}V_1 \tag{2}$$

Inverting Adder $Z = R$, $Z_1 = R_1$, $Z_2 = R_2$

$$V_o = -\left[\frac{R}{R_1}V_1 + \frac{R}{R_2}V_2\right] \tag{3}$$

Inverting Integrator $Z = \frac{1}{sC}$, $Z_1 = R_1$, $Z_2 = \infty$

$$V_o = -\frac{1}{R_1 C} \cdot \frac{1}{s} V_1 = -G_1 \frac{1}{s} V_1 \tag{4}$$

In the time domain this becomes

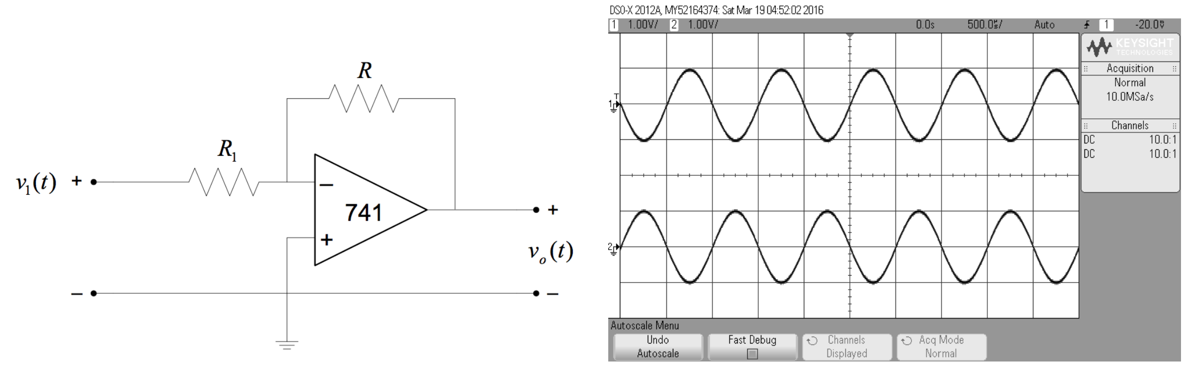
$$v_o(t) = -G_1 \int_0^t v_1(\tau) d\tau.$$

Inverting Integrator $Z = \frac{1}{sC}$, $Z_1 = R_1$, $Z_2 = R_2$

$$V_o = -\frac{1}{s} \left[\frac{1}{R_1 C} V_1 + \frac{1}{R_2 C} V_2 \right] \tag{5}$$

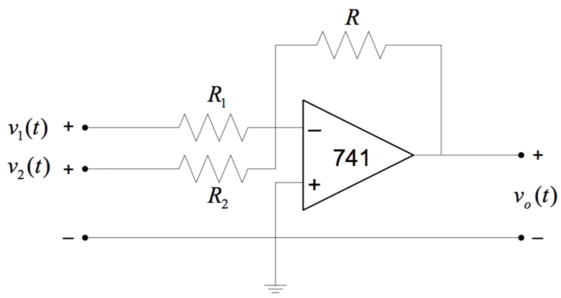
3 Results

Four circuits were assembled and analyzed using a function generator to apply a stimulus sinusoid of $1\mathrm{V_{pp}}$ at 1kHz, and an oscilloscope to measure the output of the system. Circuit schematics are taken from the lab manual [1].

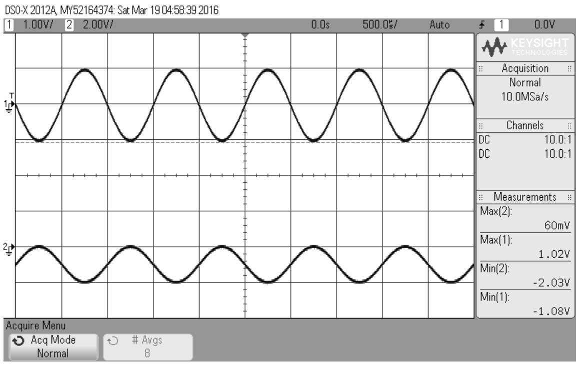


(a) $R_1 = R = 10\,\mathrm{k\Omega}$ (b) V_o, top; V_i, bottom

Figure 2: Inverter

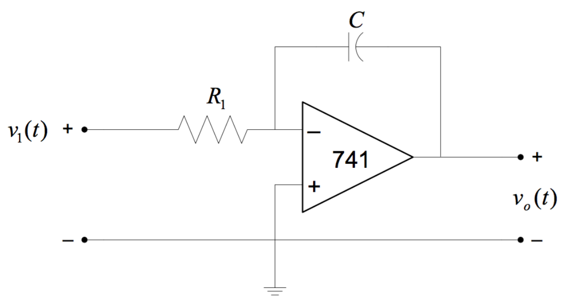


(a) $R = R_1 = R_2 = 10\,\mathrm{k\Omega}$

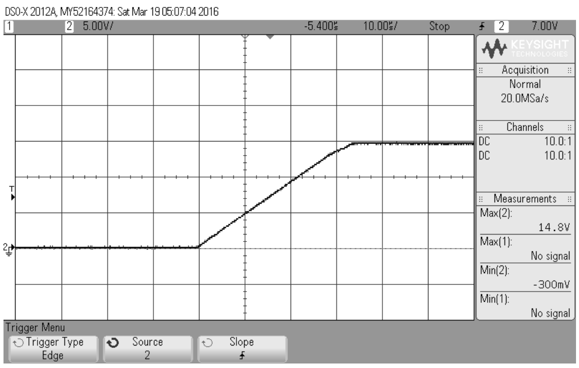


(b) V_o, top; V_i, bottom

Figure 3: Adder

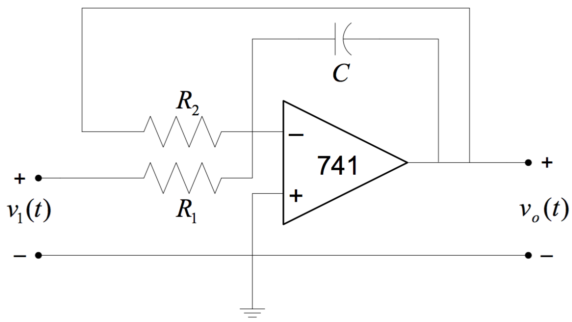


(a) $C = 16\,\mathrm{nF}$, $R_1 = 10\,\mathrm{k\Omega}$

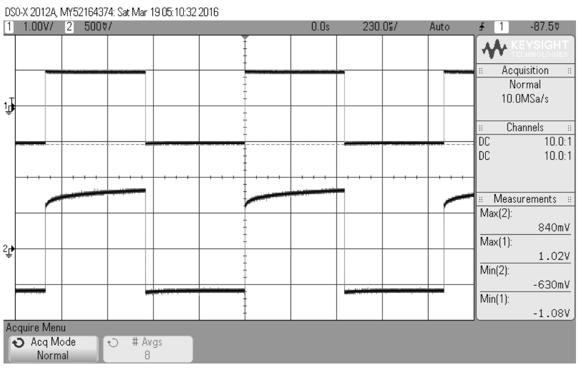


(b) Rising edge of V_o

Figure 4: Integrator



(a) $C = 16\,\mathrm{nF}$, $R_1 = R_2 = 10\,\mathrm{k\Omega}$



(b) V_i, top; V_o, bottom

Figure 5: Integrator as a first order system with feedback

4 Discussion

We confirmed frequency analysis through the Laplace transform is a valid and efficient way to analyze the response of a circuit in the time domain.

The output of the inverter circuit in Fig. 3 is of equal amplitude to the input waveform but has a gain of approximately -1. The expected gain of the circuit is

$$\text{Gain} = -\frac{R}{R_1} = -1$$

This is the expected behaviour of an inverter circuit.

Visible in Fig. 3, the output of the adder circuit is of the same phase as the input signal however the output signal is the result of adding the input signal to itself, resulting in the output being the input scaled by a factor of 2. This deviates from the experimental procedure of add a DC offset to the input sinusoid, however adding the input to itself confirms the adder circuit functions correctly when both inputs are time varying, or AC signals.

The output of the integrator circuit in Fig. 3 is the result of removing a short across the feedback capacitor, which acts as the integrating element. This ensures the integrator has an initial value of 0, and climbs to the op-amps saturation voltage of 15V when a DC input of approximately -0.1V is provided.

The final circuit, which is a first order system, demonstrates the expected response of such a system to a unit-step input: that is, the system approaches the input signal according to a time-decaying inverse exponential, which is visible in Fig. 3.

5 Conclusion

Justify conclusions and results.

References

[1] P. So and A. Zielinski, *Laboratory Manual for ELEC 300 - Linear Circuits II*, University of Victoria.