**FLIP FLOPS**

**D-FLIP FLOP:**

module DFlipFlop(D,clk,reset,Q,Qn);

input D;

input clk;

input reset;

output reg Q,Qn;

always @(posedge clk)

begin

if(reset==1)

begin

Q <= 0;

Qn <= 1;

end

else

begin

Q <= D;

Qn <= (~D);

end

end

endmodule

**WAVEFORM: **

**DESIGN SUMMARY:**

|  |  |  |  |
| --- | --- | --- | --- |
| **DFlipFlop Project Status (03/04/2024 - 11:21:13)** | | | |
| **Project File:** | D\_FF.xise | **Parser Errors:** | No Errors |
| **Module Name:** | DFlipFlop | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc6slx16-2ftg256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | No Warnings |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://21bec111/Implement/D_FF/DFlipFlop.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** | [All Constraints Met](D://21bec111/Implement/D_FF/DFlipFlop.ptwx?&DataKey=ConstraintsData) |
| **Environment:** | [System Settings](D://21bec111/Implement/D_FF/DFlipFlop_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://21bec111/Implement/D_FF/DFlipFlop.twx?&DataKey=XmlTimingReport) |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Registers | 0 | 18,224 | 0% |  | |
| Number of Slice LUTs | 1 | 9,112 | 1% |  | |
| Number used as logic | 1 | 9,112 | 1% |  | |
| Number using O6 output only | 1 |  |  |  | |
| Number using O5 output only | 0 |  |  |  | |
| Number using O5 and O6 | 0 |  |  |  | |
| Number used as ROM | 0 |  |  |  | |
| Number used as Memory | 0 | 2,176 | 0% |  | |
| Number of occupied Slices | 1 | 2,278 | 1% |  | |
| Number of MUXCYs used | 0 | 4,556 | 0% |  | |
| Number of LUT Flip Flop pairs used | 1 |  |  |  | |
| Number with an unused Flip Flop | 1 | 1 | 100% |  | |
| Number with an unused LUT | 0 | 1 | 0% |  | |
| Number of fully used LUT-FF pairs | 0 | 1 | 0% |  | |
| Number of slice register sites lost         to control set restrictions | 0 | 18,224 | 0% |  | |
| Number of bonded [IOBs](D://21bec111/Implement/D_FF/DFlipFlop_map.xrpt?&DataKey=IOBProperties) | 5 | 186 | 2% |  | |
| Number of LOCed IOBs | 5 | 5 | 100% |  | |
| IOB Flip Flops | 2 |  |  |  | |
| Number of RAMB16BWERs | 0 | 32 | 0% |  | |
| Number of RAMB8BWERs | 0 | 64 | 0% |  | |
| Number of BUFIO2/BUFIO2\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFIO2FB/BUFIO2FB\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFG/BUFGMUXs | 1 | 16 | 6% |  | |
| Number used as BUFGs | 1 |  |  |  | |
| Number used as BUFGMUX | 0 |  |  |  | |
| Number of DCM/DCM\_CLKGENs | 0 | 4 | 0% |  | |
| Number of ILOGIC2/ISERDES2s | 1 | 248 | 1% |  | |
| Number used as ILOGIC2s | 1 |  |  |  | |
| Number used as ISERDES2s | 0 |  |  |  | |
| Number of IODELAY2/IODRP2/IODRP2\_MCBs | 0 | 248 | 0% |  | |
| Number of OLOGIC2/OSERDES2s | 1 | 248 | 1% |  | |
| Number used as OLOGIC2s | 1 |  |  |  | |
| Number used as OSERDES2s | 0 |  |  |  | |
| Number of BSCANs | 0 | 4 | 0% |  | |
| Number of BUFHs | 0 | 128 | 0% |  | |
| Number of BUFPLLs | 0 | 8 | 0% |  | |
| Number of BUFPLL\_MCBs | 0 | 4 | 0% |  | |
| Number of DSP48A1s | 0 | 32 | 0% |  | |
| Number of ICAPs | 0 | 1 | 0% |  | |
| Number of MCBs | 0 | 2 | 0% |  | |
| Number of PCILOGICSEs | 0 | 2 | 0% |  | |
| Number of PLL\_ADVs | 0 | 2 | 0% |  | |
| Number of PMVs | 0 | 1 | 0% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of SUSPEND\_SYNCs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 0.86 |  |  |  | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Performance Summary** | | | | [**[-]**](?&ExpandedTable=PerformanceSummary) |
| **Final Timing Score:** | 0 (Setup: 0, Hold: 0) | **Pinout Data:** | [Pinout Report](D://21bec111/Implement/D_FF/DFlipFlop_par.xrpt?&DataKey=PinoutData) | |
| **Routing Results:** | [All Signals Completely Routed](D://21bec111/Implement/D_FF/DFlipFlop.unroutes) | **Clock Data:** | [Clock Report](D://21bec111/Implement/D_FF/DFlipFlop_par.xrpt?&DataKey=ClocksData) | |
| **Timing Constraints:** | [All Constraints Met](D://21bec111/Implement/D_FF/DFlipFlop.ptwx?&DataKey=ConstraintsData) |  |  | |
|  |  |  |  | |

**JK-FLIP FLOP:**

module jk\_ff (j, k, clk, q,x);

input j,k,clk;

output reg q,x;

wire c;

assign x=c;

div dd(clk,rst,c);

always @ (posedge c)

case ({j,k})

2'b00 : q <= q;

2'b01 : q <= 0;

2'b10 : q <= 1;

2'b11 : q <= ~q;

endcase

endmodule

module div(clk,rst,q);

input clk,rst;

output q;

reg [27:0]sig;

assign LED=q;

always @(posedge clk)

begin

if(rst==1)

sig=28'b0;

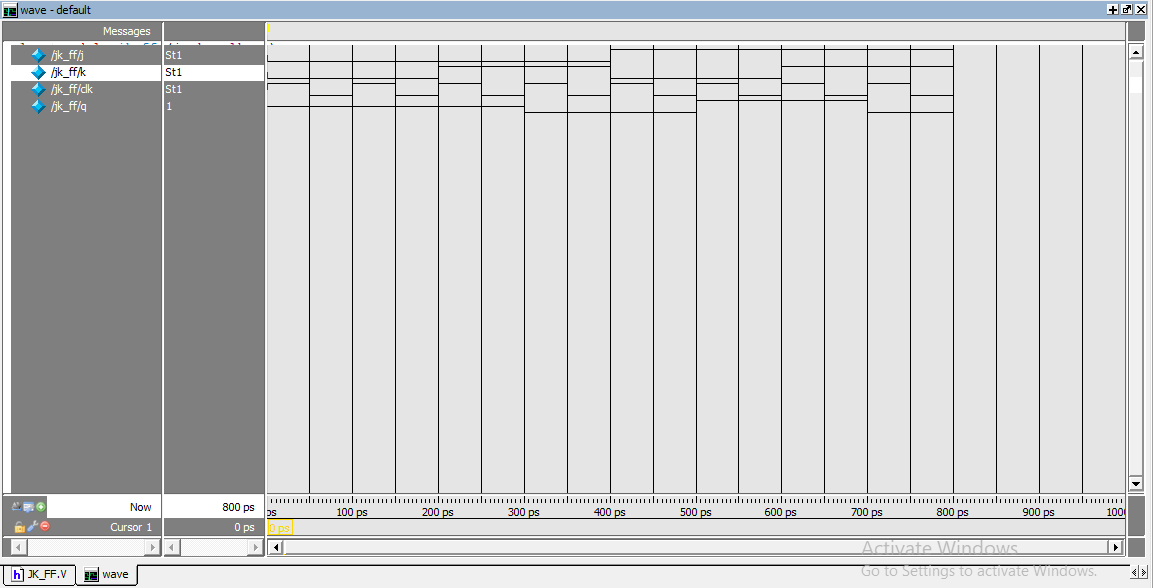
else if(rst==0)

sig=sig+1;

end

assign q=sig[24];

endmodule

**WAVEFORM:** 

**DESIGN SUMMARY:**

|  |  |  |  |
| --- | --- | --- | --- |
| **jk\_ff Project Status (03/04/2024 - 11:59:16)** | | | |
| **Project File:** | JK\_FF.xise | **Parser Errors:** | No Errors |
| **Module Name:** | jk\_ff | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc6slx16-2ftg256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | [7 Warnings (7 new)](D://21bec111/Implement/JK_FF/_xmsgs/*.xmsgs?&DataKey=Warning) |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://21bec111/Implement/JK_FF/jk_ff.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** | [All Constraints Met](D://21bec111/Implement/JK_FF/jk_ff.ptwx?&DataKey=ConstraintsData) |
| **Environment:** | [System Settings](D://21bec111/Implement/JK_FF/jk_ff_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://21bec111/Implement/JK_FF/jk_ff.twx?&DataKey=XmlTimingReport) |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Registers | 26 | 18,224 | 1% |  | |
| Number used as Flip Flops | 26 |  |  |  | |
| Number used as Latches | 0 |  |  |  | |
| Number used as Latch-thrus | 0 |  |  |  | |
| Number used as AND/OR logics | 0 |  |  |  | |
| Number of Slice LUTs | 26 | 9,112 | 1% |  | |
| Number used as logic | 25 | 9,112 | 1% |  | |
| Number using O6 output only | 0 |  |  |  | |
| Number using O5 output only | 23 |  |  |  | |
| Number using O5 and O6 | 2 |  |  |  | |
| Number used as ROM | 0 |  |  |  | |
| Number used as Memory | 0 | 2,176 | 0% |  | |
| Number used exclusively as route-thrus | 1 |  |  |  | |
| Number with same-slice register load | 0 |  |  |  | |
| Number with same-slice carry load | 1 |  |  |  | |
| Number with other load | 0 |  |  |  | |
| Number of occupied Slices | 8 | 2,278 | 1% |  | |
| Number of MUXCYs used | 28 | 4,556 | 1% |  | |
| Number of LUT Flip Flop pairs used | 26 |  |  |  | |
| Number with an unused Flip Flop | 0 | 26 | 0% |  | |
| Number with an unused LUT | 0 | 26 | 0% |  | |
| Number of fully used LUT-FF pairs | 26 | 26 | 100% |  | |
| Number of unique control sets | 2 |  |  |  | |
| Number of slice register sites lost         to control set restrictions | 14 | 18,224 | 1% |  | |
| Number of bonded [IOBs](D://21bec111/Implement/JK_FF/jk_ff_map.xrpt?&DataKey=IOBProperties) | 4 | 186 | 2% |  | |
| Number of LOCed IOBs | 4 | 4 | 100% |  | |
| Number of RAMB16BWERs | 0 | 32 | 0% |  | |
| Number of RAMB8BWERs | 0 | 64 | 0% |  | |
| Number of BUFIO2/BUFIO2\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFIO2FB/BUFIO2FB\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFG/BUFGMUXs | 1 | 16 | 6% |  | |
| Number used as BUFGs | 1 |  |  |  | |
| Number used as BUFGMUX | 0 |  |  |  | |
| Number of DCM/DCM\_CLKGENs | 0 | 4 | 0% |  | |
| Number of ILOGIC2/ISERDES2s | 0 | 248 | 0% |  | |
| Number of IODELAY2/IODRP2/IODRP2\_MCBs | 0 | 248 | 0% |  | |
| Number of OLOGIC2/OSERDES2s | 0 | 248 | 0% |  | |
| Number of BSCANs | 0 | 4 | 0% |  | |
| Number of BUFHs | 0 | 128 | 0% |  | |
| Number of BUFPLLs | 0 | 8 | 0% |  | |
| Number of BUFPLL\_MCBs | 0 | 4 | 0% |  | |
| Number of DSP48A1s | 0 | 32 | 0% |  | |
| Number of ICAPs | 0 | 1 | 0% |  | |
| Number of MCBs | 0 | 2 | 0% |  | |
| Number of PCILOGICSEs | 0 | 2 | 0% |  | |
| Number of PLL\_ADVs | 0 | 2 | 0% |  | |
| Number of PMVs | 0 | 1 | 0% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of SUSPEND\_SYNCs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 1.03 |  |  |  | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Performance Summary** | | | | [**[-]**](?&ExpandedTable=PerformanceSummary) |
| **Final Timing Score:** | 0 (Setup: 0, Hold: 0) | **Pinout Data:** | [Pinout Report](D://21bec111/Implement/JK_FF/jk_ff_par.xrpt?&DataKey=PinoutData) | |
| **Routing Results:** | [All Signals Completely Routed](D://21bec111/Implement/JK_FF/jk_ff.unroutes) | **Clock Data:** | [Clock Report](D://21bec111/Implement/JK_FF/jk_ff_par.xrpt?&DataKey=ClocksData) | |
| **Timing Constraints:** | [All Constraints Met](D://21bec111/Implement/JK_FF/jk_ff.ptwx?&DataKey=ConstraintsData) |  |  | |

**T-FLIP FLOP:**

module tff ( input t, input clk, input reset, output reg q,qb);

wire c;

div dd(clk,rst,c);

always @ (posedge c)

begin

if(reset == 1)

begin

q <= 0;

end

else

begin

if (t==0)

begin

q <= q;

qb <= q;

end

else

begin

q <= ~q;

qb <= q;

end

end

end

endmodule

module div(clk,rst,q);

input clk,rst;

output q;

reg [27:0]sig;

assign LED=q;

always @(posedge clk)

begin

if(rst==1)

sig=28'b0;

else if(rst==0)

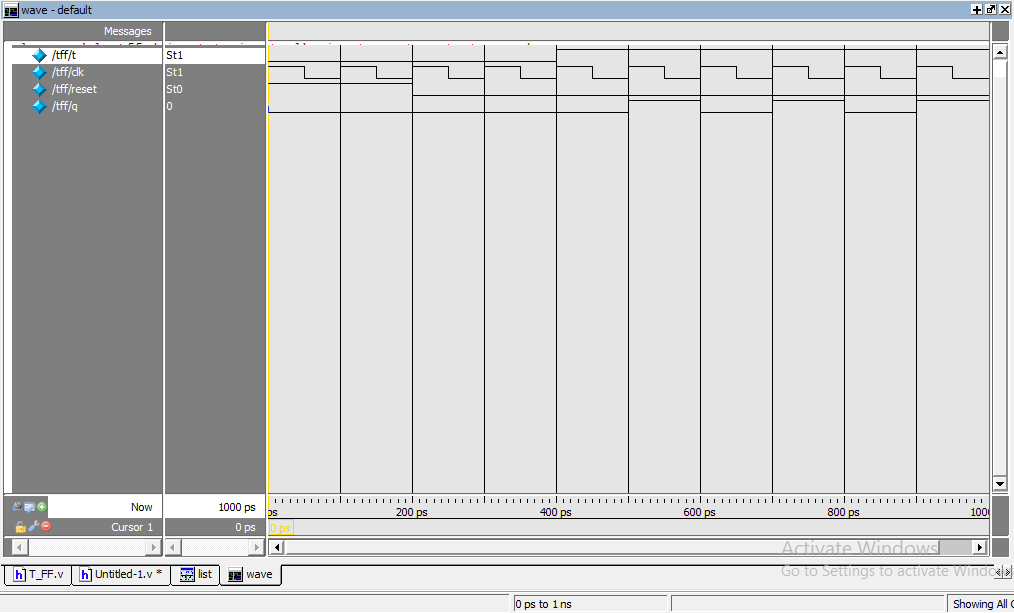
sig=sig+1;

end

assign q=sig[24];

endmodule

**WAVEFORM:**

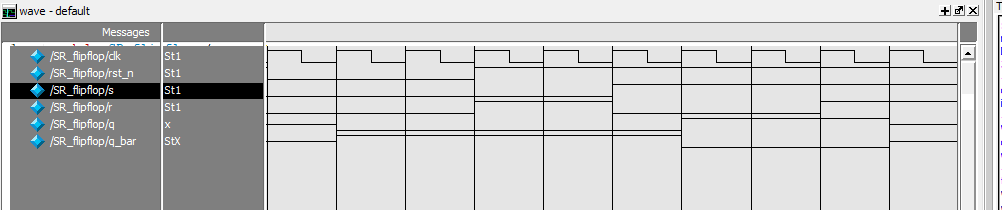


**DESIGN SUMMARY:**

|  |  |  |  |
| --- | --- | --- | --- |
| **tff Project Status (03/11/2024 - 13:20:49)** | | | |
| **Project File:** | T\_FF.xise | **Parser Errors:** | No Errors |
| **Module Name:** | tff | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc6slx16-2ftg256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | [7 Warnings (0 new)](D://21bec111/Implement/T_FF/_xmsgs/*.xmsgs?&DataKey=Warning) |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://21bec111/Implement/T_FF/tff.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** | [All Constraints Met](D://21bec111/Implement/T_FF/tff.ptwx?&DataKey=ConstraintsData) |
| **Environment:** | [System Settings](D://21bec111/Implement/T_FF/tff_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://21bec111/Implement/T_FF/tff.twx?&DataKey=XmlTimingReport) |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Registers | 27 | 18,224 | 1% |  | |
| Number used as Flip Flops | 27 |  |  |  | |
| Number used as Latches | 0 |  |  |  | |
| Number used as Latch-thrus | 0 |  |  |  | |
| Number used as AND/OR logics | 0 |  |  |  | |
| Number of Slice LUTs | 26 | 9,112 | 1% |  | |
| Number used as logic | 25 | 9,112 | 1% |  | |
| Number using O6 output only | 0 |  |  |  | |
| Number using O5 output only | 23 |  |  |  | |
| Number using O5 and O6 | 2 |  |  |  | |
| Number used as ROM | 0 |  |  |  | |
| Number used as Memory | 0 | 2,176 | 0% |  | |
| Number used exclusively as route-thrus | 1 |  |  |  | |
| Number with same-slice register load | 0 |  |  |  | |
| Number with same-slice carry load | 1 |  |  |  | |
| Number with other load | 0 |  |  |  | |
| Number of occupied Slices | 8 | 2,278 | 1% |  | |
| Number of MUXCYs used | 28 | 4,556 | 1% |  | |
| Number of LUT Flip Flop pairs used | 26 |  |  |  | |
| Number with an unused Flip Flop | 0 | 26 | 0% |  | |
| Number with an unused LUT | 0 | 26 | 0% |  | |
| Number of fully used LUT-FF pairs | 26 | 26 | 100% |  | |
| Number of unique control sets | 2 |  |  |  | |
| Number of slice register sites lost         to control set restrictions | 13 | 18,224 | 1% |  | |
| Number of bonded [IOBs](D://21bec111/Implement/T_FF/tff_map.xrpt?&DataKey=IOBProperties) | 5 | 186 | 2% |  | |
| Number of LOCed IOBs | 5 | 5 | 100% |  | |
| Number of RAMB16BWERs | 0 | 32 | 0% |  | |
| Number of RAMB8BWERs | 0 | 64 | 0% |  | |
| Number of BUFIO2/BUFIO2\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFIO2FB/BUFIO2FB\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFG/BUFGMUXs | 1 | 16 | 6% |  | |
| Number used as BUFGs | 1 |  |  |  | |
| Number used as BUFGMUX | 0 |  |  |  | |
| Number of DCM/DCM\_CLKGENs | 0 | 4 | 0% |  | |
| Number of ILOGIC2/ISERDES2s | 0 | 248 | 0% |  | |
| Number of IODELAY2/IODRP2/IODRP2\_MCBs | 0 | 248 | 0% |  | |
| Number of OLOGIC2/OSERDES2s | 0 | 248 | 0% |  | |
| Number of BSCANs | 0 | 4 | 0% |  | |
| Number of BUFHs | 0 | 128 | 0% |  | |
| Number of BUFPLLs | 0 | 8 | 0% |  | |
| Number of BUFPLL\_MCBs | 0 | 4 | 0% |  | |
| Number of DSP48A1s | 0 | 32 | 0% |  | |
| Number of ICAPs | 0 | 1 | 0% |  | |
| Number of MCBs | 0 | 2 | 0% |  | |
| Number of PCILOGICSEs | 0 | 2 | 0% |  | |
| Number of PLL\_ADVs | 0 | 2 | 0% |  | |
| Number of PMVs | 0 | 1 | 0% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of SUSPEND\_SYNCs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 1.06 |  |  |  | |

**WAVEFORM**

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