**1 to 8 DEMUX**

**STRUCTURAL MODELLING:**

module and\_gate(output b,input c,d,e,f);

assign b = c & d & e & f;

endmodule

module demux1\_8(output y0,y1,y2,y3,y4,y5,y6,y7,input a,s0,s1,s2);

and\_gate l1(y0,a,~s0,~s1,~s2);

and\_gate l2(y1,a,~s0,~s1,s2);

and\_gate l3(y2,a,~s0,s1,~s2);

and\_gate l4(y3,a,~s0,s1,s2);

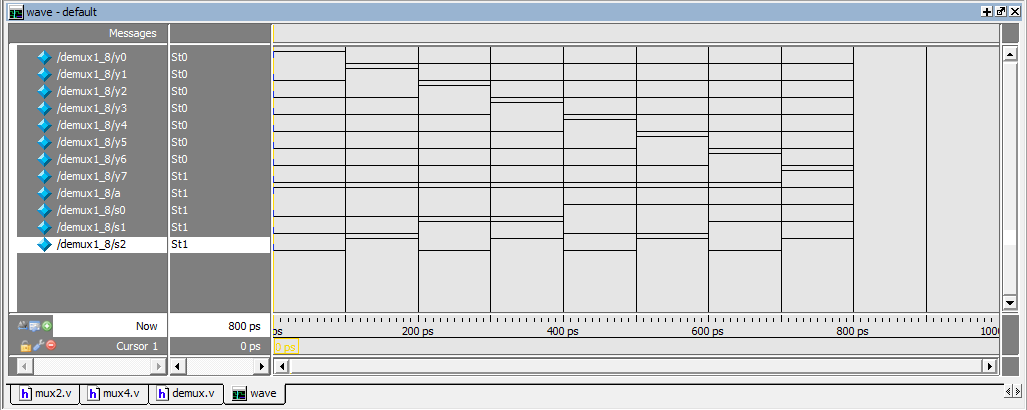
and\_gate l5(y4,a,s0,~s1,~s2);

and\_gate l6(y5,a,s0,~s1,s2);

and\_gate l7(y6,a,s0,s1,~s2);

and\_gate l8(y7,a,s0,s1,s2);

endmodule

**WAVEFORM:** 

**DESIGN SUMMARY:**

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| --- | --- | --- | --- |
| **demux1\_8 Project Status (02/12/2024 - 12:07:22)** | | | |
| **Project File:** | demux.xise | **Parser Errors:** | No Errors |
| **Module Name:** | demux1\_8 | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc6slx16-2ftg256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | No Warnings |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://21bec111/Implement/demux/demux1_8.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** |  |
| **Environment:** | [System Settings](D://21bec111/Implement/demux/demux1_8_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://21bec111/Implement/demux/demux1_8.twx?&DataKey=XmlTimingReport) |

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| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Registers | 0 | 18,224 | 0% |  | |
| Number of Slice LUTs | 4 | 9,112 | 1% |  | |
| Number used as logic | 4 | 9,112 | 1% |  | |
| Number using O6 output only | 0 |  |  |  | |
| Number using O5 output only | 0 |  |  |  | |
| Number using O5 and O6 | 4 |  |  |  | |
| Number used as ROM | 0 |  |  |  | |
| Number used as Memory | 0 | 2,176 | 0% |  | |
| Number of occupied Slices | 4 | 2,278 | 1% |  | |
| Number of MUXCYs used | 0 | 4,556 | 0% |  | |
| Number of LUT Flip Flop pairs used | 4 |  |  |  | |
| Number with an unused Flip Flop | 4 | 4 | 100% |  | |
| Number with an unused LUT | 0 | 4 | 0% |  | |
| Number of fully used LUT-FF pairs | 0 | 4 | 0% |  | |
| Number of slice register sites lost         to control set restrictions | 0 | 18,224 | 0% |  | |
| Number of bonded [IOBs](D://21bec111/Implement/demux/demux1_8_map.xrpt?&DataKey=IOBProperties) | 12 | 186 | 6% |  | |
| Number of LOCed IOBs | 12 | 12 | 100% |  | |
| Number of RAMB16BWERs | 0 | 32 | 0% |  | |
| Number of RAMB8BWERs | 0 | 64 | 0% |  | |
| Number of BUFIO2/BUFIO2\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFIO2FB/BUFIO2FB\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFG/BUFGMUXs | 0 | 16 | 0% |  | |
| Number of DCM/DCM\_CLKGENs | 0 | 4 | 0% |  | |
| Number of ILOGIC2/ISERDES2s | 0 | 248 | 0% |  | |
| Number of IODELAY2/IODRP2/IODRP2\_MCBs | 0 | 248 | 0% |  | |
| Number of OLOGIC2/OSERDES2s | 0 | 248 | 0% |  | |
| Number of BSCANs | 0 | 4 | 0% |  | |
| Number of BUFHs | 0 | 128 | 0% |  | |
| Number of BUFPLLs | 0 | 8 | 0% |  | |
| Number of BUFPLL\_MCBs | 0 | 4 | 0% |  | |
| Number of DSP48A1s | 0 | 32 | 0% |  | |
| Number of ICAPs | 0 | 1 | 0% |  | |
| Number of MCBs | 0 | 2 | 0% |  | |
| Number of PCILOGICSEs | 0 | 2 | 0% |  | |
| Number of PLL\_ADVs | 0 | 2 | 0% |  | |
| Number of PMVs | 0 | 1 | 0% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of SUSPEND\_SYNCs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 2.00 |  |  |  | |

**BOOTH MULTIPLER**

module Booth\_Multiplier(PRO, A, B);

output reg signed [7:0] PRO;

input signed [3:0] A, B;

reg [1:0] temp;

integer i;

reg e;

reg [3:0] B1;

always @(A,B)

begin

PRO = 8'd0;

e = 1'b0;

B1 = -B;

for (i=0; i<4; i=i+1)

begin

temp = { A[i], e };

case(temp)

2'd2 : PRO[7:4] = PRO[7:4] + B1;

2'd1 : PRO[7:4] = PRO[7:4] + B;

endcase

PRO = PRO >> 1;

PRO[7] = PRO[6];

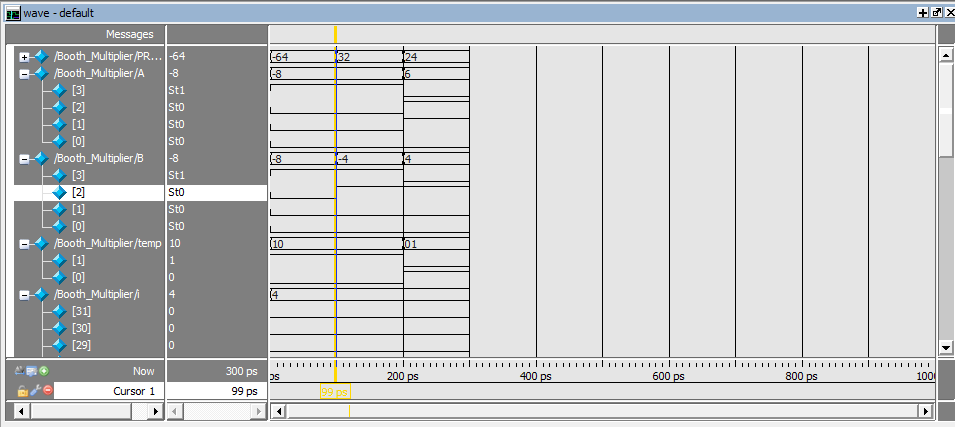
e=A[i];

end

end

endmodule

**WAVEFORM:**

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**Design Summary:**

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| --- | --- | --- | --- |
| **Booth\_Multiplier Project Status (02/26/2024 - 11:44:30)** | | | |
| **Project File:** | booth.xise | **Parser Errors:** | No Errors |
| **Module Name:** | Booth\_Multiplier | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc6slx16-2ftg256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | No Warnings |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://21bec111/Implement/booth/Booth_Multiplier.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** |  |
| **Environment:** | [System Settings](D://21bec111/Implement/booth/Booth_Multiplier_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://21bec111/Implement/booth/Booth_Multiplier.twx?&DataKey=XmlTimingReport) |

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| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Registers | 0 | 18,224 | 0% |  | |
| Number of Slice LUTs | 25 | 9,112 | 1% |  | |
| Number used as logic | 25 | 9,112 | 1% |  | |
| Number using O6 output only | 19 |  |  |  | |
| Number using O5 output only | 0 |  |  |  | |
| Number using O5 and O6 | 6 |  |  |  | |
| Number used as ROM | 0 |  |  |  | |
| Number used as Memory | 0 | 2,176 | 0% |  | |
| Number of occupied Slices | 11 | 2,278 | 1% |  | |
| Number of MUXCYs used | 0 | 4,556 | 0% |  | |
| Number of LUT Flip Flop pairs used | 25 |  |  |  | |
| Number with an unused Flip Flop | 25 | 25 | 100% |  | |
| Number with an unused LUT | 0 | 25 | 0% |  | |
| Number of fully used LUT-FF pairs | 0 | 25 | 0% |  | |
| Number of slice register sites lost         to control set restrictions | 0 | 18,224 | 0% |  | |
| Number of bonded [IOBs](D://21bec111/Implement/booth/Booth_Multiplier_map.xrpt?&DataKey=IOBProperties) | 16 | 186 | 8% |  | |
| Number of LOCed IOBs | 16 | 16 | 100% |  | |
| Number of RAMB16BWERs | 0 | 32 | 0% |  | |
| Number of RAMB8BWERs | 0 | 64 | 0% |  | |
| Number of BUFIO2/BUFIO2\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFIO2FB/BUFIO2FB\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFG/BUFGMUXs | 0 | 16 | 0% |  | |
| Number of DCM/DCM\_CLKGENs | 0 | 4 | 0% |  | |
| Number of ILOGIC2/ISERDES2s | 0 | 248 | 0% |  | |
| Number of IODELAY2/IODRP2/IODRP2\_MCBs | 0 | 248 | 0% |  | |
| Number of OLOGIC2/OSERDES2s | 0 | 248 | 0% |  | |
| Number of BSCANs | 0 | 4 | 0% |  | |
| Number of BUFHs | 0 | 128 | 0% |  | |
| Number of BUFPLLs | 0 | 8 | 0% |  | |
| Number of BUFPLL\_MCBs | 0 | 4 | 0% |  | |
| Number of DSP48A1s | 0 | 32 | 0% |  | |
| Number of ICAPs | 0 | 1 | 0% |  | |
| Number of MCBs | 0 | 2 | 0% |  | |
| Number of PCILOGICSEs | 0 | 2 | 0% |  | |
| Number of PLL\_ADVs | 0 | 2 | 0% |  | |
| Number of PMVs | 0 | 1 | 0% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of SUSPEND\_SYNCs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 3.83 |  |  |  | |