**4x1 MUX**

**DATA FLOW MODELLING:**

module multi2(y,s0,s1,i0,i1,i2,i3);

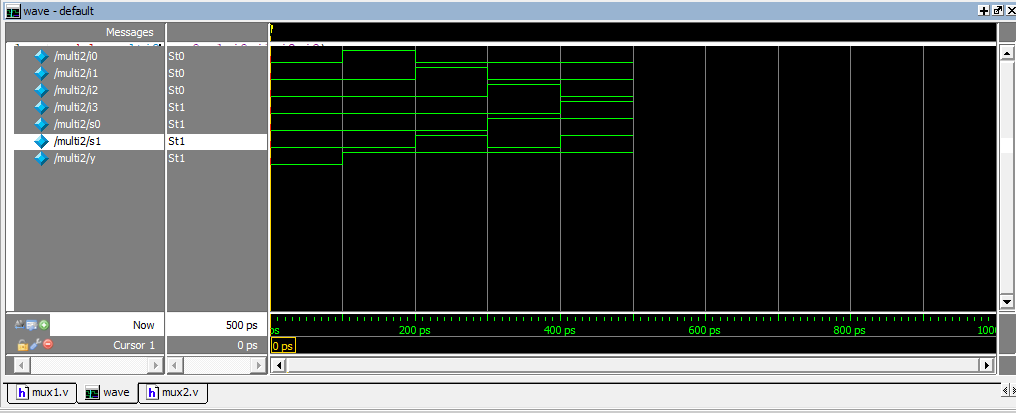
input i0,i1,i2,i3,s0,s1;

output y;

assign y=((~s0)&(~s1)&i0)|((~s0)&(s1)&i1)|((s0)&(~s1)&i2)|(s0&s1&i3);

endmodule

**WAVEFORM:**

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**DESIGN SUMMARY:**

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| --- | --- | --- | --- |
| **multi2 Project Status (02/05/2024 - 11:50:48)** | | | |
| **Project File:** | mux2.xise | **Parser Errors:** | No Errors |
| **Module Name:** | multi2 | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc6slx16-2ftg256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | No Warnings |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://21bec111/Implement/mux2/multi2.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** |  |
| **Environment:** | [System Settings](D://21bec111/Implement/mux2/multi2_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://21bec111/Implement/mux2/multi2.twx?&DataKey=XmlTimingReport) |

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| --- | --- | --- | --- | --- | --- |
| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Registers | 0 | 18,224 | 0% |  | |
| Number of Slice LUTs | 1 | 9,112 | 1% |  | |
| Number used as logic | 1 | 9,112 | 1% |  | |
| Number using O6 output only | 1 |  |  |  | |
| Number using O5 output only | 0 |  |  |  | |
| Number using O5 and O6 | 0 |  |  |  | |
| Number used as ROM | 0 |  |  |  | |
| Number used as Memory | 0 | 2,176 | 0% |  | |
| Number of occupied Slices | 1 | 2,278 | 1% |  | |
| Number of MUXCYs used | 0 | 4,556 | 0% |  | |
| Number of LUT Flip Flop pairs used | 1 |  |  |  | |
| Number with an unused Flip Flop | 1 | 1 | 100% |  | |
| Number with an unused LUT | 0 | 1 | 0% |  | |
| Number of fully used LUT-FF pairs | 0 | 1 | 0% |  | |
| Number of slice register sites lost         to control set restrictions | 0 | 18,224 | 0% |  | |
| Number of bonded [IOBs](D://21bec111/Implement/mux2/multi2_map.xrpt?&DataKey=IOBProperties) | 7 | 186 | 3% |  | |
| Number of LOCed IOBs | 7 | 7 | 100% |  | |
| Number of RAMB16BWERs | 0 | 32 | 0% |  | |
| Number of RAMB8BWERs | 0 | 64 | 0% |  | |
| Number of BUFIO2/BUFIO2\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFIO2FB/BUFIO2FB\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFG/BUFGMUXs | 0 | 16 | 0% |  | |
| Number of DCM/DCM\_CLKGENs | 0 | 4 | 0% |  | |
| Number of ILOGIC2/ISERDES2s | 0 | 248 | 0% |  | |
| Number of IODELAY2/IODRP2/IODRP2\_MCBs | 0 | 248 | 0% |  | |
| Number of OLOGIC2/OSERDES2s | 0 | 248 | 0% |  | |
| Number of BSCANs | 0 | 4 | 0% |  | |
| Number of BUFHs | 0 | 128 | 0% |  | |
| Number of BUFPLLs | 0 | 8 | 0% |  | |
| Number of BUFPLL\_MCBs | 0 | 4 | 0% |  | |
| Number of DSP48A1s | 0 | 32 | 0% |  | |
| Number of ICAPs | 0 | 1 | 0% |  | |
| Number of MCBs | 0 | 2 | 0% |  | |
| Number of PCILOGICSEs | 0 | 2 | 0% |  | |
| Number of PLL\_ADVs | 0 | 2 | 0% |  | |
| Number of PMVs | 0 | 1 | 0% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of SUSPEND\_SYNCs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 1.00 |  |  |  | |

**STRUCTURAL MODELLING:**

module and\_gate(output a, input b, c, d);

assign a = b & c & d;

endmodule

module not\_gate(output f, input e);

assign f = ~ e;

endmodule

module or\_gate(output l, input m, n, o, p);

assign l = m | n | o | p;

endmodule

module m41(out, a, b, c, d, s0, s1);

output out;

input a, b, c, d, s0, s1;

wire s0bar, s1bar, T1, T2, T3;

not\_gate u1(s1bar, s1);

not\_gate u2(s0bar, s0);

and\_gate u3(T1, a, s0bar, s1bar);

and\_gate u4(T2, b, s0, s1bar);

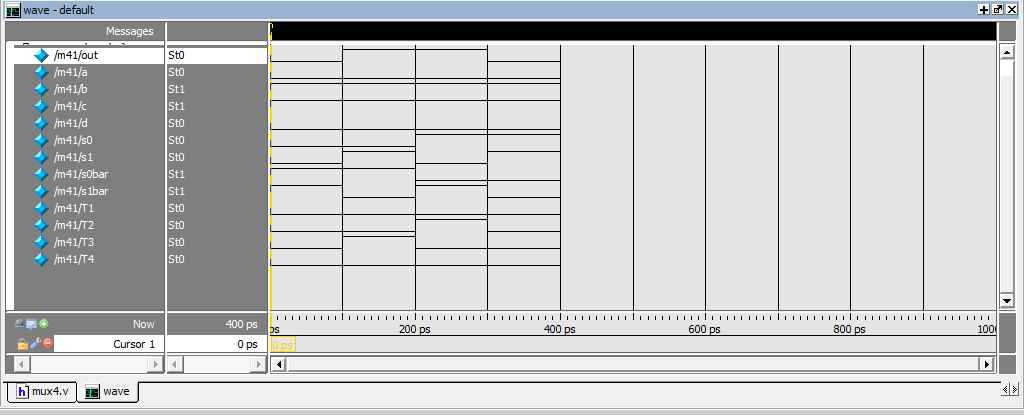
and\_gate u5(T3, c, s0bar, s1);

and\_gate u6(T4, d, s0, s1);

or\_gate u7(out, T1, T2, T3, T4);

endmodule

WAVEFORM:



**DESIGN SUMMARY:**

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| --- | --- | --- | --- |
| **m41 Project Status (02/12/2024 - 10:40:51)** | | | |
| **Project File:** | mux4.xise | **Parser Errors:** | No Errors |
| **Module Name:** | m41 | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc6slx16-2ftg256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | No Warnings |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://21bec111/Implement/mux4/m41.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** |  |
| **Environment:** | [System Settings](D://21bec111/Implement/mux4/m41_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://21bec111/Implement/mux4/m41.twx?&DataKey=XmlTimingReport) |

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| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
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| Number of Slice LUTs | 1 | 9,112 | 1% |  | |
| Number used as logic | 1 | 9,112 | 1% |  | |
| Number using O6 output only | 1 |  |  |  | |
| Number using O5 output only | 0 |  |  |  | |
| Number using O5 and O6 | 0 |  |  |  | |
| Number used as ROM | 0 |  |  |  | |
| Number used as Memory | 0 | 2,176 | 0% |  | |
| Number of occupied Slices | 1 | 2,278 | 1% |  | |
| Number of MUXCYs used | 0 | 4,556 | 0% |  | |
| Number of LUT Flip Flop pairs used | 1 |  |  |  | |
| Number with an unused Flip Flop | 1 | 1 | 100% |  | |
| Number with an unused LUT | 0 | 1 | 0% |  | |
| Number of fully used LUT-FF pairs | 0 | 1 | 0% |  | |
| Number of slice register sites lost         to control set restrictions | 0 | 18,224 | 0% |  | |
| Number of bonded [IOBs](D://21bec111/Implement/mux4/m41_map.xrpt?&DataKey=IOBProperties) | 7 | 186 | 3% |  | |
| Number of LOCed IOBs | 7 | 7 | 100% |  | |
| Number of RAMB16BWERs | 0 | 32 | 0% |  | |
| Number of RAMB8BWERs | 0 | 64 | 0% |  | |
| Number of BUFIO2/BUFIO2\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFIO2FB/BUFIO2FB\_2CLKs | 0 | 32 | 0% |  | |
| Number of BUFG/BUFGMUXs | 0 | 16 | 0% |  | |
| Number of DCM/DCM\_CLKGENs | 0 | 4 | 0% |  | |
| Number of ILOGIC2/ISERDES2s | 0 | 248 | 0% |  | |
| Number of IODELAY2/IODRP2/IODRP2\_MCBs | 0 | 248 | 0% |  | |
| Number of OLOGIC2/OSERDES2s | 0 | 248 | 0% |  | |
| Number of BSCANs | 0 | 4 | 0% |  | |
| Number of BUFHs | 0 | 128 | 0% |  | |
| Number of BUFPLLs | 0 | 8 | 0% |  | |
| Number of BUFPLL\_MCBs | 0 | 4 | 0% |  | |
| Number of DSP48A1s | 0 | 32 | 0% |  | |
| Number of ICAPs | 0 | 1 | 0% |  | |
| Number of MCBs | 0 | 2 | 0% |  | |
| Number of PCILOGICSEs | 0 | 2 | 0% |  | |
| Number of PLL\_ADVs | 0 | 2 | 0% |  | |
| Number of PMVs | 0 | 1 | 0% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of SUSPEND\_SYNCs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 1.00 |  |  |  | |

**2 Bit comparator**

module comp(a,b,eq,lt,gt);

input [1:0]a,b;

output eq,lt,gt;

reg eq,lt,gt;

initial eq=0;

initial lt=0;

initial gt=0;

always @(a,b)

begin

if(a < b)

begin

gt=0;

lt=1;

eq=0;

end

if(a == b)

begin

gt=0;

lt=0;

eq=1;

end

else

begin

gt=1;

lt=0;

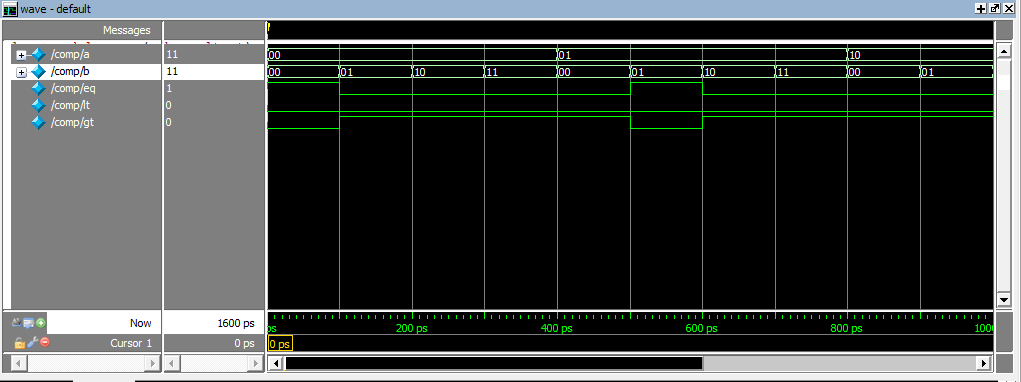
eq=0;

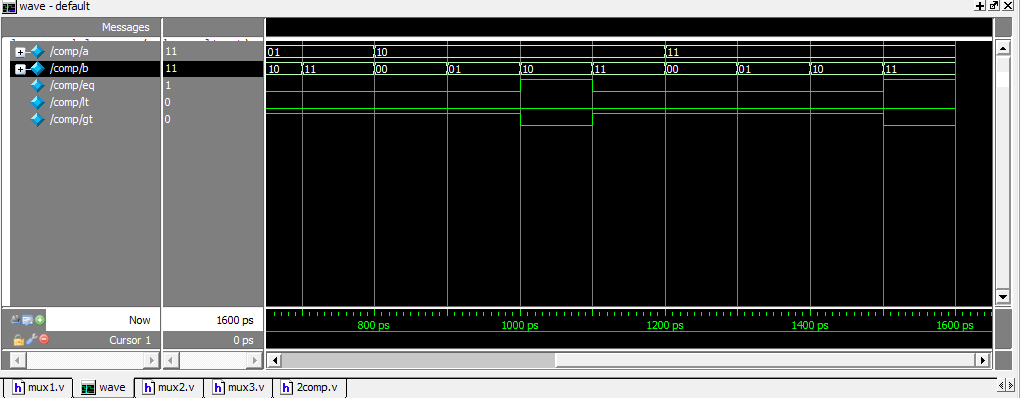
end

end

endmodule

**Wave form:**

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**Design summary:**

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| --- | --- | --- | --- |
| **comp Project Status** | | | |
| **Project File:** | comp.xise | **Parser Errors:** | No Errors |
| **Module Name:** | comp | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc6slx16-2ftg256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | No Warnings |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://21bec111/Implement/comp/comp.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** |  |
| **Environment:** | [System Settings](D://21bec111/Implement/comp/comp_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://21bec111/Implement/comp/comp.twx?&DataKey=XmlTimingReport) |

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| Number used as Memory | 0 | 2,176 | 0% |  | |
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| Number of BUFHs | 0 | 128 | 0% |  | |
| Number of BUFPLLs | 0 | 8 | 0% |  | |
| Number of BUFPLL\_MCBs | 0 | 4 | 0% |  | |
| Number of DSP48A1s | 0 | 32 | 0% |  | |
| Number of ICAPs | 0 | 1 | 0% |  | |
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| Number of PCILOGICSEs | 0 | 2 | 0% |  | |
| Number of PLL\_ADVs | 0 | 2 | 0% |  | |
| Number of PMVs | 0 | 1 | 0% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of SUSPEND\_SYNCs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 1.00 |  |  |  | |