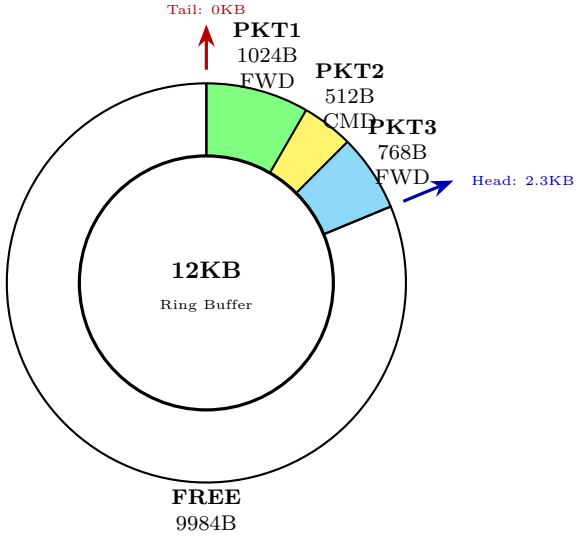
Circular Buffer Architecture - Packet Flow Timeline

12KB Ring Buffer with Strict FIFO Order

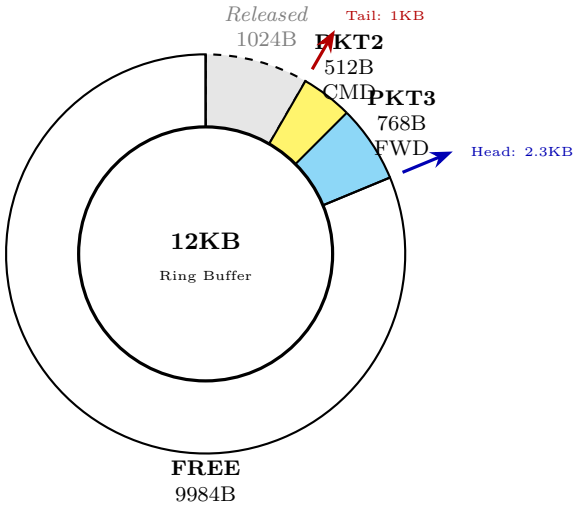
T=0ms: Initial State

3 packets in buffer, PKT1 being forwarded



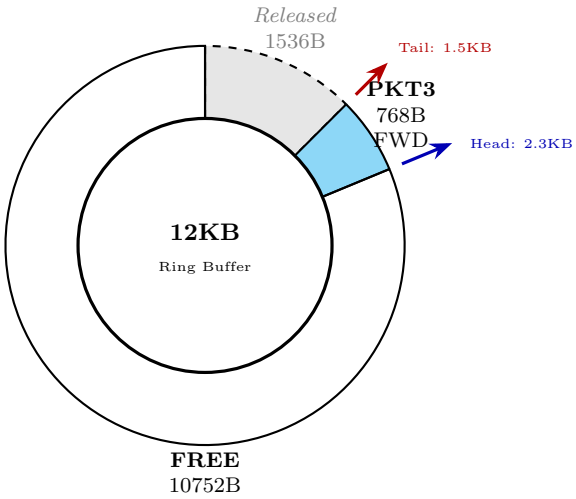
T=2.3ms: PKT1 Released

Tail advances to 1KB, PKT2 processing starts



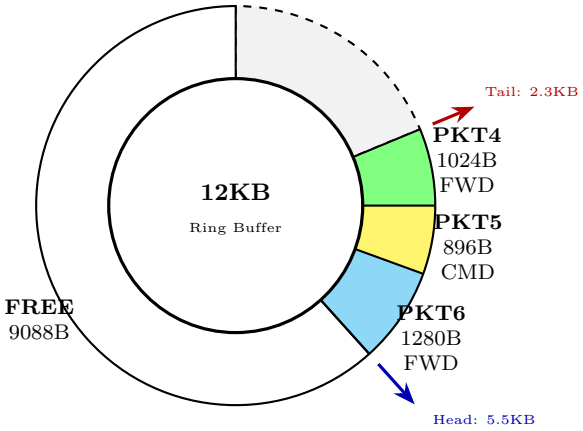
T=2.5ms: PKT2 Released

Tail advances to 1.5KB, PKT3 forwarding starts



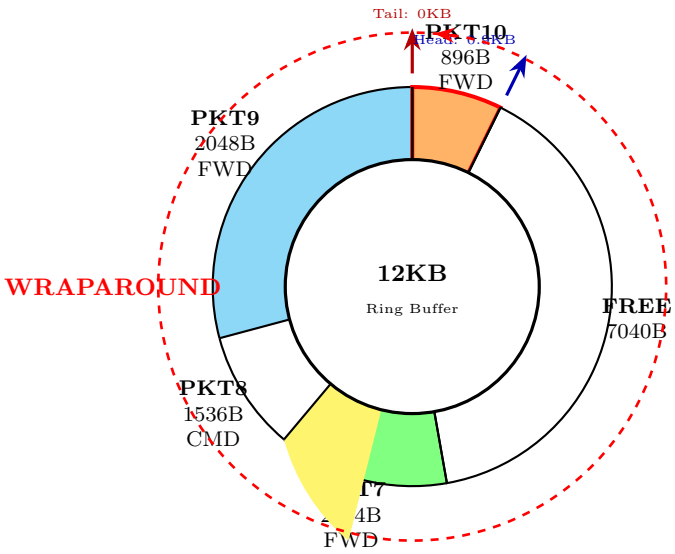
T=5ms: New Packets

PKT4, PKT5, PKT6 arrive after PKT3 released



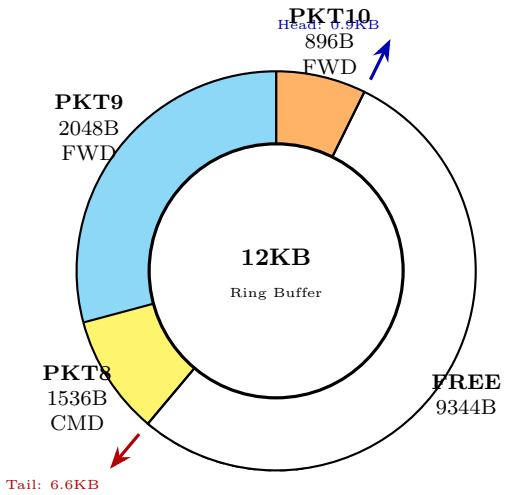
Wraparound Scenario

Buffer nearly full, packets contiguous, PKT10 wraps to start



After Wraparound

PKT7 released, tail advances, packets remain contiguous



Key Observations:

- **Strict FIFO Order**: Packets always released in arrival order (Tail advances sequentially)
- **Zero External Fragmentation**: Packets allocated contiguously with NO gaps between packets
- **Contiguous Allocation**: All packets stored contiguously; FREE space exists only in continuous region between head and tail
- **Wraparound Handling**: When insufficient space at buffer end, allocation wraps to start (shown in orange)
- **Pointer Movement**: Tail follows head clockwise around ring as packets are processed and released
- **Dynamic Capacity**: Buffer holds 10-12 variable-sized packets (avg 958B) vs theoretical 12.5 with perfect packing

Packet Type Color Coding: Green = Forward packets (FWD) - Zero-copy forwarded to next UART Yellow = Command packets (CMD) - Copied to CMD_Pool for processing Cyan = Forward packets (alternate) Orange = Wraparound packet (special handling)