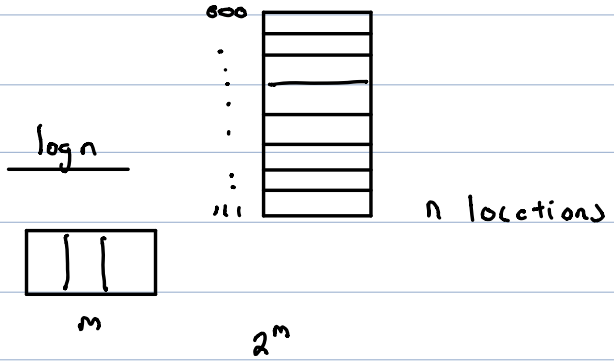


ε TLB Search

1 μs memory access

α : TLB hit ratio

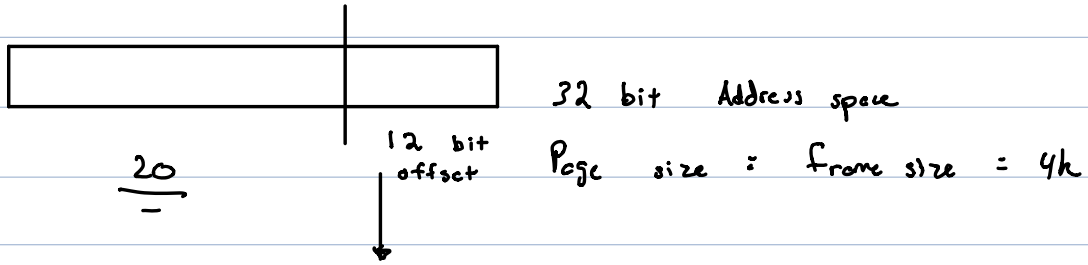
If it's a hit

effective access time

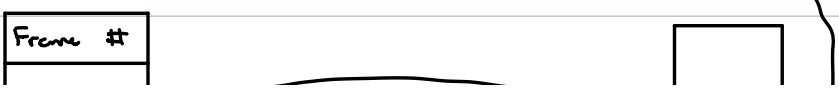
$$\alpha[\varepsilon + 1] + [1 - \alpha](\varepsilon + 2)$$

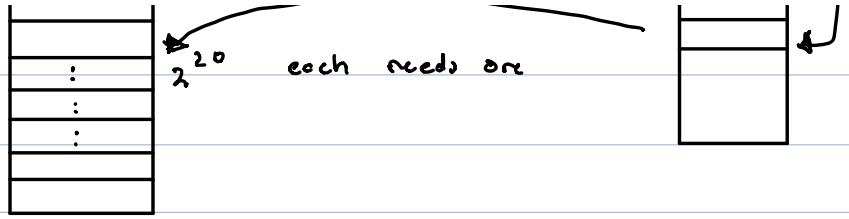
$$= \varepsilon - a + 2$$

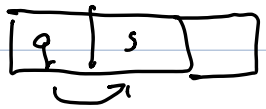
Two-level Paging Example



Hence







q is mapped into page s

- TLB Entry will have a process ID / shared

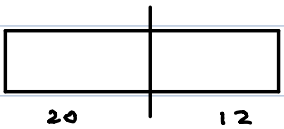
↑ Process has it's own hash table

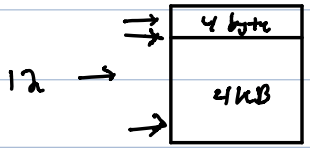
---

32 bit address space

4kB

↓ Logical Address



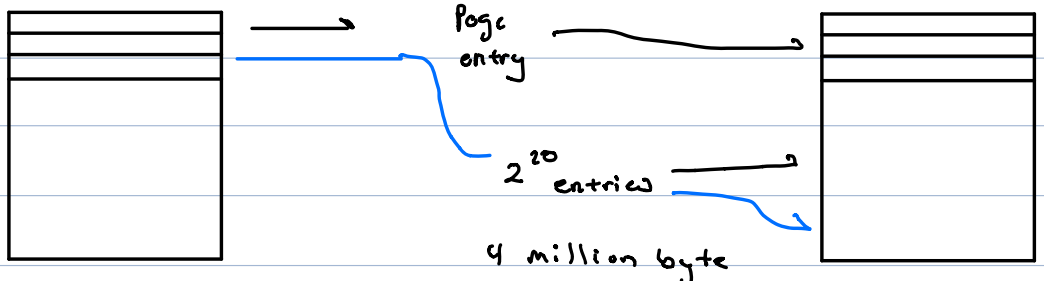


Outer from 2^{20}

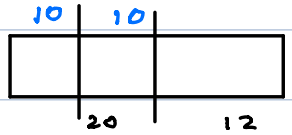
Page entry

2^{20} entries

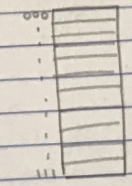
4 million byte



$2^{12} = 4k$



Main Memory



logn addresses

n locations

ε ← time

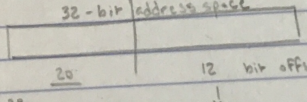
TLB search; Effective access time

1 μs memory access

α ; TLB hit ratio

= α[ε+1] + (1-α)[ε+2]

Page size = frame size = 4K

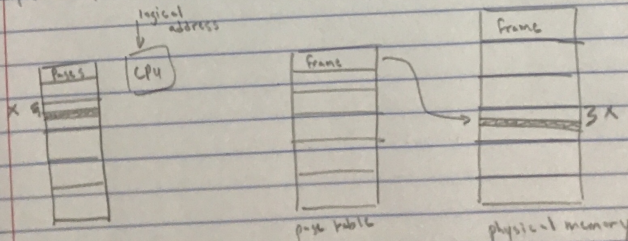


2^{20} in page table

2^{12} = 4K

Frame = physical memory

page = process memory



X = some offset