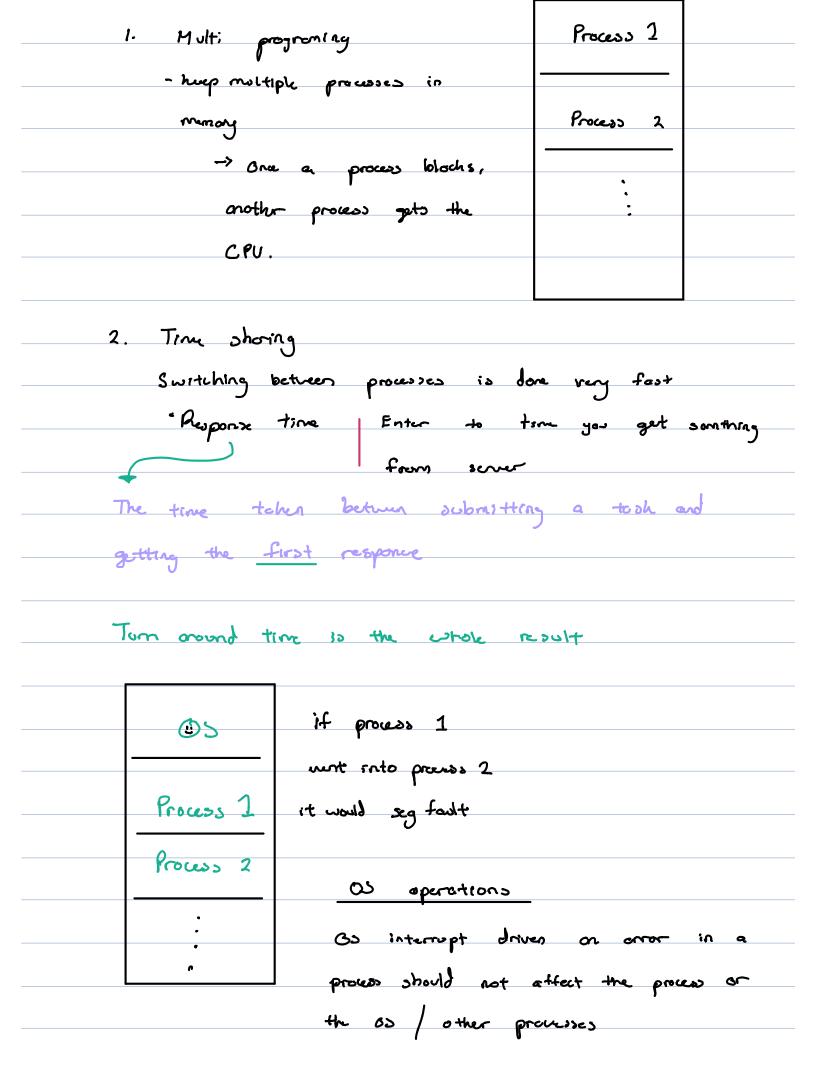
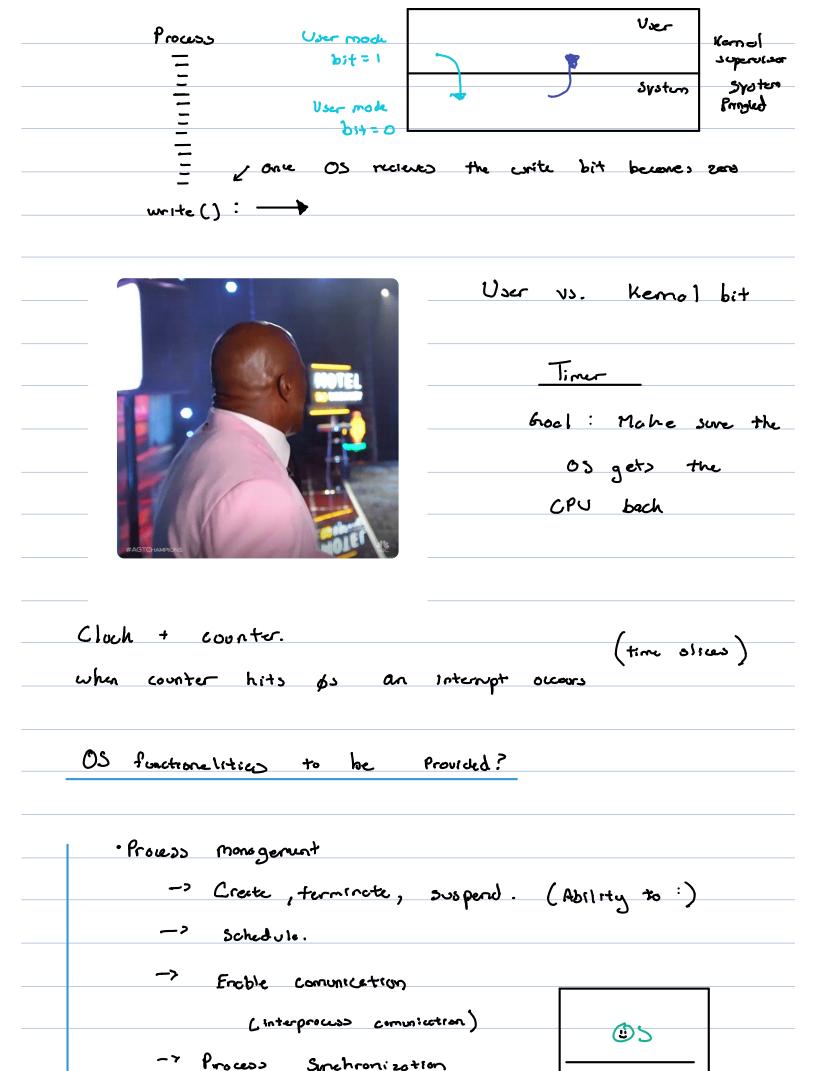
- 03	· Interrupt s	· Organiz	otion
Computer syst	en architecture		
1. Single	Processor System		
->	4 single CPU execu	tes general	purpose instruction
	- Other processor's h	elp the CP	V
7 M. J. S.			
•	cessor System	CPUI	CPUZ CP
	Two or more CPUs	reg	reg reg
	shoring bus, memory		
	?	Γ	Memory
·	. Increased Throughput	_ -	
	· Speedup would		then (n)
	due to there be		
	Regoing the cornec		
	1. More reliable		
	· System still 4	runctions wer	if some
	proussors fail		

- Asymetric	as Sumator	
	₽	
not peers	p eers	
Multi core		
Processors are on	CPU1 CPU2	
the some Chip	reg reg	
23.0 1.11	cache	
	Cab	
why?	Cache	
· Faster Comunication		
· less power		
· less space		
System System		
103(820 2/0.41)		
· Individual System Connected	through a fast local a	
nutura (LAN)		
- High performance com	puting clusters	
- parfor (MATLAB)		
each thing	; will have different in	
•		
	em (different CPU)	
· Fach long	on different CPU	
24011 199		

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Shoved memory	Process I	
Message Passing	frows 2	
	:	
· Menong monogenent	•	
-> Trach memory (Free + in use)		
-> List storage / memory locotrons		
belonging to each process.		
-> Allocating and deallocating	100	
-> Preced / Write	4 15	
Disk and unsuspend from	/ ,	
Dish	No.	10
Disk		
· Storege moreguent	7	
1. File system [Manging files/Din	uton w _	
2. No dures		
Monage devous through drivers		
Network, display, mrcc, cords	, printers	
~		
· Paur Moncgement		
· Protection + Security		3
User groups		
υ 1 [—]		

Around

200

SC.

	broken some	
· hoch is to find the		
right system coll va API	ones.	
0 ,	Security) Pemisorons	