			INPUT		
Instruction	Name	Format	i_inst[30]	i_inst[14:12]	i_inst[6:2]
DontCare			?	???	?????
Width			1	3	5
add	ADD	R	0	000	01100
sub	SUB	R	1	000	01100
xor	XOR	R	0	100	01100
or	OR	R	0	110	01100
and	AND	R	0	111	01100
sll	Shift Left Logical	R	0	001	01100
srl	Shift Right Logical	R	0	101	01100
sra	Shift Right Arith	R	1	101	01100
slt	Set Less Than	R	0	010	01100
sltu	Set Less Than Unsigned	R	0	011	01100
addi	ADD Immediate	I	*	000	00100
xori	XOR Immediate	I	*	100	00100
ori	OR Immediate	I	*	110	00100
andi	AND Immediate	I	*	111	00100
slli	Shift Left Logical Immediate	I	0	001	00100
srli	Shift Right Logical Immediate	I	0	101	00100
srai	Shift Right Arith Immediate	I	1	101	00100
slti	Set Less Than Immediate	I	*	010	00100
sltiu	Set Less Than Immediate Unsigned	I	*	011	00100
lb	Load Byte	I	*	000	00000
lh	Load Half	I	*	001	00000
lw	Load Word	I	*	010	00000
lbu	Load Byte Unsigned	I	*	100	00000
lhu	Load Half Unsigned	I	*	101	00000
sb	Store Byte	S	*	000	01000
sh	Store Half	S	*	001	01000
sw	Store Word	S	*	010	01000
beq	Branch ==	B	*	000	11000
bne	Branch !=	B	*	001	11000
blt	Branch <	B	*	100	11000
bge	Branch >=	B	*	101	11000
bltu	Branch < Unsigned	B	*	110	11000
bgeu	Branch >= Unsigned	B	*	111	11000
jal	Jump And Link	J	*	*	11011
jalr	Jump And Link Reg	I	*	000	11001
lui	Load Upper Immediate	U	*	*	01101
auipc	Add Upper Immediate to PC	U	*	*	00101

OUTPUT							
o_imm_sel	o_reg_wen	o_br_un	is_br	is_jp	o_b_sel	o_a_sel	o_alu_sel
IMM_I	0	0	0	0	B_REG	A_REG	ALU_ADD
IMMSEL_W	1	1	1	1	BSEL_W	ASEL_W	ALUSEL_W
*	1	*	0	0	B_REG	A_REG	ALU_ADD
*	1	*	0	0	B_REG	A_REG	ALU_SUB
*	1	*	0	0	B_REG	A_REG	ALU_XOR
*	1	*	0	0	B_REG	A_REG	ALU_OR
*	1	*	0	0	B_REG	A_REG	ALU_AND
*	1	*	0	0	B_REG	A_REG	ALU_SLL
*	1	*	0	0	B_REG	A_REG	ALU_SRL
*	1	*	0	0	B_REG	A_REG	ALU_SRA
*	1	*	0	0	B_REG	A_REG	ALU_SLT
*	1	*	0	0	B_REG	A_REG	ALU_SLTU
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_ADD
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_XOR
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_OR
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_AND
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_SLL
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_SRL
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_SRA
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_SLT
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_SLTU
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_ADD
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_ADD
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_ADD
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_ADD
IMM_I	1	*	0	0	B_IMM	A_REG	ALU_ADD
IMM_S	0	*	0	0	B_IMM	A_REG	ALU_ADD
IMM_S	0	*	0	0	B_IMM	A_REG	ALU_ADD
IMM_S	0	*	0	0	B_IMM	A_REG	ALU_ADD
IMM_B	0	*	1	0	B_IMM	A_PC	ALU_ADD
IMM_B	0	*	1	0	B_IMM	A_PC	ALU_ADD
IMM_B	0	0	1	0	B_IMM	A_PC	ALU_ADD
IMM_B	0	0	1	0	B_IMM	A_PC	ALU_ADD
IMM_B	0	1	1	0	B_IMM	A_PC	ALU_ADD
IMM_B	0	1	1	0	B_IMM	A_PC	ALU_ADD
IMM_J	1	*	0	1	B_IMM	A_PC	ALU_ADD
IMM_I	1	*	0	1	B_IMM	A_REG	ALU_ADD
IMM_U	1	*	0	0	B_IMM	A_ZERO	ALU_ADD
IMM_U	1	*	0	0	B_IMM	A_PC	ALU_ADD

o_st_mem	o_wb_sel
0	WB_ALU
1	WBSEL_W
0	WB_ALU
0	WB_ALU
0	WB_ALU
0	WB_ALU
0	WB_ALU
0	WB_ALU
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0	WB_ALU
0	WB_MEM
0	WB_MEM
0	WB_MEM
0	WB_MEM
0	WB_MEM
1	*
1	*
1	*
0	*
0	*
0	*
0	*
0	*
0	*
0	WB_PC
0	WB_PC
0	WB_ALU
0	WB_ALU