Pham Quoc Trung

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Profile

Third-year Electronics & Telecommunications Engineering student with hands-on experience in Analog IC Design and Digital Logic. Skilled in schematic design, circuit simulation, layout implementation, and LVS/DRC verification using Cadence Virtuoso and Siemens Tanner EDA. Passionate about VLSI design and seeking to contribute as an IC Design Intern while growing into a Design Engineer.

Education

VNUHCM - University of Science *Sep 2023 - Sep 2027*
Bachelor of Electronics & Telecommunications Engineering

- GPA: 3.668/4.0.

Skills

VLSI & EDA Tools:

- **Cadence Virtuoso (250nm technology):** Full analog IC design flow – schematic capture, simulation (DC, AC, transient), layout design, LVS & DRC verification.
- **Siemens EDA (250nm technology):** Hands-on experience with complete front-end and back-end flow, including layout implementation and verification (LVS, DRC).
- Intel Quartus Prime, ModelSim/Questa (digital design & simulation)
- LTspice, OrCAD (circuit simulation)

Programming & HDL:

- **Verilog HDL (basic):** Designed fundamental digital modules and developed a simple test bench for simulation.
- C, C++, Python (algorithm & embedded applications)

Software Tools:

- Git, Linux, Visual Studio Code

Projects

Analog IC Internship – University Lab

CMOS 2-Stage Operational Amplifier (250nm – Siemens Tanner EDA):

- Designed and simulated a 2-stage OpAmp at transistor level.
- Completed front-end (schematic design, DC/AC/transient analysis) and back-end (layout).
- Verified performance (gain, phase margin, power) and ensured manufacturability through LVS & DRC verification.

CMOS 4-bit Full Adder (250nm – Cadence Virtuoso):

- Implemented a 4-bit full adder using transistor-level CMOS (28T).
- Conducted schematic capture, functional verification, and layout design.
- Achieved LVS/DRC clean layout and validated design through post-layout simulation.

Experience

Analog IC Internship – University Lab 2025

- Designed and implemented CMOS 2-stage OpAmp and CMOS 4-bit Full Adder (28T, 250nm) from schematic to layout.

- Performed analog simulations (gain, bandwidth, slew rate, phase margin) and digital functional verification.
- Completed full back-end flow with layout design, post-layout simulation, and LVS/DRC verification using Siemens Tanner EDA and Cadence Virtuoso.

Programming Tutor – Robotics & IoT Club 2023 – 2025

- Tutored C/C++ programming for embedded systems (Arduino, STM32, Lego Spike).
- Guided students in robotics projects, focusing on FSM-based control and PID algorithms.

Activities

F-Race Competition 2024 – 2025

AI-based Human-Robot Interaction Project – Research Student 2024 – 2025

Robocus Competition – Robotics Coach 2024 – 2025

Backend Rookie Hackathon – Participant Oct 2023

Collaborator – AWS First Cloud Journey Training Program Sep – Nov 2024