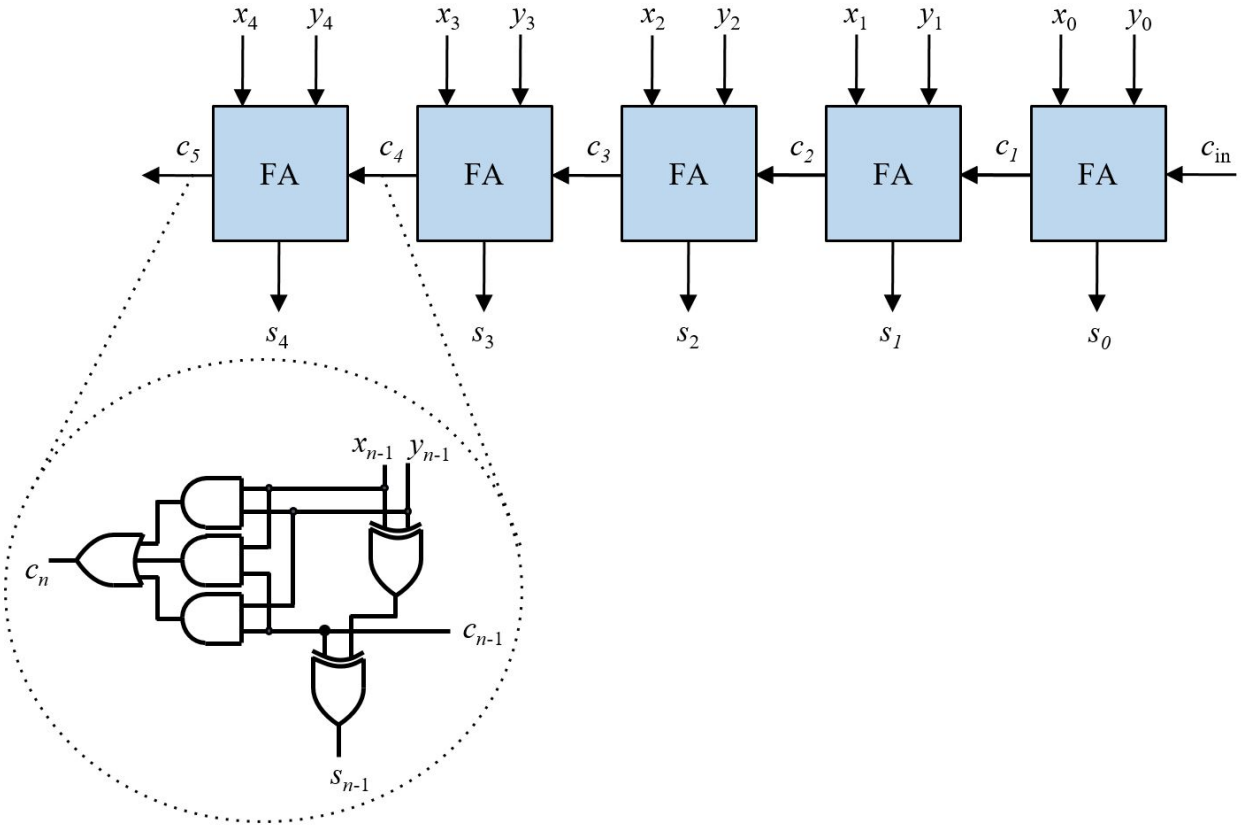
ECE 375
Computer Organization and Assembly Language Programming
Fall 2021
Homework #4

Problem #1 [18 pts]

Suppose that you want to build an ALU which performs addition using **5-bit** operands. For this homework you will utilize a Ripple Carry Adder as illustrated below. Assume that all digital input signals arrive simultaneously.



(a) [2 pts] How many OR gates will you need in order to implement the 5-bit RCA?

(b) [2 pts] How many AND gates will you need in order to implement the 5-bit RCA?

(c) [2 pts] How many exclusive-OR gates will you need in order to implement the 5-bit RCA?

(d) [3 pts] How many gate delays (abbreviated as "gds") are required in order for the RCA to compute the first sum bit (S_0)?

(e) [3 pts] How many gate delays (abbreviated as "gds") are required in order for the RCA to compute the second sum bit (S_1)?

(f) [3 pts] How many gate delays are required in order for the RCA to compute the output carry bit (C_5)?

(g) [3 pts] Imagine that you have insider knowledge regarding the value of Cin. For the application in question, you are informed that **Cin** will **always** have a value of 0. Armed with this information, how many logic gates would we be able to eliminate from the schematic? Hint: C_1 and S_0 will only depend on the value of X_0 and Y_0

Problem #2 [25 pts]
For each of the math problems below, indicate what values the AVR microcontroller will assign to each of the following flags:

- **C**arry flag
- o**V**erflow flag
- **N**egative flag
- **S**ign flag
- **Z**ero flag

Assume that the AVR is performing 8-bit arithmetic with the built-in instructions ADD and SUB. Note that each problem is independent from the others. Feel free to check your answers using the AVR simulator, but be sure that you understand how to determine the flags.

(a) $21 - 32$

(b) $93 + 112$

(c) $(-3) - (-100)$

(d) $(120) + (136)$

(e) $(-33) - 7$

Problem #3 [22 pts]
Please read section 120 of the AVR Instruction Set Manual and review operation of the `STD Z+q, Rr` instruction (an indirect store with displacement).

(a) List and explain the sequence of microoperations required to implement this instruction on the enhanced AVR datapath (Figure 8.26 in the textbook). Note that this instruction takes two execute cycles (EX1 and EX2).

(b) List and explain the control signals and the Register Address Logic (RAL) output for the `STD Z+q, Rr` instruction. Clearly explain your reasoning. Control signals for the Fetch cycle are given below.

Control Signals	IF	STD Z+q, Rr	
		EX1	EX2
MJ	0	X	X
MK	0	X	X
ML	0	X	X
IR_en	1	0	X
PC_en	1	0	0
PCh_en	0	0	0
PCl_en	0	0	0
NPC_en	1	X	X
SP_en	0	0	0
DEMUX	x	X	X
MA	x	X	X
MB	x	X	X
ALU_f	xxxx	xxxx	xxxx
MC	xx	xx	xx
RF_wA	0	0	0
RF_wB	0	0	0
MD	x	X	1
ME	x	X	1
DM_r	x	X	0
DM_w	0	0	1
MF	x	X	X
MG	x	1	X
Adder_f	xx	11	xx
Inc_Dec	x	X	X
MH	x	1	X
MI	x	X	X

RAL Output	STD Z+q, Rr	
	EX1	EX2
wA	X	X
wB	X	X
rA	ZH	X
rB	ZL	Rd