IC TRAINING CENTER VIET NAM
FUNDAMENTAL DESIGN AND VERIFICATION COURSE

FINAL PROJECT
FINAL REPORT

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Table 1 lists the project files and their locations within the ZIP archieve and on the ICTC server. The folders `rtl`, `tb` and `sim` are available in both the ZIP archieve and on the server.

Requirement	`Source`	**File Name/Path**
Design specification	ZIP	Design_Specification.pdf
RTL code	Server	/ictc/student_data/tramhoang/timer_advanced/rtl
	ZIP	`rtl` folder
Verification plan	ZIP	Verification_Plan.exe
Verification environment	Server	/ictc/student_data/tramhoang/timer_advanced/sim /ictc/student_data/tramhoang/timer_advanced/tb
	ZIP	`sim` folder `tb` folder
Testcases	Server	/ictc/student_data/tramhoang/timer_advanced/testcases
	ZIP	`testcases` folder

Table 1: Project checklist.

The images below provide evidence of all testcases passing and demonstrate 100% coverage in the verification report.

```
tramhoang@ictc-eda-ldap:~/timer_advanced/sim$ ./report.csh
init
rw
reserved
1hot
byte_access
cnt_ctrl
cnt
int
halt
apb
unaligned
|-------------------------------------------------------------------------------|
| PAT_NAME                    | RUN_DATE                  | RESULT           |
|-------------------------------------------------------------------------------|
| init                        | 03:01:37 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
| rw                          | 03:01:39 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
| reserved                    | 03:01:42 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
| 1hot                        | 03:01:43 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
| byte_access                 | 03:01:45 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
| cnt_ctrl                    | 03:01:47 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
| cnt                         | 03:01:49 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
| int                         | 03:01:51 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
| halt                        | 03:01:53 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
| apb                         | 03:01:55 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
| unaligned                   | 03:01:57 Oct 12 2025      | PASSED           |
|-------------------------------------------------------------------------------|
```

Figure 1: 100% testcases passed with checkers.

```
tramhoang@ictc-eda-ldap:~/timer_advanced/sim$ cat coverage/summary_report.txt
Coverage Report Summary Data by instance

================================================================================
=== Instance: /test_bench/dut/u_slave
=== Design Unit: work.apbif
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         8         8         0   100.00%
    Expressions                      6         6         0   100.00%
    Statements                       7         7         0   100.00%
    Toggles                          4         4         0   100.00%

================================================================================
=== Instance: /test_bench/dut/u_ctrl
=== Design Unit: work.cnt_ctrl
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         8         8         0   100.00%
    Expressions                      8         8         0   100.00%
    Statements                      13        13         0   100.00%
    Toggles                         56        56         0   100.00%

================================================================================
=== Instance: /test_bench/dut/u_cnt
=== Design Unit: work.counter
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        16        16         0   100.00%
    Statements                      10        10         0   100.00%
    Toggles                        384       384         0   100.00%

================================================================================
=== Instance: /test_bench/dut/u_reg
=== Design Unit: work.regset
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        45        45         0   100.00%
    Expressions                     61        61         0   100.00%
    Statements                      61        61         0   100.00%
    Toggles                        378       378         0   100.00%

================================================================================
=== Instance: /test_bench/dut
=== Design Unit: work.timer_top
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                        284       284         0   100.00%
```

Figure 2: Coverage report.