Time														100 ns					
clk=1				Ш							Ĺ								
rst=0																			
stall_signal[3:0]=0000	0000																		
addr[31:0]=00000024	xx+ (00000	000	χ0000	0004 (0	000000	8 (0000	000CX00	000010	000000	14 (0000	00018 (	000000	1C X000	00020	(0000	0024X	000000	28 X000	0000C
inst[31:0]=1423FFF9	00000000	X340100	003 <u>X</u> 3403	0003 \( 3	404000	5 XA041	0000 000	411020	304200	OF X0024	10018 (	800000	12 <b>X</b> 302	21000F	1423	FFF9X	080000	0A XA04	10000
id_srcLeft[31:0]=0000000F	00000000									(0000	00003		χ000	00000	(0000	000F		(000	00000
id_srcRight[31:0]=0000000F	00000000		(0000	0003		(0000	0005 (00	000003	3	(0000	000FX	000000	05 X000	00000	(0000	000FX	000000	03 (000	00000
o_dest[4:0]=01	00		X01	χ0	3	X04	χ00		(02		χ(	00	χ01			χ	00		
o_takeBranch=0																			
o_jpc[31:0]=00000000	00000000															X	000000	0C X000	00000
ex_dest[4:0]=01	xx (00			χ0	1	χ03	χ04		χ00	X02			χ00		<b>X</b> 01			χ00	
o_result[31:0]=0000000F	xx+ (00000	000		χ0	000000	3	χ00	000005	5 (030303	03 (0000	00003		X00C	00000	(0000	000F		(000	00000
we=0																			
i_hi[31:0]=00000000	xx+ (00000	000																	
i_lo[31:0]=00000000	xx+ (00000	000											X00C	0000F	(0000	0000			
<u> </u>	000																		
ramAddr[31:0]=00000000	00000000																		
ramSel[3:0]=0000	0000								χ0001	(0000									
writeEnable=1																			
writeAddr[4:0]=00	xx (00					χ01	χ03		χ04	X00	χ(	02			X00	X	01		
writeResult[31:0]=00000000	xx+ (00000	000				(0000	0003		000000	05 (0303	30303 X	000000	03		(0000	0000 X	000000	0F	
\ram[0][31:0]=00000003	00000000										χ(	000000	03						
\ram[1][31:0]=00000000	00000000																		
•	00000000																		
\ram[3][31:0]=00000000	00000000																		
\registers[1][31:0]=00000003	xx+ (00000	000					χ00	000003	3									0000	0000F
. •	xx+ (00000	000											X000	00003					
\registers[3][31:0]=00000003	xx+ (00000	000							χ000000	03									
\registers[4][31:0]=00000005	xx+ (00000	000								(0000	00005								

Time	100	0 ns															20	0 ns				
clk=1					ШГ															Ĺ		ШГ
rst=0																						
stall_signal[3:0]=0000	0000																					
addr[31:0]=00000024	0+\(0000	0020	0000002	<u>4 (0000</u>	0028 (0	000000	CX00000	010 (000	00014)	(00000)	018 X	000000	1CX000	00020	χ000	0002	4 <b>X</b> 0000	0028	(0000	000C	χ0000	0010 (0
inst[31:0]=1423FFF9	0+\(3021	000F	1423FFF	<u>9 (0800)</u>	000A XA	041000	0 (00411	020 \(304	2000F)	(00240	018 X	000008	12 \( 302	10001	₹X142	3FFF	9 (0800	000A	(A041	10000	X0041	1020 X3
id_srcLeft[31:0]=0000000F	0+\(0000	0000	0000000	F	χ0	000000	0 (00000	003	)	(00000)	012 X	000000	OF X000	00000	χ000	0004	в ХОООС	000B	(0000	0000	χ0000	0002
id_srcRight[31:0]=0000000F	0+\(0000	0000	0000000	FX0000	0003 \( 0	000000	0 (00000	00F			X	000000	05 (000	00000	) <u>(</u> 000	0000	F)(0000	0003	(0000	0000	χ0000	000B
o_dest[4:0]=01	00\(01			χ00				(02				00	X01				χ00					χ0:
o_takeBranch=0																						
o_jpc[31:0]=00000000	0000000	00		(0000	000CX0	000000	0										(0000	000C	(0000	0000		
ex_dest[4:0]=01	02\(00		01		χ0	0			)	02			(0.0)		χ01				(00			
o_result[31:0]=0000000F	0+\(0000	0000	0000000	F	χ0	000000	0	(OFO	FOFOF)	00000	012 X	000000	02\(000	00000	) X000	0004	BX0000	000B	(0000	0000		χ0:
we=0																						
i_hi[31:0]=0000000	0000000	00																				
i_lo[31:0]=00000000	0+\(0000	000F	0000000	10									(000	0004E	3 <u>X000</u>	0000	0					
loadop[2:0]=000	000																					
ramAddr[31:0]=00000000	0000000	00						χ000	100003)	(00000)	000											χ0
ramSel[3:0]=0000	0000							X100	0	0000												χ0.
writeEnable=1																						
writeAddr[4:0]=00	02		00	χ01			(00					02			χ00		X01				χ00	
writeResult[31:0]=00000000	0000000	)3 /	0000000	0000	000F		χ00000	000		OF0F01	FOF X	000000	12 (000	00002	2 <b>X</b> 000	0000	0 (0000	004B	(0000	)000B	χ0000	0000
\ram[0][31:0]=00000003	0000000	)3										0F0000	03									
\ram[1][31:0]=00000000	0000000	00																				
\ram[2][31:0]=00000000	0000000																					
\ram[3][31:0]=00000000	0000000	00																				
\registers[1][31:0]=00000003	0000000				χ0	000000	F												(0000	004B	χ0000	000B
	0+\(0000												(000	00012	2 <b>X</b> 000	0000	2					
\registers[3][31:0]=00000003	0000000	)3																				
\registers[4][31:0]=00000005	0000000	)5																				