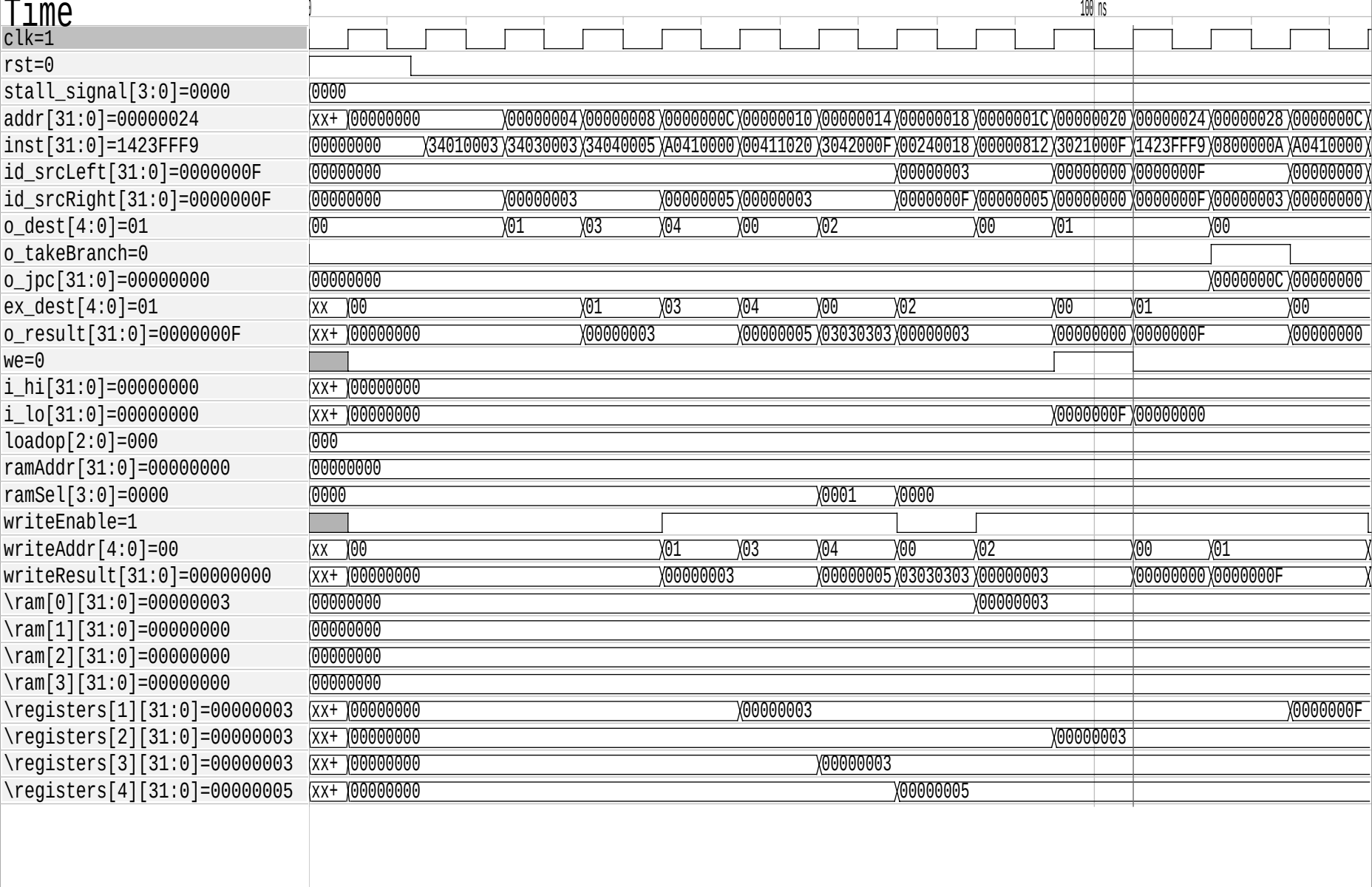
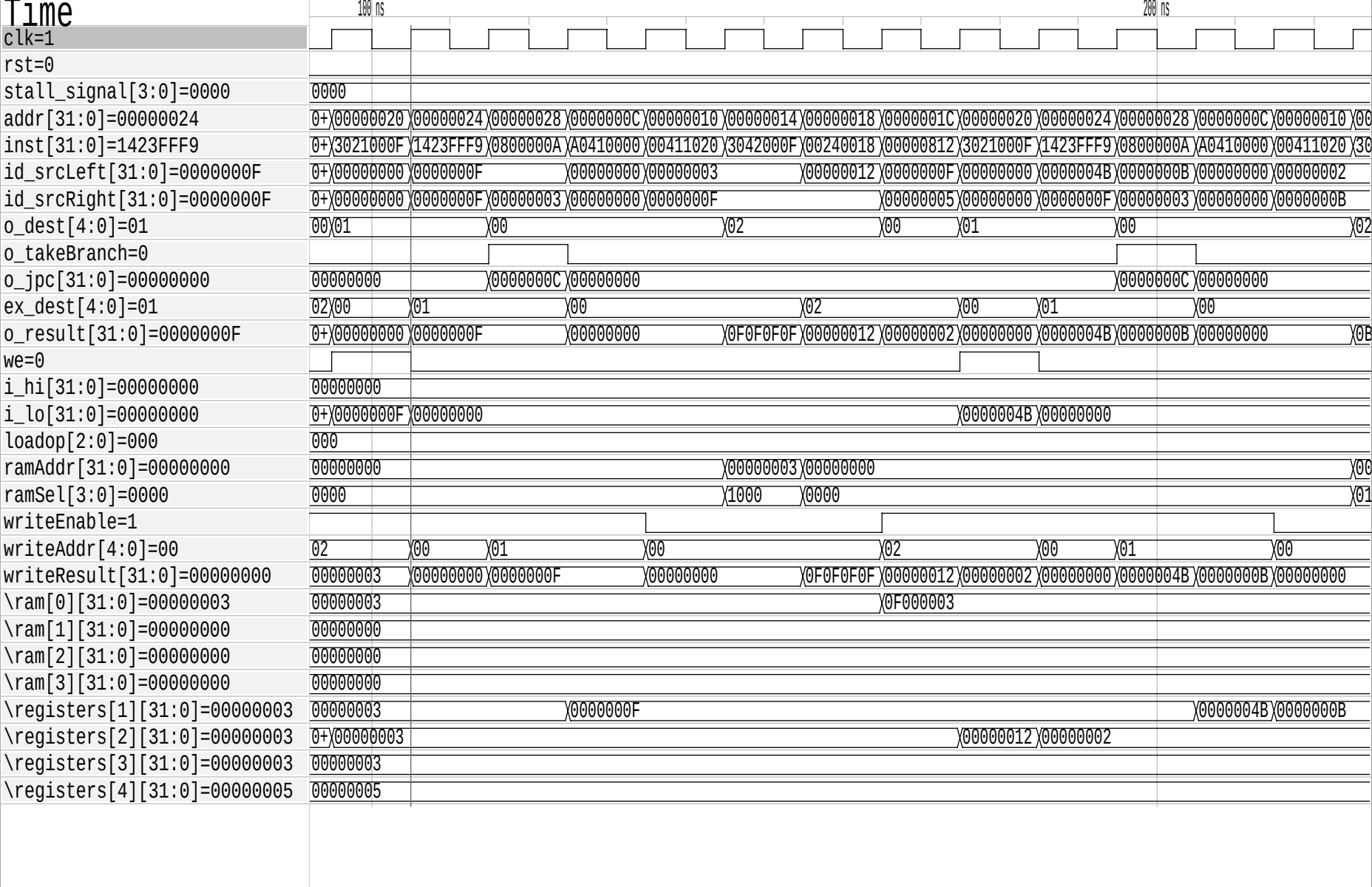

Time
100 ns
clk=1
rst=0
stall_signal[3:0]=0000
addr[31:0]=00000024
inst[31:0]=1423FFF9
id_srcLeft[31:0]=0000000F
id_srcRight[31:0]=0000000F
o_dest[4:0]=01
o_takeBranch=0
o_jpc[31:0]=00000000
ex_dest[4:0]=01
o_result[31:0]=0000000F
we=0
i_hi[31:0]=00000000
i_lo[31:0]=00000000
loadop[2:0]=000
ramAddr[31:0]=00000000
ramSel[3:0]=0000
writeEnable=1
writeAddr[4:0]=00
writeResult[31:0]=00000000
\ram[0][31:0]=00000003
\ram[1][31:0]=00000000
\ram[2][31:0]=00000000
\ram[3][31:0]=00000000
\registers[1][31:0]=00000003
\registers[2][31:0]=00000003
\registers[3][31:0]=00000003
\registers[4][31:0]=00000005


Time
100 ns
200 ns
clk=1
rst=0
stall_signal[3:0]=0000
addr[31:0]=00000024
inst[31:0]=1423FFF9
id_srcLeft[31:0]=0000000F
id_srcRight[31:0]=0000000F
o_dest[4:0]=01
o_takeBranch=0
o_jpc[31:0]=00000000
ex_dest[4:0]=01
o_result[31:0]=0000000F
we=0
i_hi[31:0]=00000000
i_lo[31:0]=00000000
loadop[2:0]=000
ramAddr[31:0]=00000000
ramSel[3:0]=0000
writeEnable=1
writeAddr[4:0]=00
writeResult[31:0]=00000000
\ram[0][31:0]=00000003
\ram[1][31:0]=00000000
\ram[2][31:0]=00000000
\ram[3][31:0]=00000000
\registers[1][31:0]=00000003
\registers[2][31:0]=00000003
\registers[3][31:0]=00000003
\registers[4][31:0]=00000005