Time														100	0 ns					
clk=0			i			ΠĹ			Ĺ			ШГ								
rst=0																				
stall_signal[3:0]=0000	0000																			
addr[31:0]=00000034	XX+ (	0000000	10	(000)	00004	000000	08 <u>(</u> 0000	000CX00	00001	0 (000000	14 (0000	0018 (0	000001	1C <b>X</b> 0000	0020	(0000	000CX0	000001	10 0000001	14)
inst[31:0]=3443FFFF	00000	0000	(00000)	320 <u>(</u> 2002	20004	000018	20 X8C24	0050 X20	21000	4 X006418	20 (2042	FFFF X1	440FFI	FBXAC23	0050	(8C24	0050 X2	2021000	04 \(0064182	20 Y
id_srcLeft[31:0]=00000002	00000	0000										χ0	00000	04 (0000	0003	(0000	0000 (0	000000	)4	$\equiv$
id_srcRight[31:0]=FFFFFFFF	00000	0000				<u> X000000</u>	04 (0000	0000		(000000	04 (0000	0000 XF	FFFFFI	FF X0000	0000				(000000)	J4)
o_dest[4:0]=02	00			X01		X02	χ03	χ04		X01	X03	χ0	2	X00			χC	)4	χ01	$\equiv$
o_takeBranch=0																				
o_jpc[31:0]=00000000	00000	0000												(0000	000C	(0000	0000			_
ex_dest[4:0]=00	XX (	00				X01	χ02	χ03		χ04	X01	χ0	3	X02		(00			X0 4	$\supseteq$
o_result[31:0]=00000000	XX+ (	0000000	10				(0000	0004\(00	00000	0	(0000	0004 (0	000000	00000	0003	(0000	0000			
we=0																				
i_hi[31:0]=00000000	XX+ (	0000000	10																	_
i_lo[31:0]=00000000	XX+ (	0000000	10																	_
loadop[2:0]=000	000									χ011	(000								X011	
ramAddr[31:0]=00000000	00000	0000								χ000000	50 (0000	0000							2000000	54)
	0000																			_
writeEnable=0																				
	xx (	00					X01	χ02		χ03	X04	χ0		χ03		X02		0		
		0000000	10					χ00	00000	4 X000000	00	χ0	000000	04 (0000	0000	(0000	0003 (0	000000	00	_
\ram[0][31:0]=00000000	00000	0000																		_
\ram[1][31:0]=00000000	00000	0000																		_
•	00000																			_
•	00000																			_
\registers[1][31:0]=00000010	XX+ (	0000000	10											0000	0004					_
		0000000								χ000000	04						χC	000000	03	_
\registers[3][31:0]=0000FFFF	XX+	0000000	10																	_
<pre>\registers[4][31:0]=FFFFFFF</pre>	XX+ (	0000000	10																	_

Time	100 n	S															200 ns				
clk=0			i [			$\neg$		T			ΙГ								i		
rst=0							_														
stall_signal[3:0]=0000	0000																				
addr[31:0]=00000034	0000	00+\(000	0000C)	(000000	10 (00	00000	14 (000	00018	(000000	1CX0000	0020 (0	00000	00CX0	000001	00000	0014 (000	00018	(000)	0001C	χ00000	020 (00000
inst[31:0]=3443FFFF	AC23	00+ X8C2	240050 X	202100	04 (00	064182	20 <u>X</u> 204	2FFFF	(1440FF	FBXAC23	0050 X8	3C240	050 X2	021000	14 (00641	.820 <u>(</u> 204	2FFFF	X144	OFFFB	XAC230	050 <u>(</u> 8C240
id_srcLeft[31:0]=00000002	0000	00+\(000	00000	(000000	04		χ000	00000	(000000	03 (0000)	0002 (0	00000	000 <u>X</u> 0	000000	18	χ000	00000	X000	00002	χ00000	001 (00000
id_srcRight[31:0]=FFFFFFFF	0000	0000			χος	00000	04 X000	00000	(FFFFFF	FF X0000	0000				(0000)	0004 (000	00000	(FFF)	FFFFF	00000	000
o_dest[4:0]=02	00			04	X01	1	χ03		(02	(00			χ0	4	X01	X03		X02		χ00	
o_takeBranch=0																					
o_jpc[31:0]=00000000	0000	00+\(000	00000							(0000	000C XC	00000	000							00000	00C <u>(</u> 00000
ex_dest[4:0]=00	02	χ00			χ04	4	χ01		(03	(02	χ	00			χ04	X01		<b>χ</b> 03		χ02	χ00
o_result[31:0]=00000000	0000	00+\(000	00000				χ000	80000	(000000	0000,000	0002 (0	0000	000			X000	00000	X000	00000	<u> X00000</u>	001 (00000
we=0																					
i_hi[31:0]=00000000	0000	0000																			
i_lo[31:0]=00000000	0000	0000																			
loadop[2:0]=000	000				χ01		χ000								X011	(000					
ramAddr[31:0]=00000000	0000	0000			χος	20000	54 <u>X000</u>	100000							(00000	0058 000	00000				
ramSel[3:0]=0000	0000																				
writeEnable=0																					
writeAddr[4:0]=00	03	χ02		00			χ04		X01	χ03		)2	χ0			χ04		X01		χ03	X02
writeResult[31:0]=00000000	0000	00+\(000	00003	(000000	000				(000000	08 (0000	0000 (0	00000	002 <u>X</u> 0	000000	0			X000	0000C	<u> X00000</u>	000 <u>X</u> 00000
\ram[0][31:0]=00000000	0000	0000																			
\ram[1][31:0]=00000000	0000	0000																			
\ram[2][31:0]=00000000	0000	0000																			
\ram[3][31:0]=00000000	0000	0000																			
\registers[1][31:0]=00000010	0000	0004								χ0000	8000									<u> X00000</u>	00C
\registers[2][31:0]=00000002	0000	0004		(000000	003								χ0	000000	12						
\registers[3][31:0]=0000FFFF	0000	0000																			
<pre>\registers[4][31:0]=FFFFFFF</pre>	0000	0000																			

Time				2	00 ns																3	00 ns
clk=0		ī																Ĺ				
rst=0																						
stall_signal[3:0]=0000	0000																					
addr[31:0]=00000034	000+ X00	<u> </u>	0000)	0014 (000	00018	00000	01C\(000	00020	(0000)	000CX(	000000	10 (000	00014)	(00000	018 XO	00000	01CX000	00002	20 \(000	0002	4 X000	00028
inst[31:0]=3443FFFF	8C2+ \(20	J210004	4 <u>X</u> 0064	1820 (204	2FFFF	X1440F	FFB\AC2	30050	(8C24)	0050 X2	2021000	04 (006	41820)	(2042F	FFF X1	L440F1	FFB (AC2	23005	0 X8C2	4005	(800 <b>)</b>	11822
id_srcLeft[31:0]=00000002	000+ X00	3000008	3	χ000	00000	00000	002 (000	00001	(0000)	0000)	000000	)C		(00000)	00 X	00000	001 (000	0000	000 <u>X</u> 000	0001	)	
id_srcRight[31:0]=FFFFFFFF	0000000	0	χ0000	0004 (000	00000	XFFFFF	FFF X000	00000				(000	00004)	(00000	000 XF	FFFF	FFF X000	0000	0			
o_dest[4:0]=02	00 X04	4	χ01	χ03		<b>χ</b> 02	χ00			χC	)4	χ01		(03	χ0	)2	χ00				X04	
o_takeBranch=0																						
o_jpc[31:0]=00000000	0000000	0					(000	0000C	(0000)	0000							χ000	0000	C X000	0000	)	
ex_dest[4:0]=00	00		X04	χ01		χ03	(02		(00			χ04		(01	χ0	)3	χ02		χ00			
o_result[31:0]=00000000	0000000	0		(000	000C	X00000	000,000	00001	(0000)	0000				(00000	010 XO	00000	000					
we=0																						
i_hi[31:0]=0000000	0000000	10																				
i_lo[31:0]=00000000	0000000	10																				
loadop[2:0]=000	000		X011	χ000								X011		(000								
ramAddr[31:0]=00000000	0000000	10	χ0000	0058 (000	0000							(000	0005C)	(00000	000						(000)	00060
ramSel[3:0]=0000	0000																				X111	1
writeEnable=0																						
writeAddr[4:0]=00	02 X00	)		χ04		χ01	X03		(02		00			(04	χ0	)1	χ03		χ02		X00	
writeResult[31:0]=00000000	000+ X00		)			00000	00CX000	00000	(0000)	0001 (0	000000	00			χ0	00000	010 (000	0000	0			
\ram[0][31:0]=00000000	0000000	10																				
\ram[1][31:0]=00000000	0000000	0																				
\ram[2][31:0]=00000000	0000000	0																				
\ram[3][31:0]=00000000	0000000	10																				
\registers[1][31:0]=00000010	0000000	18					(000	0000C									(000	00001	.0			
\registers[2][31:0]=00000002	000+ X00	<u> </u>	2							χ	000000	01									(000)	00000
\registers[3][31:0]=0000FFFF	0000000	10																				
<pre>\registers[4][31:0]=FFFFFFF</pre>	0000000	0																				

Time		800 ns												400 ns			
clk=0										Ĺ	ΠĹ				ΠĹ		Ĺ
rst=0																	
stall_signal[3:0]=0000	0000	(0011															
addr[31:0]=00000034	0000+ X000	00028 (0000	002C	(0000)	0000\(0000	0034 (00	00003	8 <b>X</b> 00000	003C X000	00040	<u> X000000</u>	44 (0000	00048 <u>X</u> 000	0004C	X00000	)50 <u>X</u> 00	00003
inst[31:0]=3443FFFF	8C24+ X008	11822 (2002	20003	X2042I	FFFF <b>X344</b> 3	BFFFF X20	04FFF	FX3085F	FFFF X00A	43025	X00A638	24 X1040	0001 X080	0000C	(2002F)	FF X20	42FFF
id_srcLeft[31:0]=00000002	00000010	(0000	0000		(0000	0003 (00	00000	2 X00000	)000 XFFF	FFFFF	(0000FF	FF	χ000	00002	(00000)	000	
<pre>id_srcRight[31:0]=FFFFFFFF</pre>	00000000	(0000	00010	(0000)	0003 XFFFI	FFFF X00	OOFFF	f XFFFFF	FFF X000	0FFFF	FFFFFF	FF	(000	00000			
o_dest[4:0]=02	00 \( \( \) \( \) \( \)	X03		X02		χ03		X04	χ05		X06	(07	χ00				
o_takeBranch=0																	
o_jpc[31:0]=00000000	00000000												χ000	00050	00000	)30 <u></u> X00	00000
ex_dest[4:0]=00	00	X04	χ00	χ03	χ02			χ03	χ04		χ05	X06	χ07		χ00		
o_result[31:0]=00000000	00000000			\FFFF1	FFF0 X0000	0003 (00	00000	2 X0000F	FFF XFFF	FFFFF	X0000FF	FF XFFFF	FFFF X000	0FFFF	00000	000	
we=0																	
i_hi[31:0]=0000000	00000000																
i_lo[31:0]=00000000	00000000																
loadop[2:0]=000	000	X011	(000														
ramAddr[31:0]=0000000	0000+ X000	00060	(0000	0000													
ramSel[3:0]=0000	0000 <u>X</u> 111	1 (0000															
writeEnable=0																	
writeAddr[4:0]=00	02 \( \( \)00		X04	χ00	χ03	χ02			χ03		X04	χ05	χ06		χ07	χ00	
writeResult[31:0]=00000000	00000000				XFFF1	FFF0 X00	00000	3 (00000	0002 (000	0FFFF	XFFFFFF	FF X0000	FFFF XFFF	FFFFF	X0000F1	FF X00	00000
\ram[0][31:0]=00000000	00000000																
\ram[1][31:0]=00000000	00000000																
\ram[2][31:0]=00000000	00000000																
\ram[3][31:0]=00000000	00000000																
\registers[1][31:0]=00000010	00000010																
\registers[2][31:0]=00000002	0000+ \( \)000	00000						(00000	0003 (000	00002							
\registers[3][31:0]=0000FFFF	00000000					XFF:	FFFFF	0			<u> 10000FF</u>	FF					
<pre>\registers[4][31:0]=FFFFFFF</pre>	00000000											\FFFF	FFFF				