```
library IEEE;
  use ieee.std_logic_1164.ALL;
  use IEEE.STD_LOGIC_ARITH.ALL;
  use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity tb_cla_block is
end entity tb_cla_block;

architecture behavioral of tb_cla_block is

  component CLA_block is
    port(
      a, b : in std_logic_vector(3 downto 0);
      cin  : in std_logic;
      s    : out std_logic_vector(3 downto 0);
      cout : out std_logic
    );
  end component;


  signal tb_a, tb_b : std_logic_vector(3 downto 0):= (others => '0');
  signal tb_cin : std_logic:= '0';

  signal tb_cout : std_logic;
  signal tb_s : std_logic_vector(3 downto 0):= (others => '0');
  signal error : integer:=0;
begin

  DUT: CLA_block
  port map(
    a    => tb_a,
    b    => tb_b,
    cin  => tb_cin,
    s    => tb_s,
    cout => tb_cout
  );

  process
  begin
      tb_cin <= '0';
      for i in 0 to 3 loop
            for j in 0 to 3 loop
                tb_a <= conv_std_logic_vector(i,4);
                tb_b <= conv_std_logic_vector(j,4);
                wait for 10 ns;
                if(conv_integer(tb_cout & tb_s) /= (i + j)) then
              error <= error + 1;
            end if;
            end loop;
        end loop;

        tb_cin <= '1';
      for i in 0 to 3 loop
            for j in 0 to 3 loop
                tb_a <= conv_std_logic_vector(i,4);
                tb_b <= conv_std_logic_vector(j,4);
                wait for 10 ns;
                if(conv_integer(tb_cout & tb_s) /= (i + j + 1)) then
              error <= error + 1;
```

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            end if;
            end loop;
        end loop;

    wait for 10 ns;

    report("Ferdig!") severity note;
    std.env.stop;
  end process;
end architecture behavioral;
```