```
# Compile of cla_block.vhd was successful.
# Compile of tb_cla_block.vhd was successful.
# Compile of fulladder.vhd was successful.
# 3 compiles, 0 failed with no errors.
vsim -voptargs=+acc work.tb_cla_block
# vsim -voptargs="+acc" work.tb_cla_block
# Start time: 21:36:37 on Sep 22,2021
# ** Note: (vsim-3813) Design is being optimized due to module
recompilation...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading ieee.std_logic_arith(body)
# Loading ieee.std_logic_unsigned(body)
# Loading std.env(body)
# Loading work.tb_cla_block(behavioral)#1
# Loading work.cla_block(mixed)#1
# Loading work.full_adder(gate_level)#1
add wave -position insertpoint  \
sim:/tb_cla_block/tb_a
add wave -position insertpoint  \
sim:/tb_cla_block/tb_b
add wave -position insertpoint  \
sim:/tb_cla_block/tb_cin
add wave -position insertpoint  \
sim:/tb_cla_block/tb_cout
add wave -position insertpoint  \
sim:/tb_cla_block/tb_s
run -all
# ** Note: Ferdig!
#    Time: 330 ns  Iteration: 0  Instance: /tb_cla_block
# Break in Process line__39 at /home/tsauren/M-
drive/Documents/oblig2/tb_cla_block.vhd line 67
```