```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity CLA_top is
  generic(
    width : positive := 32
  );
  port(
    a, b : in  std_logic_vector(width-1 downto 0);
    cin  : in  std_logic;
    s  : out std_logic_vector(width-1 downto 0);
    cout : out std_logic
  );
end entity CLA_top;

architecture mixed of CLA_top is
  component CLA_block is
    port (
      a, b : in std_logic_vector(3 downto 0);
      cin  : in std_logic;
      s    : out std_logic_vector(3 downto 0);
      cout : out std_logic
    );
  end component CLA_block;

  signal c : std_logic_vector(8 downto 0); -- 8, fordi det blir brukt 8 CLA-blokker
  signal i : integer := 0;
  begin
      c(0) <= cin;

  min_lokke: for i in 0 to 7 generate ny_komponent: CLA_block
  port map(
      a => a(i*4 + 3 downto i*4),
      b => b(i*4 + 3 downto i*4),
      cin => c(i),
      s => s(i*4 + 3 downto i*4),
      cout => c(i+1)
    );

end generate;
end architecture mixed;
```