```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity CLA_block is
  port(
    a, b : in std_logic_vector(3 downto 0);
    cin  : in std_logic;
    s    : out std_logic_vector(3 downto 0);
    cout : out std_logic
  );
end entity CLA_block;
architecture mixed of CLA_block is
  component full_adder is
    port (
      a,b, cin : in std_logic;
      s, cout : out std_logic
    );
  end component full_adder;

  signal p : std_logic_vector(3 downto 0);
  signal g : std_logic_vector(3 downto 0);
  signal p30 : std_logic;
  signal g30 : std_logic;
  signal c : std_logic_vector(4 downto 0);
  begin
  p(0) <= a(0) or b(0);
  p(1) <= a(1) or b(1);
  p(2) <= a(2) or b(2);
  p(3) <= a(3) or b(3);

  g(0) <= a(0) or b(0);
  g(1) <= a(1) or b(1);
  g(2) <= a(2) or b(2);
  g(3) <= a(3) or b(3);

  p30 <= (p(3) and p(2) and p(1) and p(0));
  g30 <= (g(3) or (p(3) and (g(2) or (p(2) and (g(1) or (p(1) and g(0)))))));
  cout <=  (g30 or (cin and p30));
  c(0) <= cin;

  min_lokke: for i in 0 to 3 generate ny_komponent: full_adder
  port map(
    a => a(i),
    b => b(i),
    cin => c(i),
    s => s(i),
    cout => c(i+1)
    );
end generate;

end architecture mixed;
```