```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity full_adder is
 Port (
 a,b,cin : in STD_LOGIC;
 s,cout : out STD_LOGIC
 );
end full_adder;

architecture gate_level of full_adder is

begin

 s <= a XOR b XOR cin ;
 cout <= ((a XOR b) and cin) or (a and b);

end gate_level;
```