NATIONAL OPEN UNIVERSITY OF NIGERIA
14-16 AHMADU BELLO WAY, VICTORIA ISLAND LAGOS
SCHOOL OF SCIENCE AND TECHNOLOGY

MAY/JUNE 2012 EXAMINATION

CIT 309 COMPUTER ARCHITECTURE
TIME: 3 HOURS

INSTRUCTION: ANSWER ANY FIVE QUESTIONS IN ALL

1a. List and discuss the basic functions that a computer can perform. *[6 marks]*
1b. Write short note on the components of the C. P. U.
[6 marks]
1c. Illustrate with simple diagram the basic Instruction fetch and execution cycle. *[8 marks]*

2a. Define the following:
i. processors instruction.
ii. Instruction.
iii. Data types.
[5 marks]
2b. Using the Instruction: ADD, R, Y to explain the following:
i. ADD, R, Y
ii. Y
iii. R
iv. ADD
[5 marks]
2c. Explain the elements of a machine instruction.
[10 marks]

3a Discuss how the A.L.U is interconnected with the rest of the processor. *[8 marks]*
3b. Briefly state how the 2s complement operation can be perform on any given integer numbers.

[6 marks]
3c. When does the Overflow rule occur?
[6 marks]

4a. i. Explain what is meant by Micro-operation?
[4 marks]

ii. Give 4 examples of shorter subcycles/operation that made up of an instruction cycle.

iii.
[2 marks]

4b. Write the full meaning of the following acronym:
i. MAR.
ii. MBR.
iii. IR.
iv. PC.
[2 marks]

4c. Define the following acronym:
i. MAR.
ii. MBR.
iii. IR.
iv. PC.
v. Interrupt.
vi. Timer.
[12 marks]

5a. Define the following:
i. Dual core processor chip.
[3 marks]
ii. L2 cache.
[3 marks]
iii. System control element (SCE).
[2 marks]
iv. Main store control (MSC).
[2 marks]
v. Memory card.
[2 marks]

5b. Write short note on the simultaneous execution of the action: Read word from memory and Increment PC.
[6 marks]

5c. Discuss why (PC - MAR) must precede (Memory - MBR) operation in fetch cycle. *[2 marks]*

6a. List and briefly explain the four (4) types of parallel processor system. *[10 marks]*

6b. List and describe the two (2) basic tasks of control unit.
[6 marks]

6c. Explain the following:
a. Clock.
[2 marks]
b. Flags.
[2 marks]

7a. Highlight the features and functionality of a multi programming system to accommodate multiple processor.
[2 marks]

7b. Write short note on the following:
[8 marks]

i. Multithreading
ii. Process switch
iii. Thread
iv. Thread switch

7c, List and briefly explain the four (4) characteristics of Reduced Instruction Set architecture.

[10 marks]