Nixie Alarm Clock - Base

Rev A 09/10/2022

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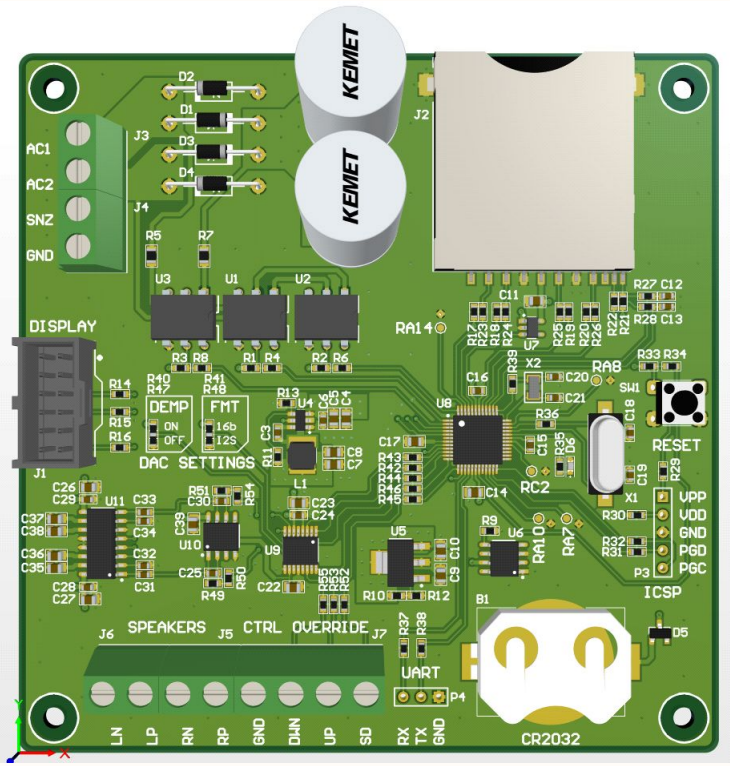
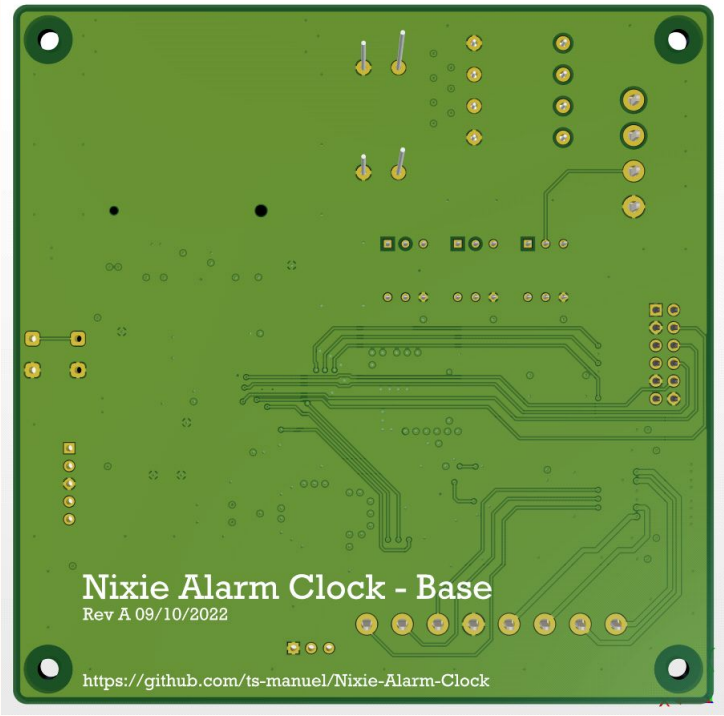
TOP VIEW



BOTTOM VIEW



DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DEBUG NOTE:
Example text for debug notes.

POWER SUPPLY NOTE:
Example text for power supply notes

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

Title: [01] - COVER PAGE.SchDoc			
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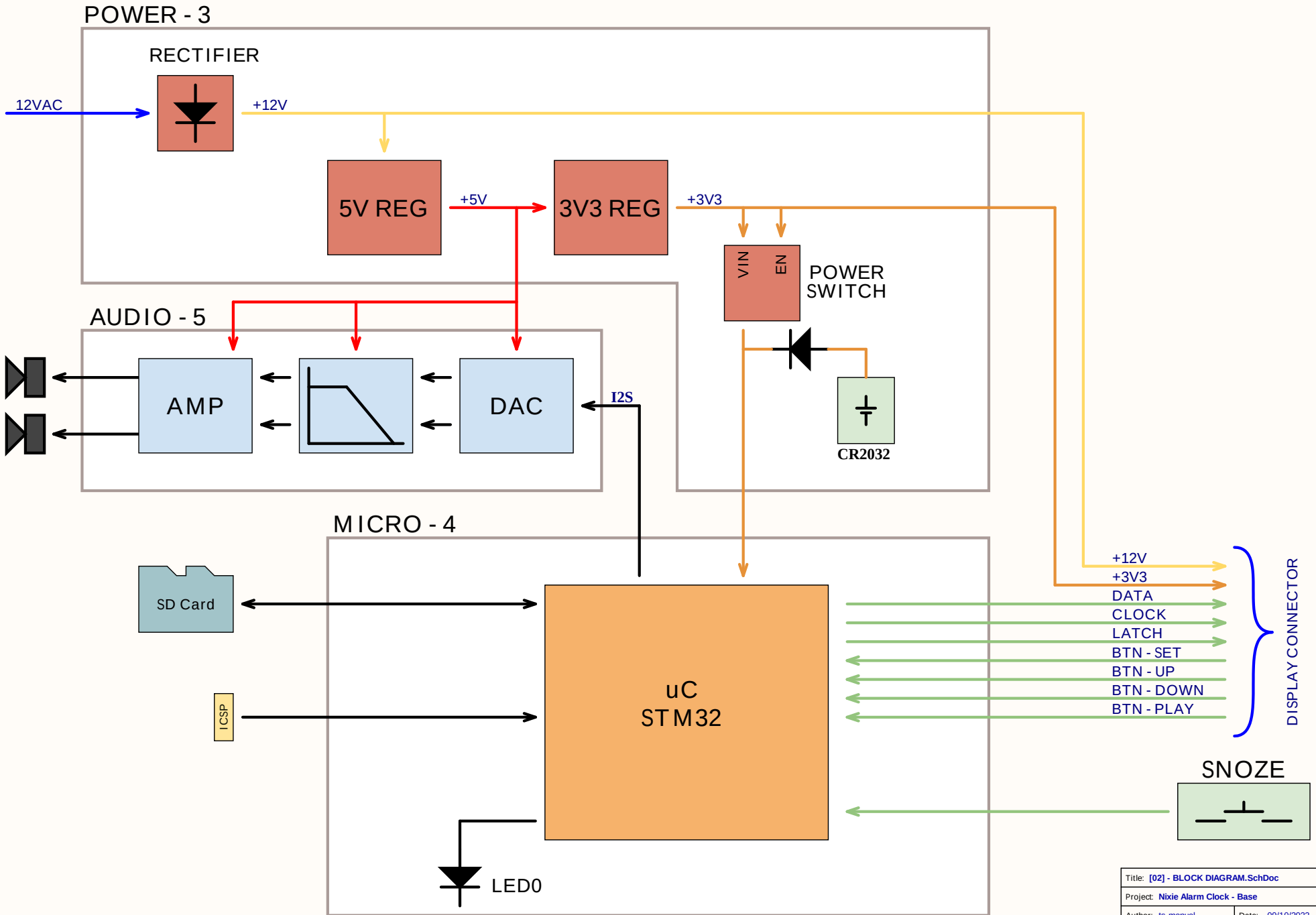

Title: [02] - BLOCK DIAGRAM.SchDoc	
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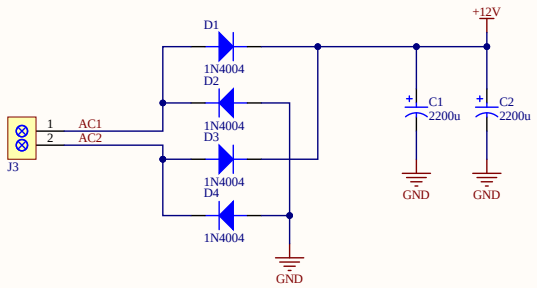
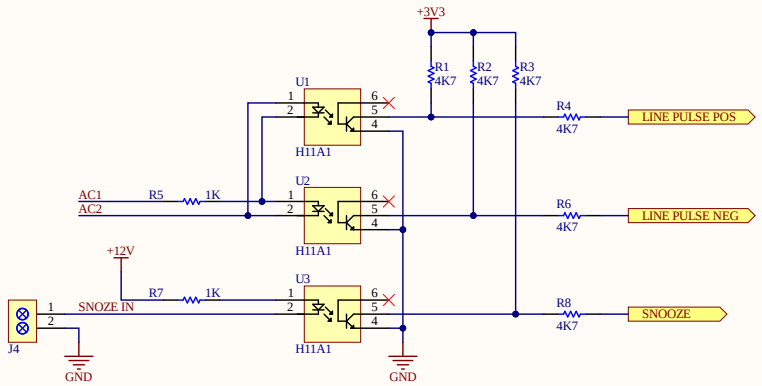
BRIDGE RECTIFIER



POWER SUPPLY NOTE:

Maximum +12V current load:
5V SWCH 320mA
DISPLAY 750mA
TOT = 1.1A

AC PULSE / SNOOZER OPTOCUPLERS



5V BUCK & 3V3 LDO

POWER SUPPLY NOTE:

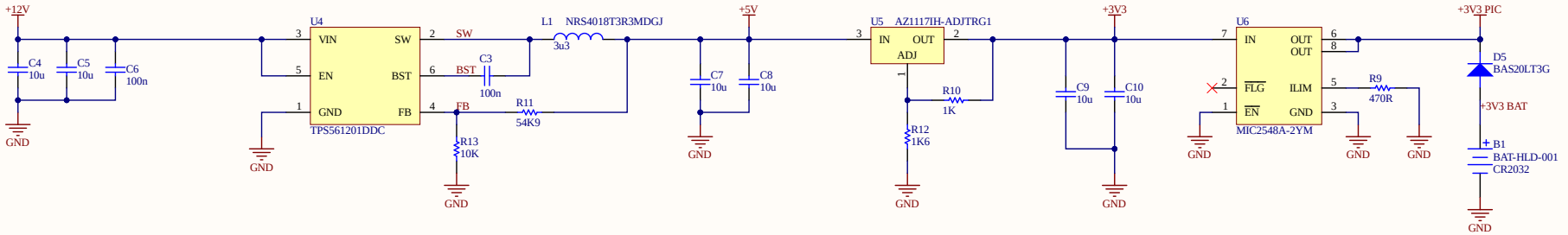
Maximum +5V current load:
3V3 LDO 220mA
DAC 25mA
AMP 350mA
TOT = 600mA

POWER SUPPLY NOTE:

Maximum +3V3 current load:
Display 12mA
SD 100mA
uC 6.3mA
TOT = 220mA

DESIGN NOTE:

Maximum reverse charge current for CR2032 is 1uA
Diode leakage must be lower



DESIGN NOTE:

The MIC2548 isolates +3V3 PIC from +3V3 when mains power is removed.
Reverse leackage = 1uA

DESIGN NOTE:

Curren limit on +3V3 PIC:
230 / R = 490 mA

Title: [03] - POWER.SchDoc	
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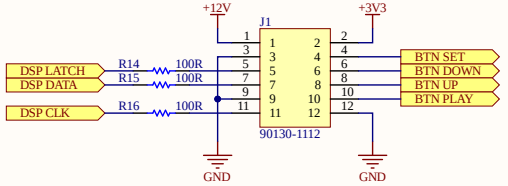
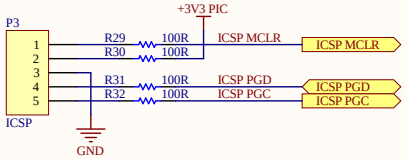
DISPLAY CONNECTOR



POWER SUPPLY NOTE:

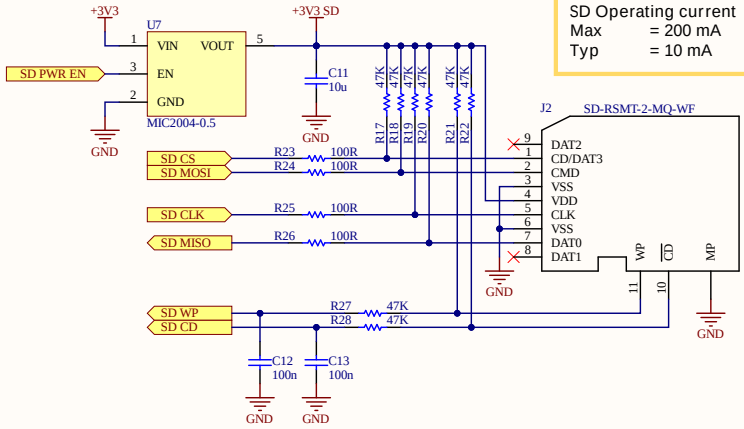
+12V = 750 mA (max)
+3V3V = 12 mA (max)

ICSP CONNECTOR



DEBUG NOTE:
The PICkit 4 doesn't provide enought power, during programming the board must be powered externally

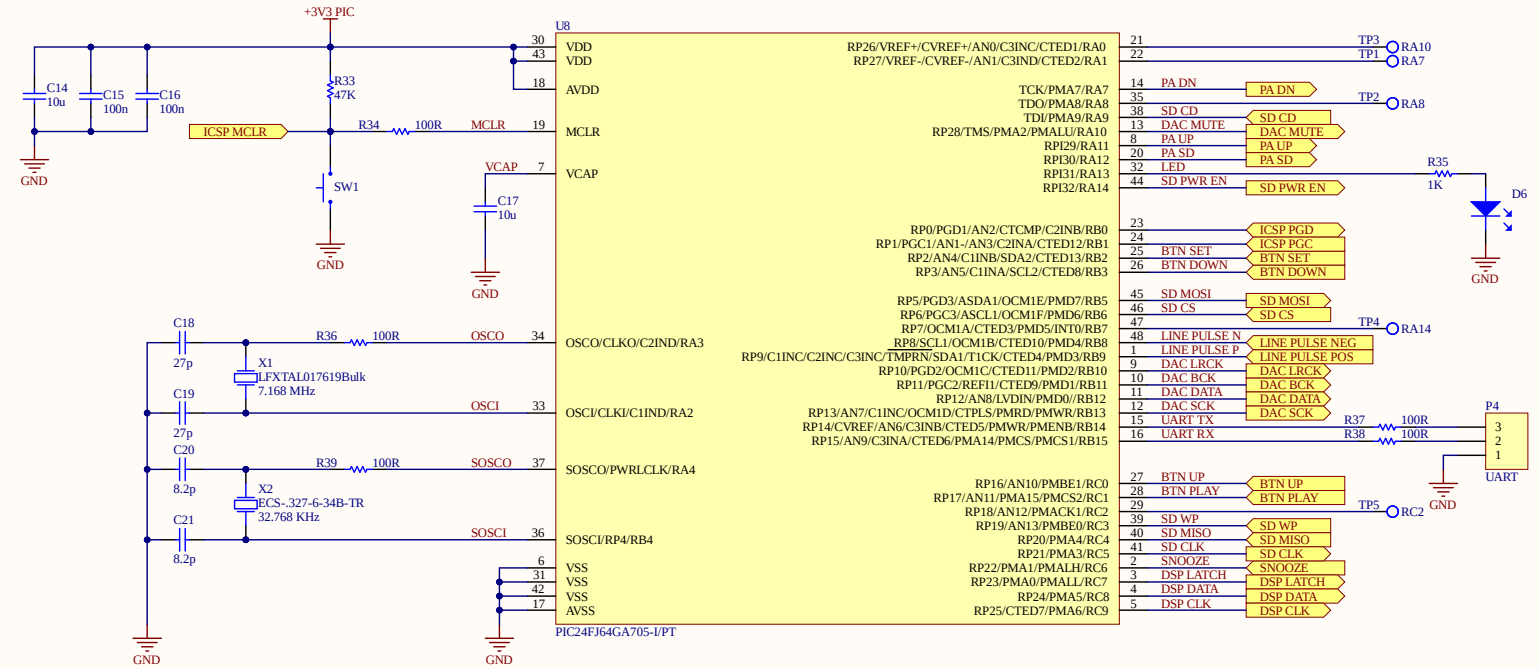
SD CARD



POWER SUPPLY NOTE:

SD Operating current
Max = 200 mA
Typ = 10 mA

MICROCONTROLLER



POWER SUPPLY NOTE:

Microcontroller current:
Operating 32 Mhz = 6.3 mA
Sleep + RTC = 7.4 uA
LV Sleep + RTC = 3.3 uA

DEBUG NOTE:

Set DAC SCK frequency to USB PLL / 14 = 6.144 MHz
0.0% error with 48 kHz audio sample rate

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24bit SIGMA DELTA STEREO DAC

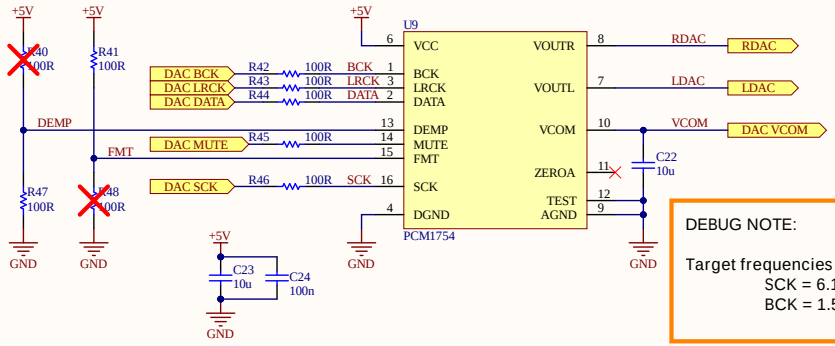
POWER SUPPLY NOTE:

DAC Supply current
+5V = 25 mA

DEBUG NOTE:

DEMP: DE–EMPHASIS FUNCTION
LOW = 44.1 kHz de–emphasis OFF
HIGH = 44.1 kHz de–emphasis ON

FMT: DATA FORMAT
LOW = 16– to 24–bit, I2S format
HIGH = 16–bit right–justified



DEBUG NOTE:

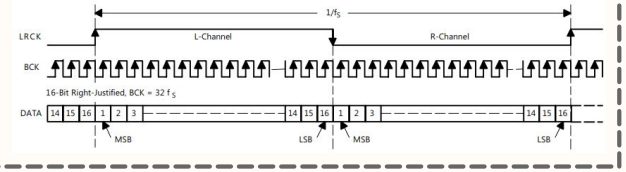
Target frequencies for 48 kHz FS
SCK = 6.144 MHz
BCK = 1.536 MHz

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)						
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1152 f_S
8 kHz	1.024	1.536	2.048	3.072	4.096	6.144	9.216
16 kHz	2.048	3.072	4.096	6.144	8.192	12.288	18.432
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576	36.864
44.1 kHz	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688	(1)
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864	(1)
88.2 kHz	11.2896	16.9344	22.5792	33.8688	45.1584	(1)	(1)
96 kHz	12.288	18.432	24.576	36.864	49.152	(1)	(1)
192 kHz	24.576	36.864	(1)	(1)	(1)	(1)	(1)

(1) This system clock rate is not supported for the given sampling frequency.

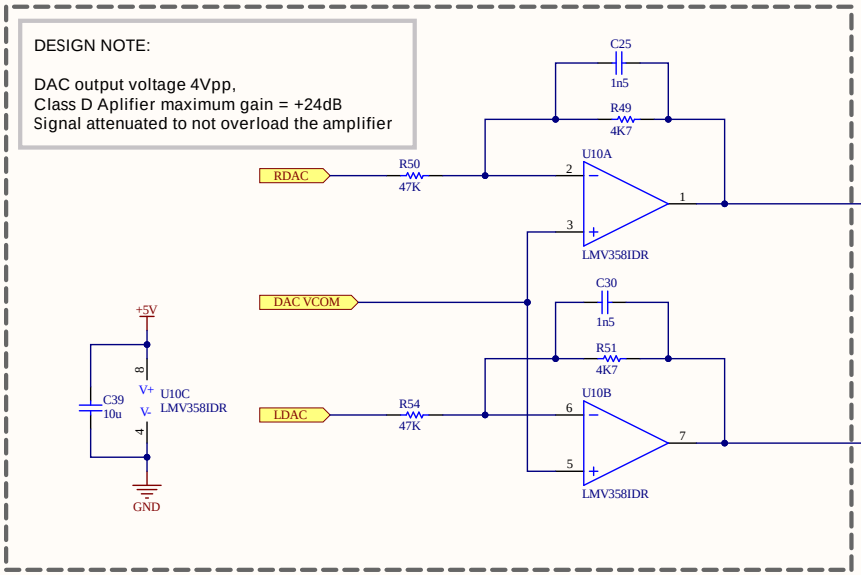
Standard Data Format; L-Channel = HIGH, R-Channel = LOW



LOW PASS FILTER Gain -20dB Ft 20kHz

DESIGN NOTE:

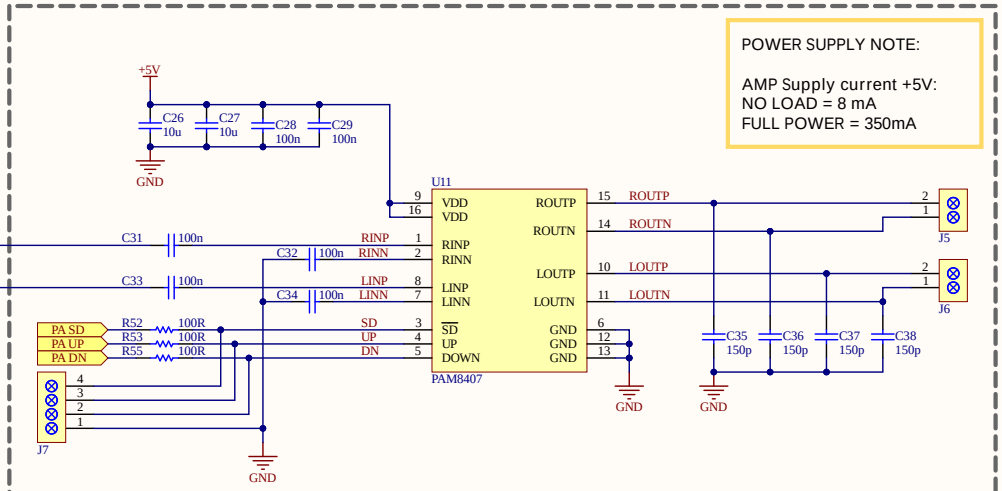
DAC output voltage 4Vpp,
Class D Aplifier maximum gain = +24dB
Signal attenuated to not overload the amplifier



CLASS D AMPLIFIER

POWER SUPPLY NOTE:

AMP Supply current +5V:
NO LOAD = 8 mA
FULL POWER = 350mA



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