

i.MX6 Demo Board

Rev: 01 2026-02-16

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PCB:

Number of Layers:	6
Thickness:	1.6 mm ±10%
Overall Dimensions:	80.00 x 70.00 mm
Silkscreen:	White
Solder Mask:	Green
Via Solder Tenting:	YES
Copper Finish:	ENIG
Min Track / Spacing:	0.12 mm / 0.12 mm
Min Hole Diameter:	0.20 mm

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes

DEBUG NOTE:
Example text for debug notes

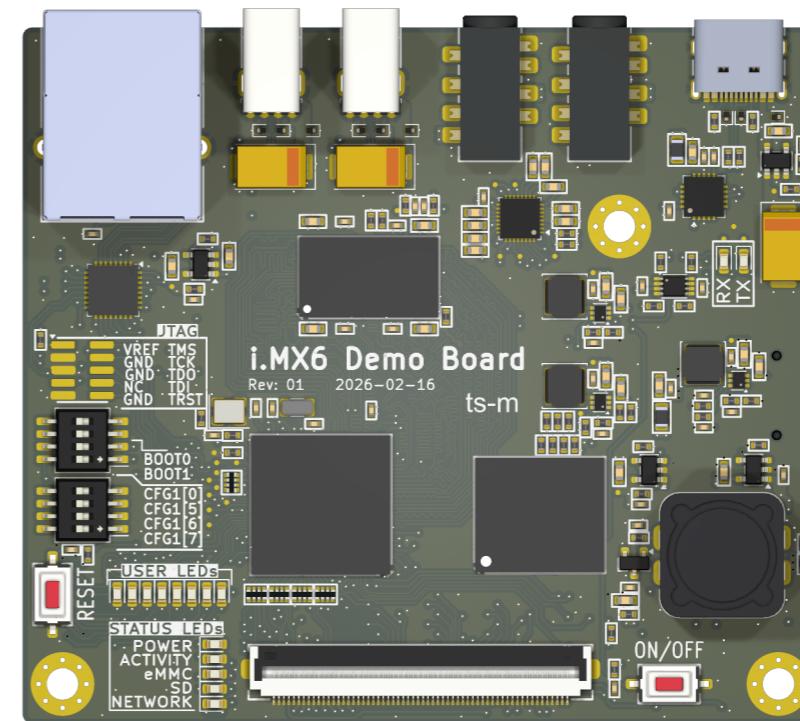
DESIGN NOTE:
Example text for critical design notes

LAYOUT NOTE:
Example text for design notes

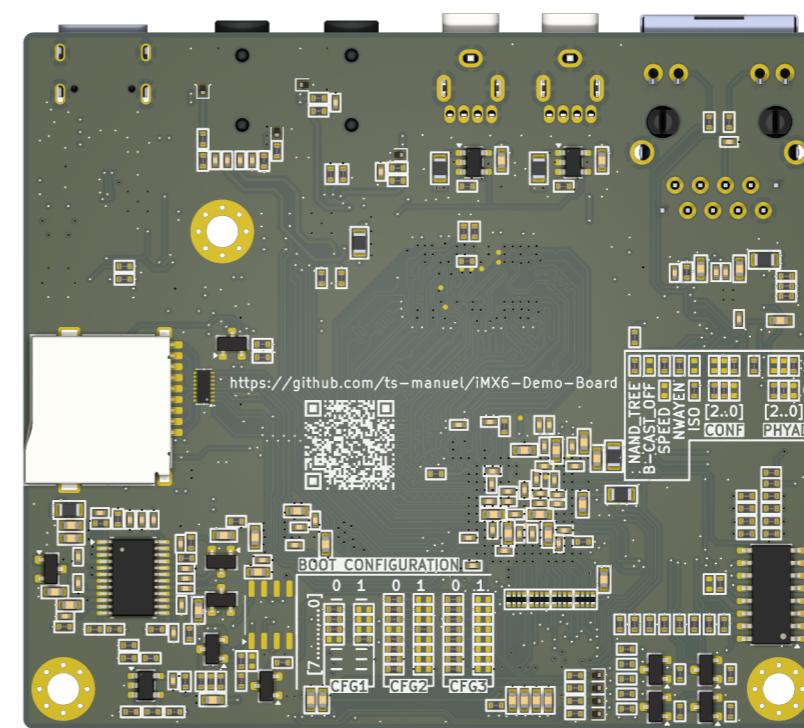
POWER TREE

i.MX6ULL MAIN

TOP VIEW



BOTTOM VIEW



Title: i.MX6 Demo Board

File: iMX6 Demo Board.kicad_sch

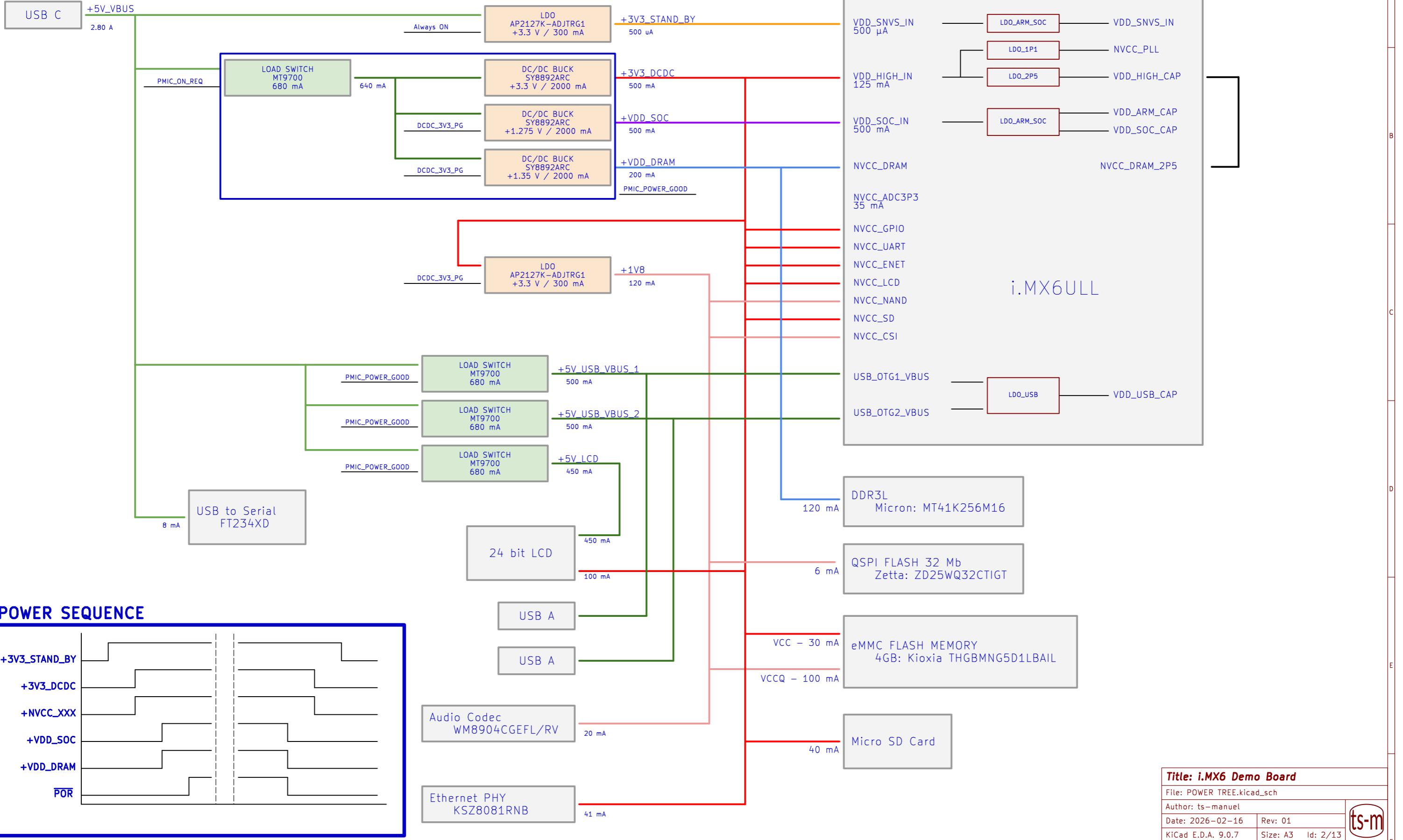
Author: ts-manuel

Date: 2026-02-16 Rev: 01

KiCad E.D.A. 9.0.7 Size: A3 Id: 1/13



POWER TREE



Title: i.MX6 Demo Board

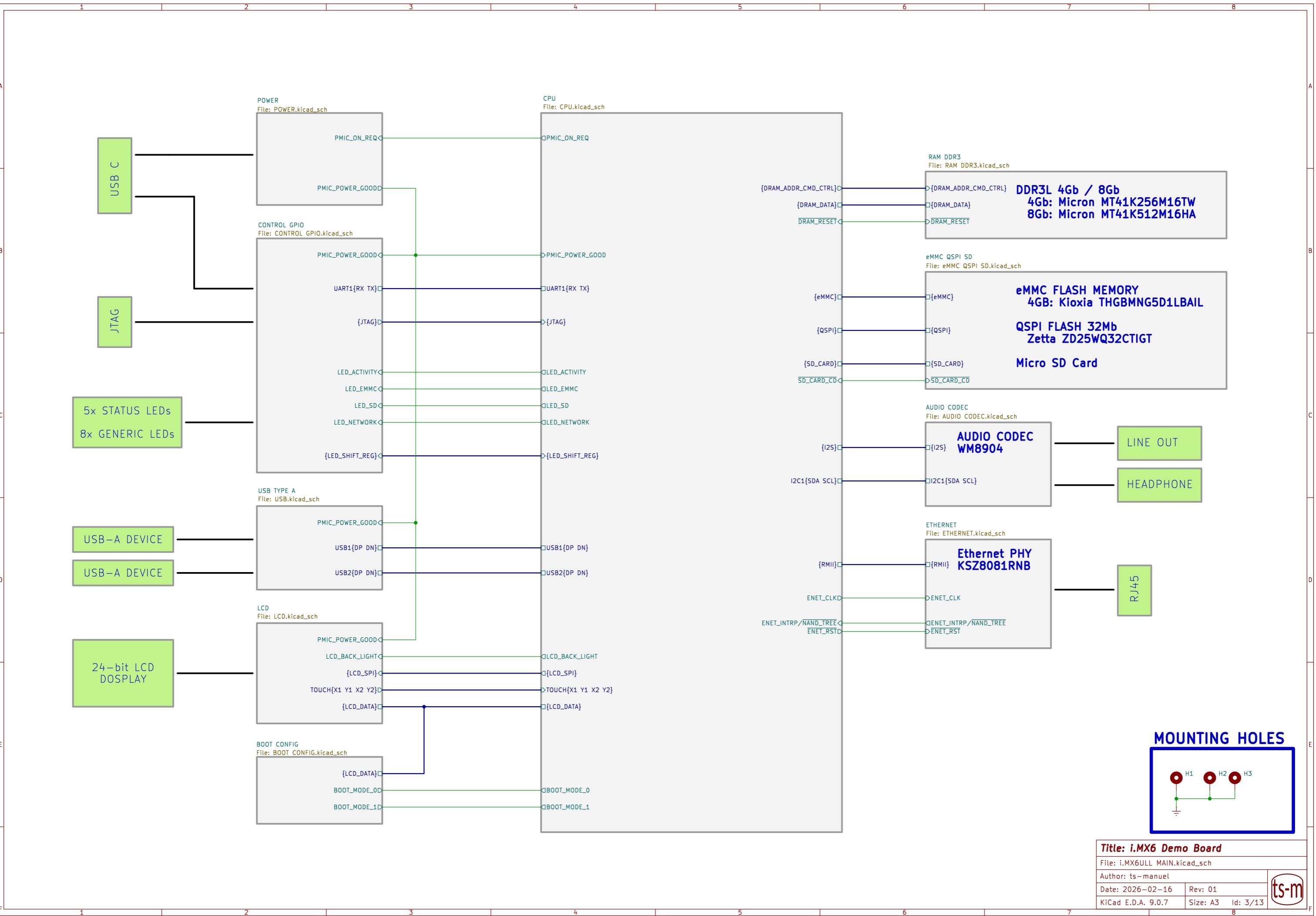
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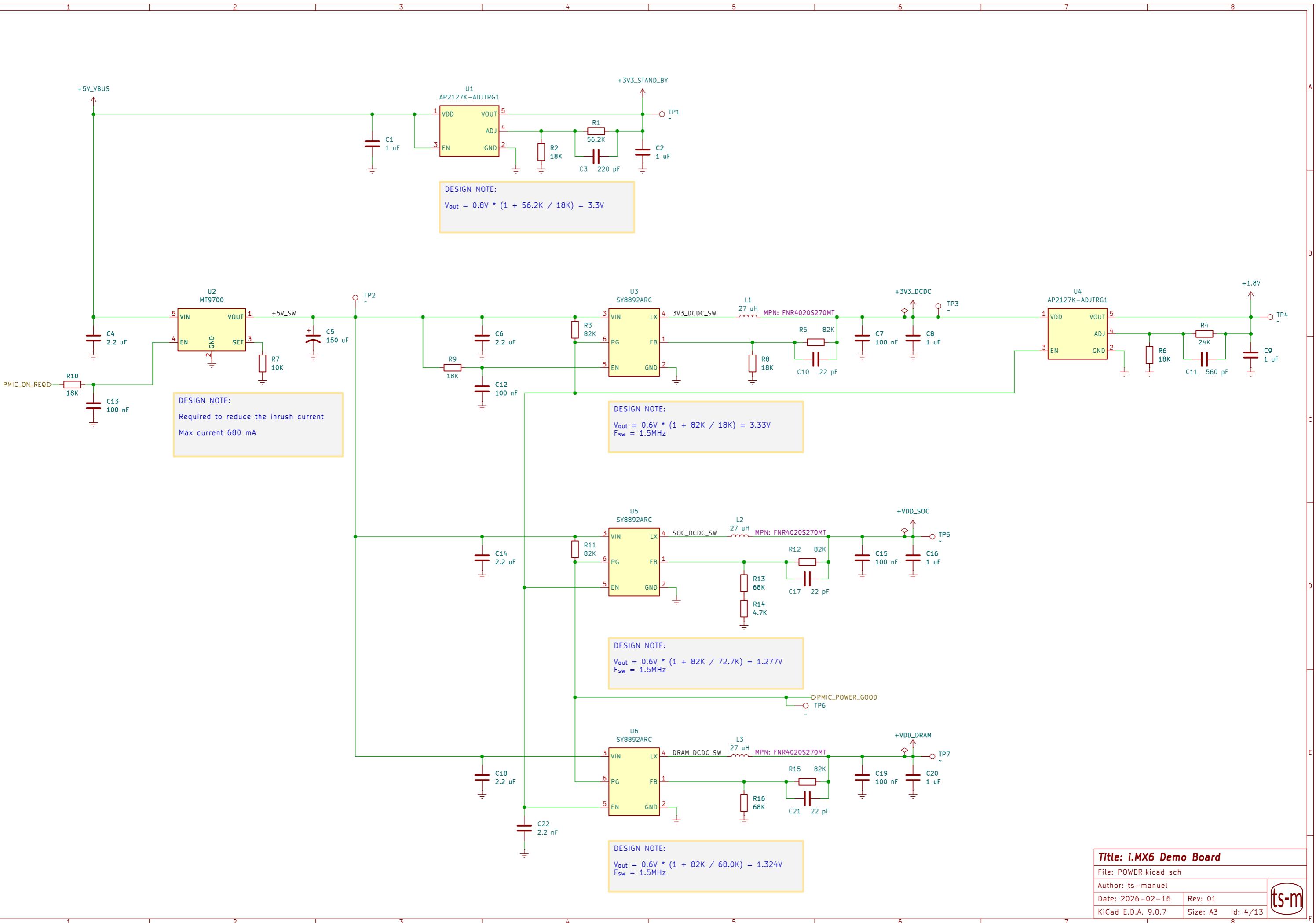
Author: ts-manuel

Date: 2026-02-16 Rev: 0

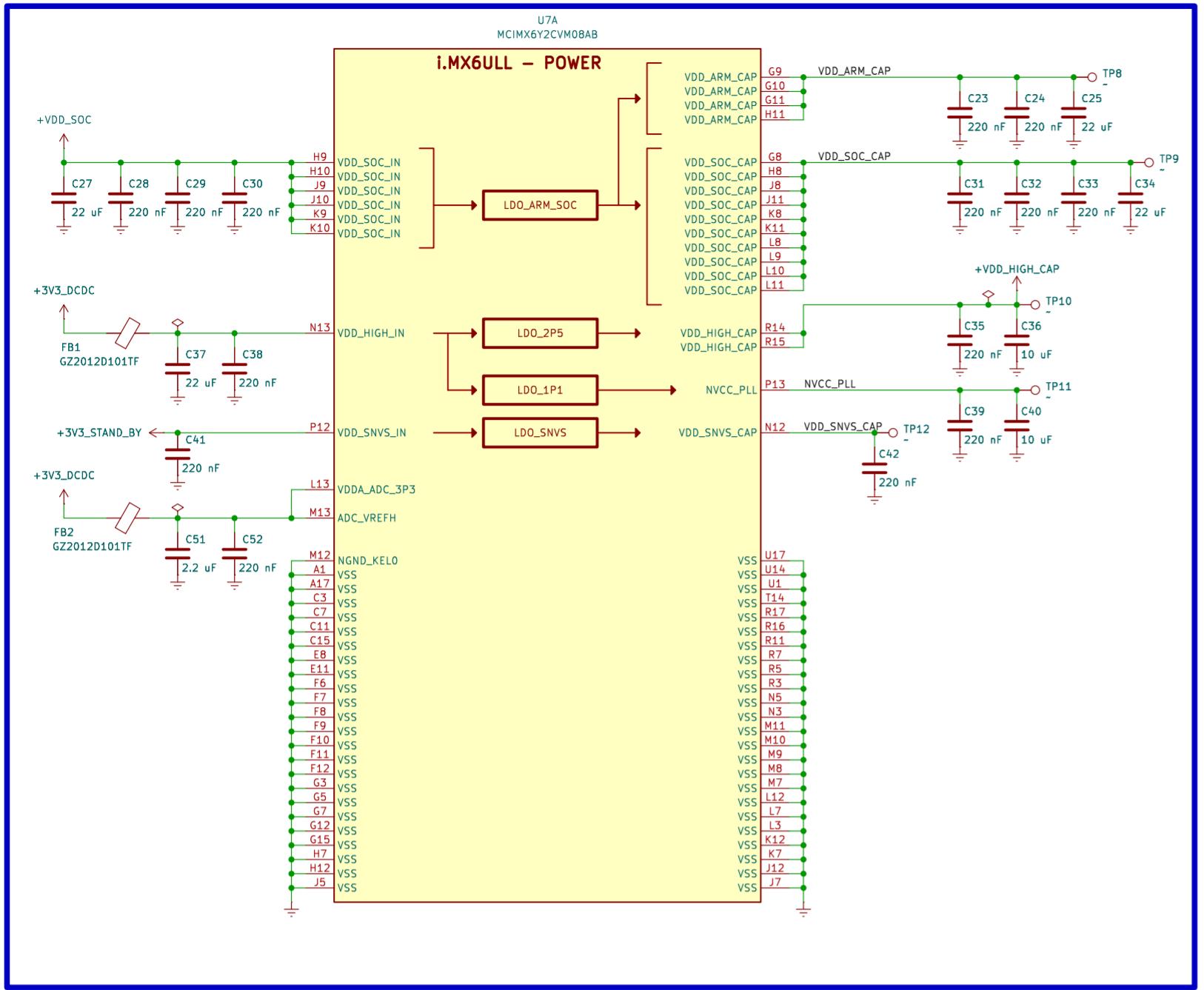
KiCad E.D.A. 9.0.7



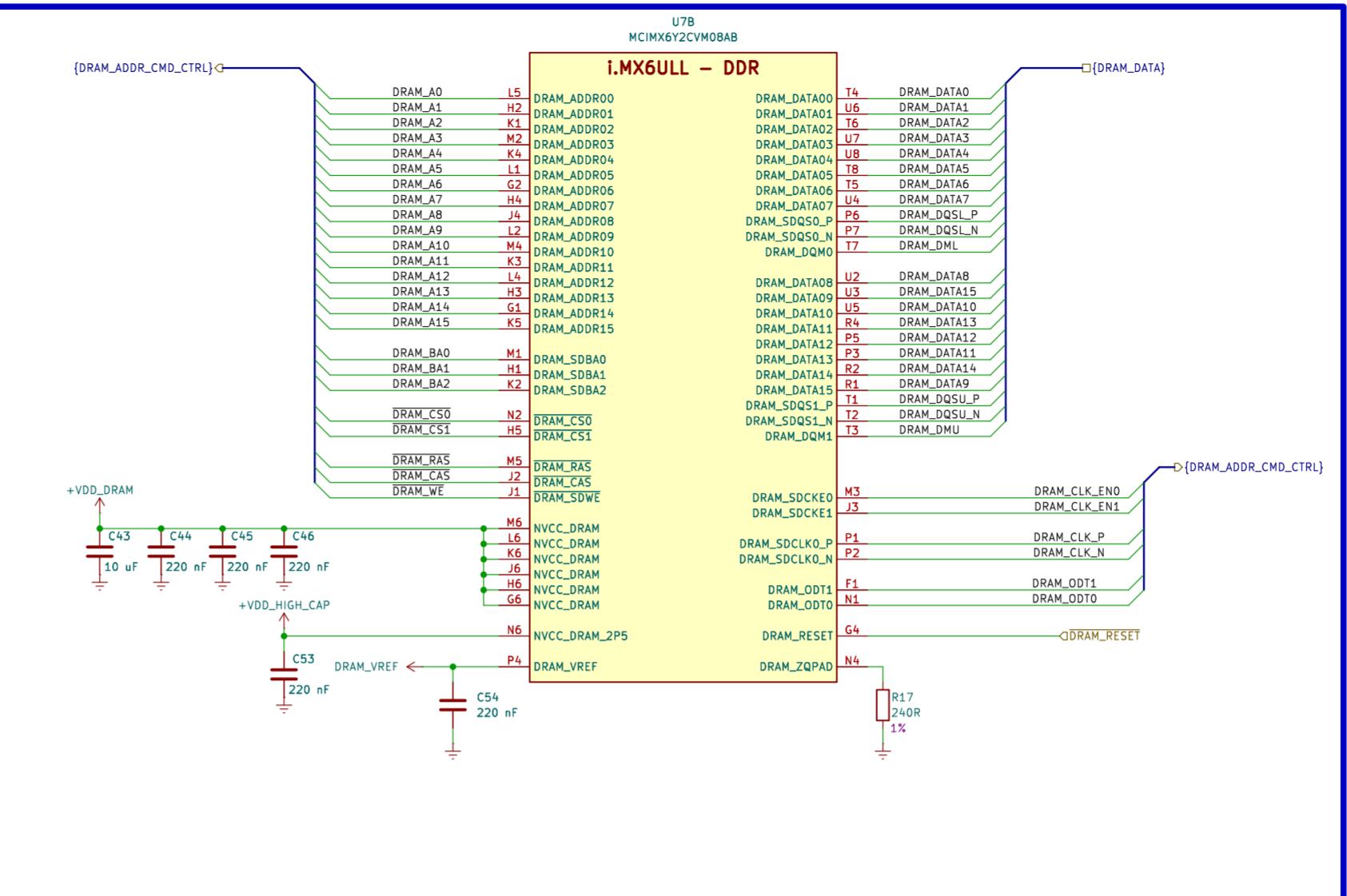




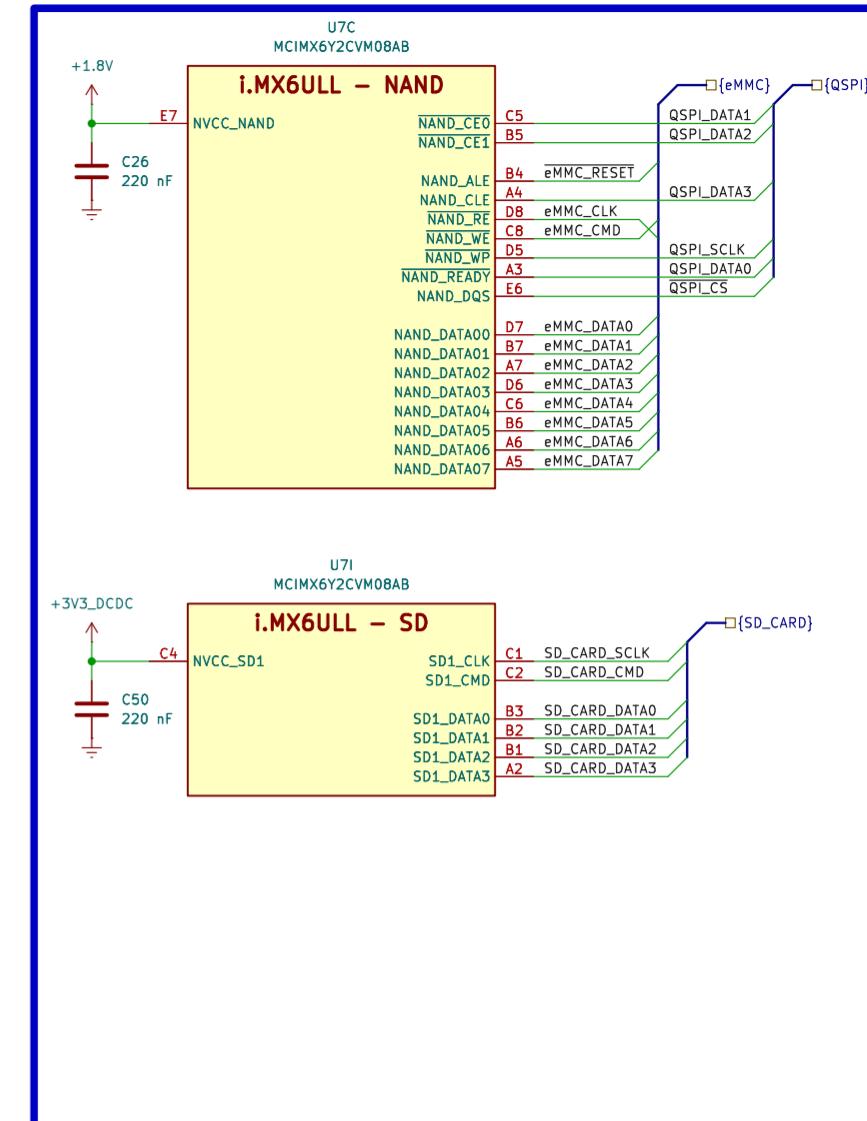
POWER



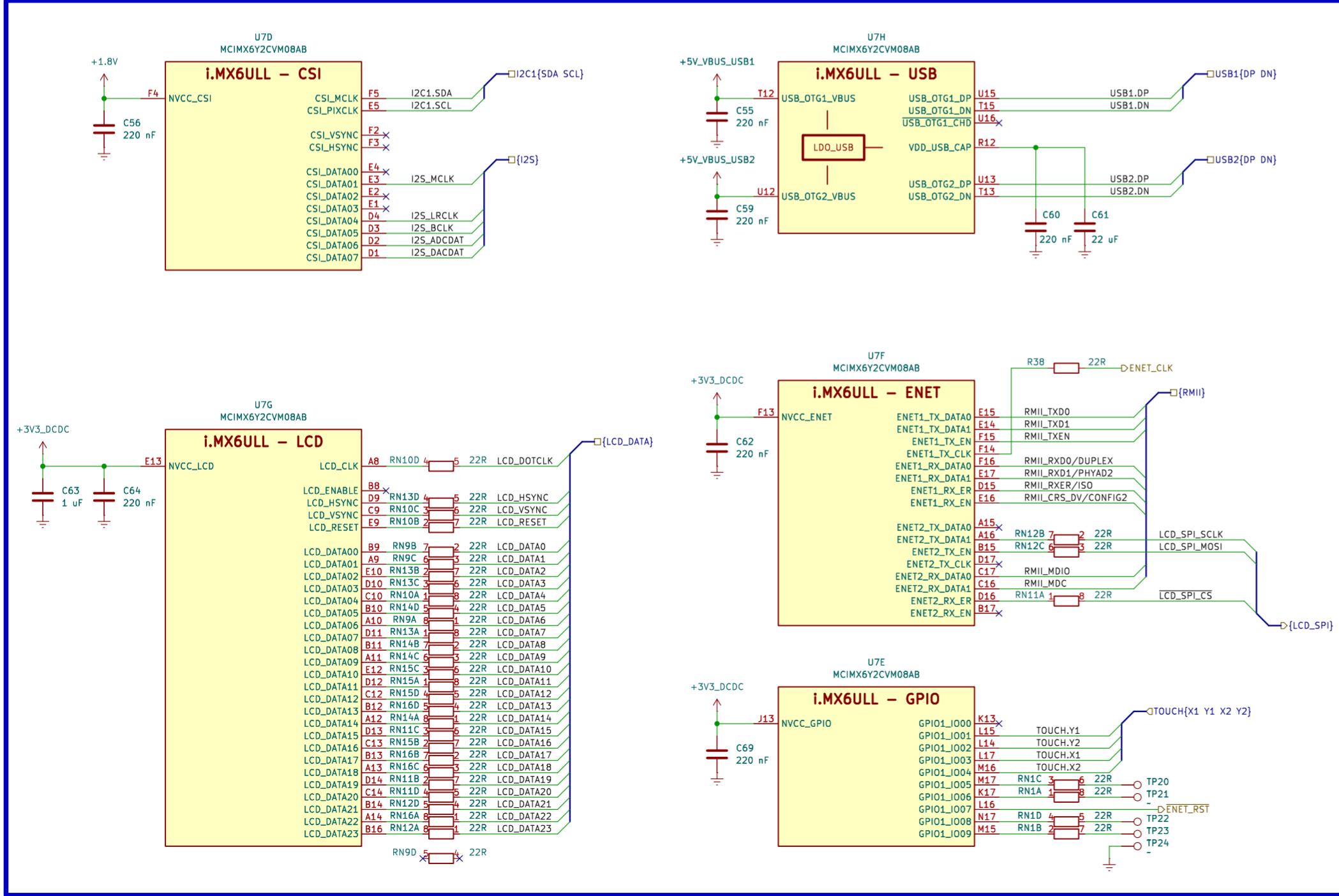
DDR3



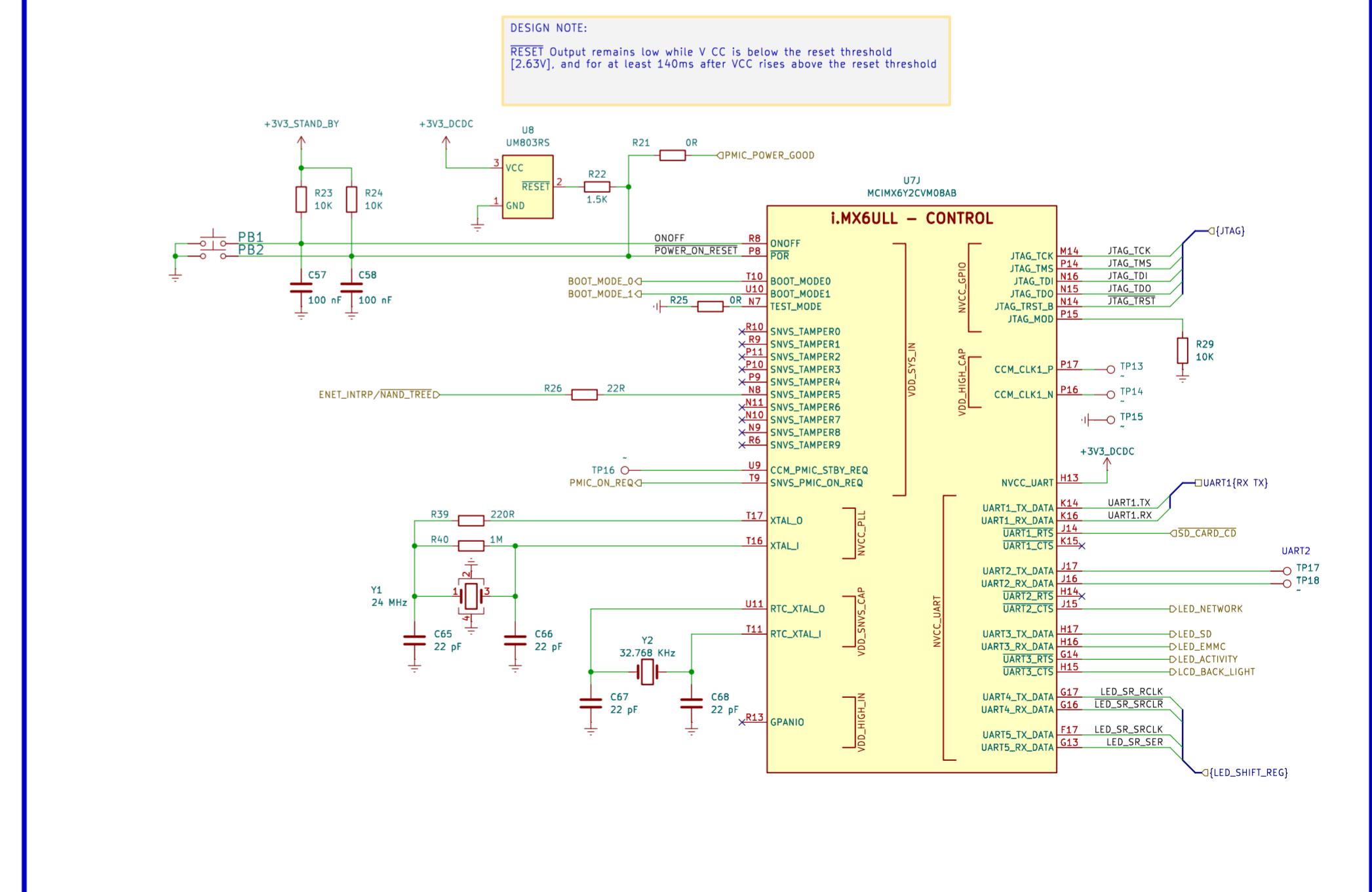
eMMC/QSPI/SD

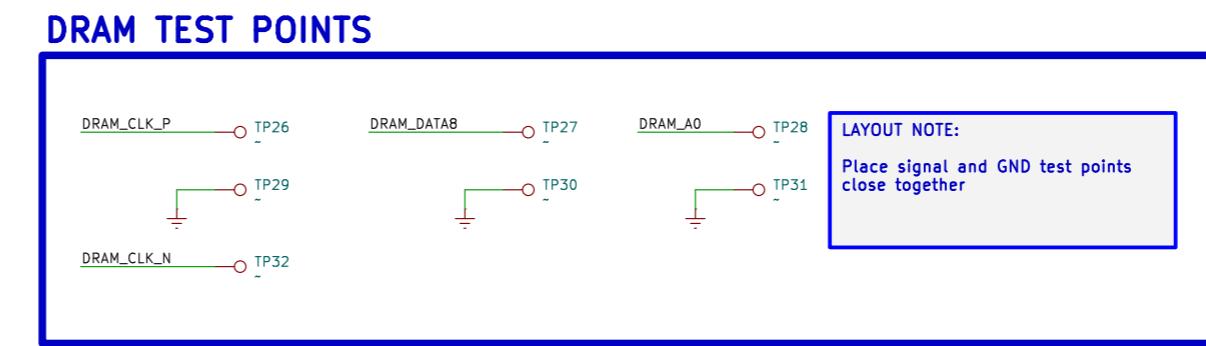
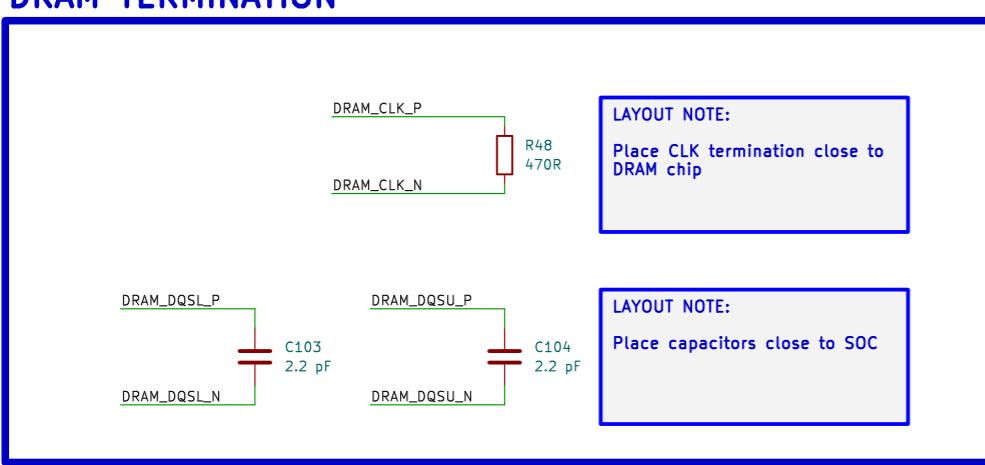
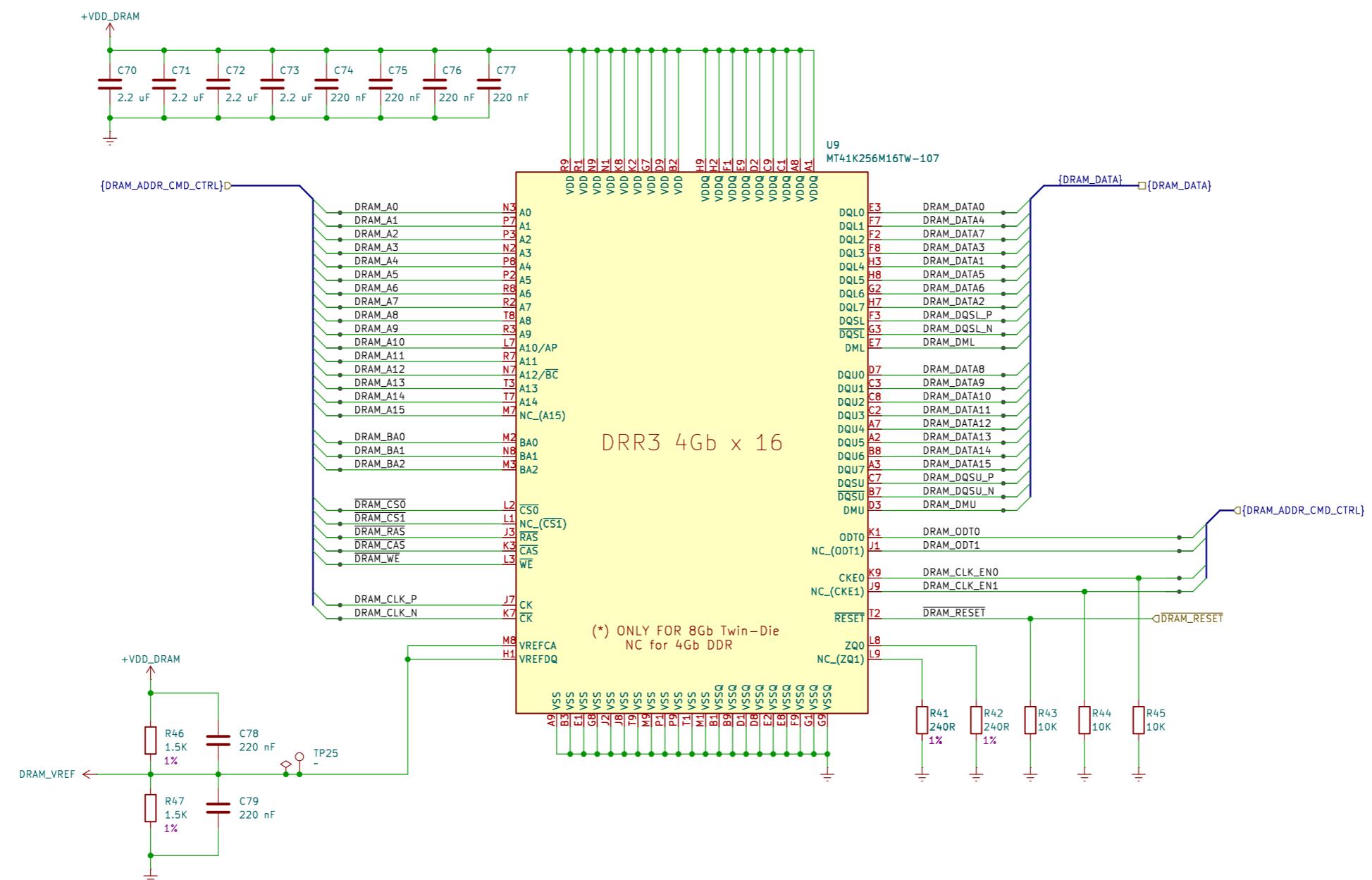


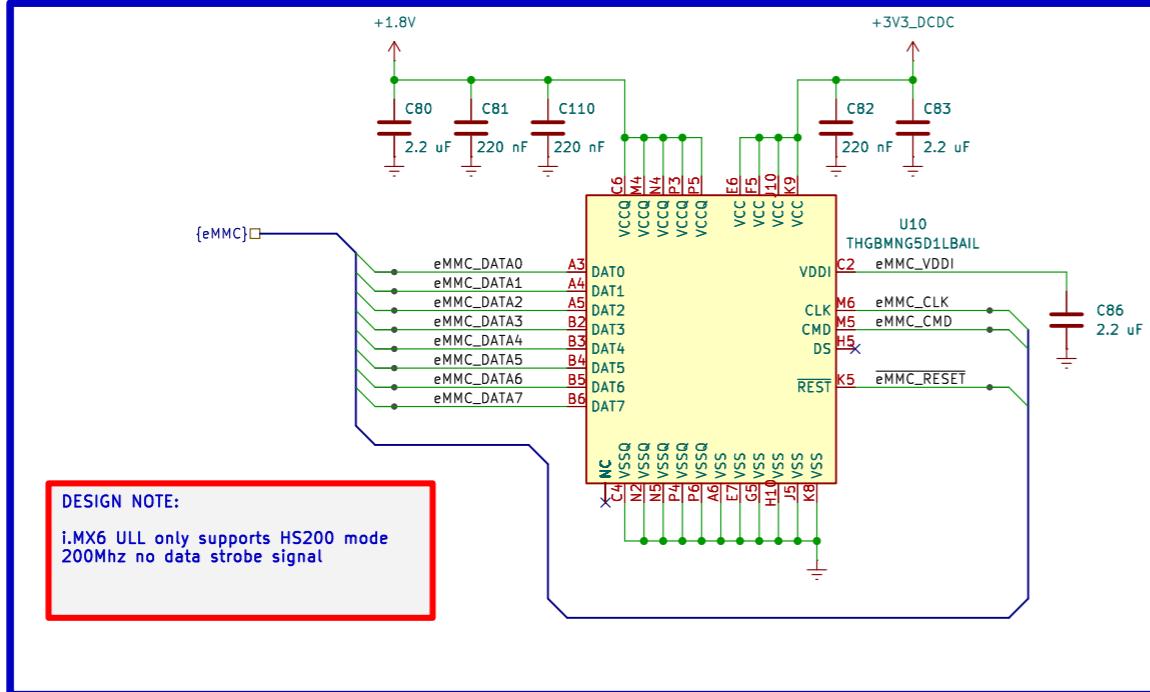
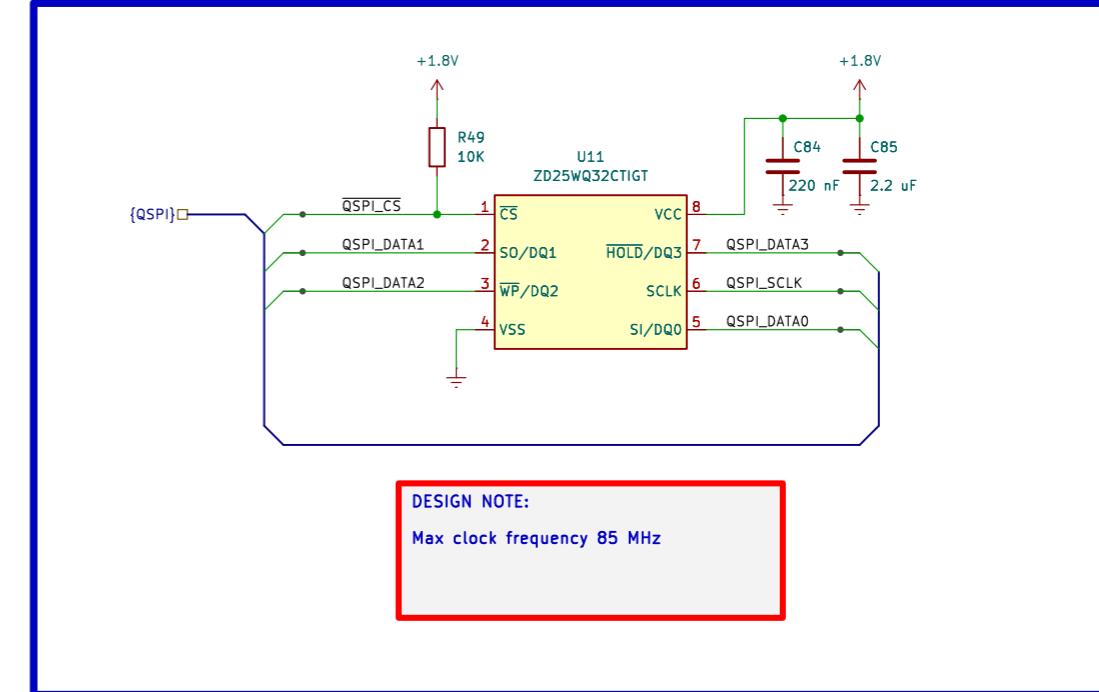
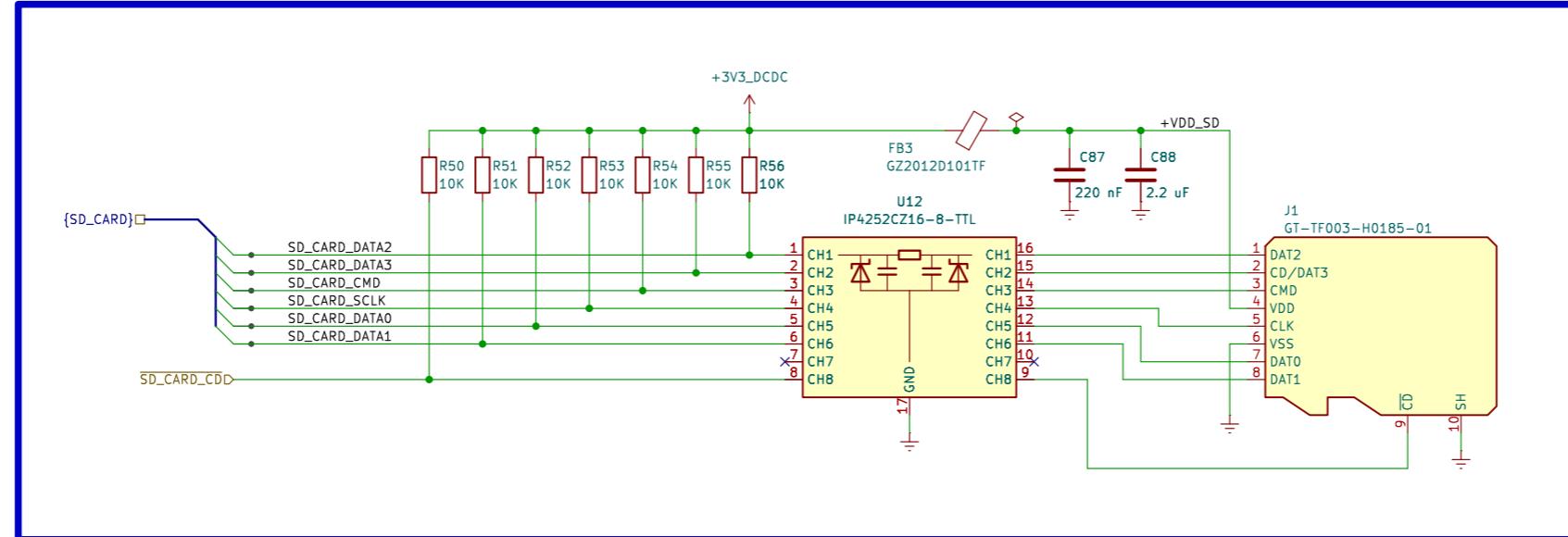
PERIPHERALS



CONTROL





eMMC**QSPI****MICRO SD**

Title: i.MX6 Demo Board

File: eMMC_QSPI_SD.kicad_sch

Author: ts-manuel

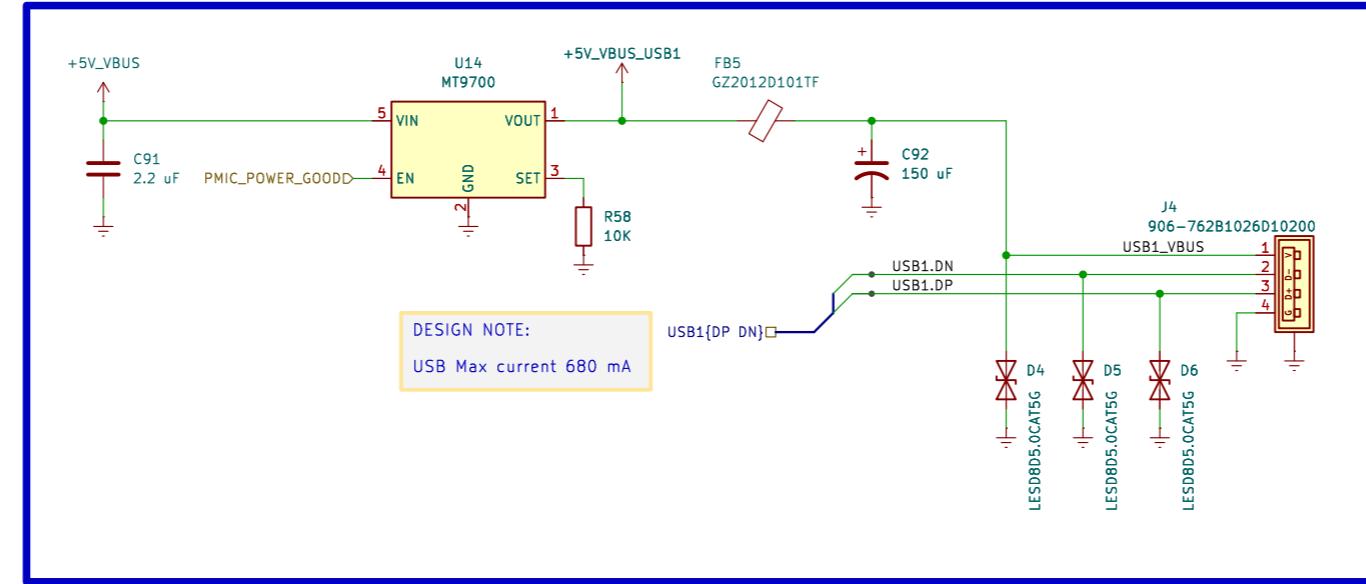
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A

A

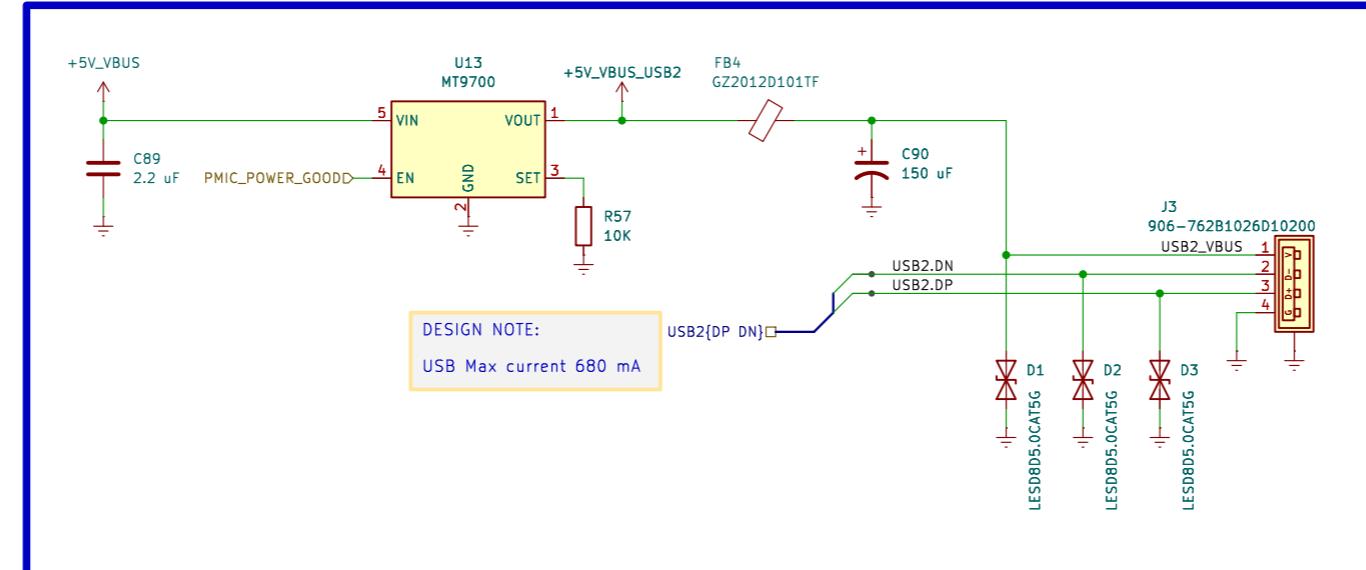
USB1

B

B

C

C

USB2

D

D

E

E

F

F

Title: i.MX6 Demo Board

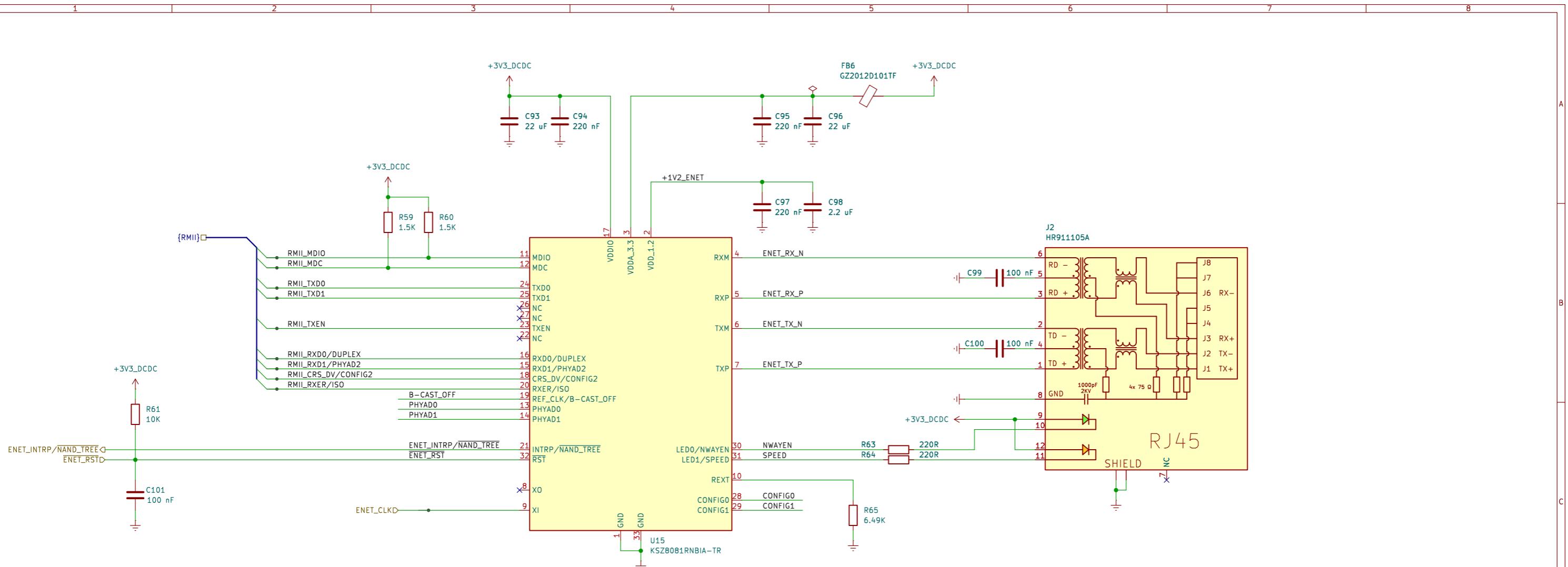
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Author: ts-manuel

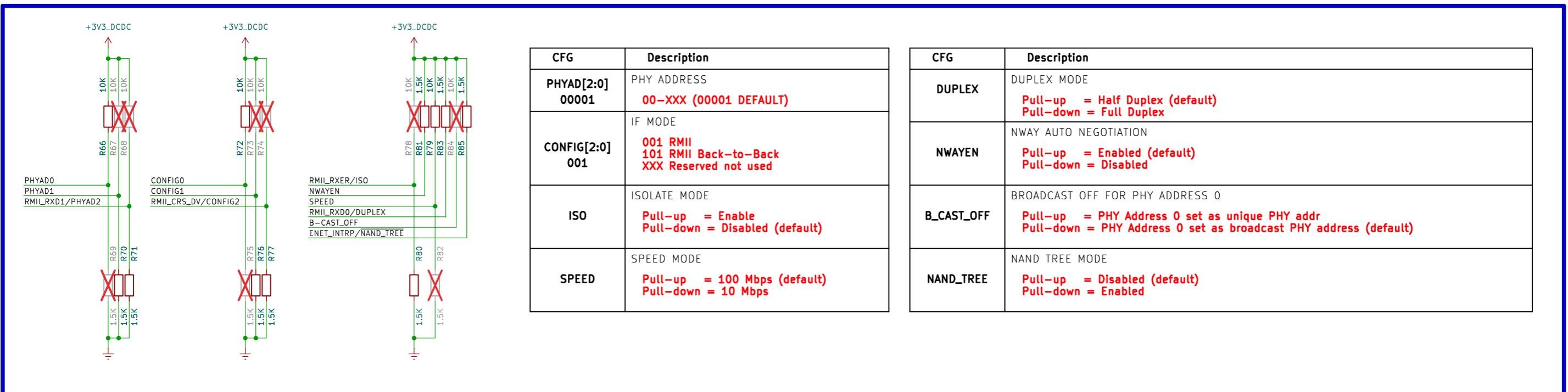
Date: 2026-02-16 Rev: 01

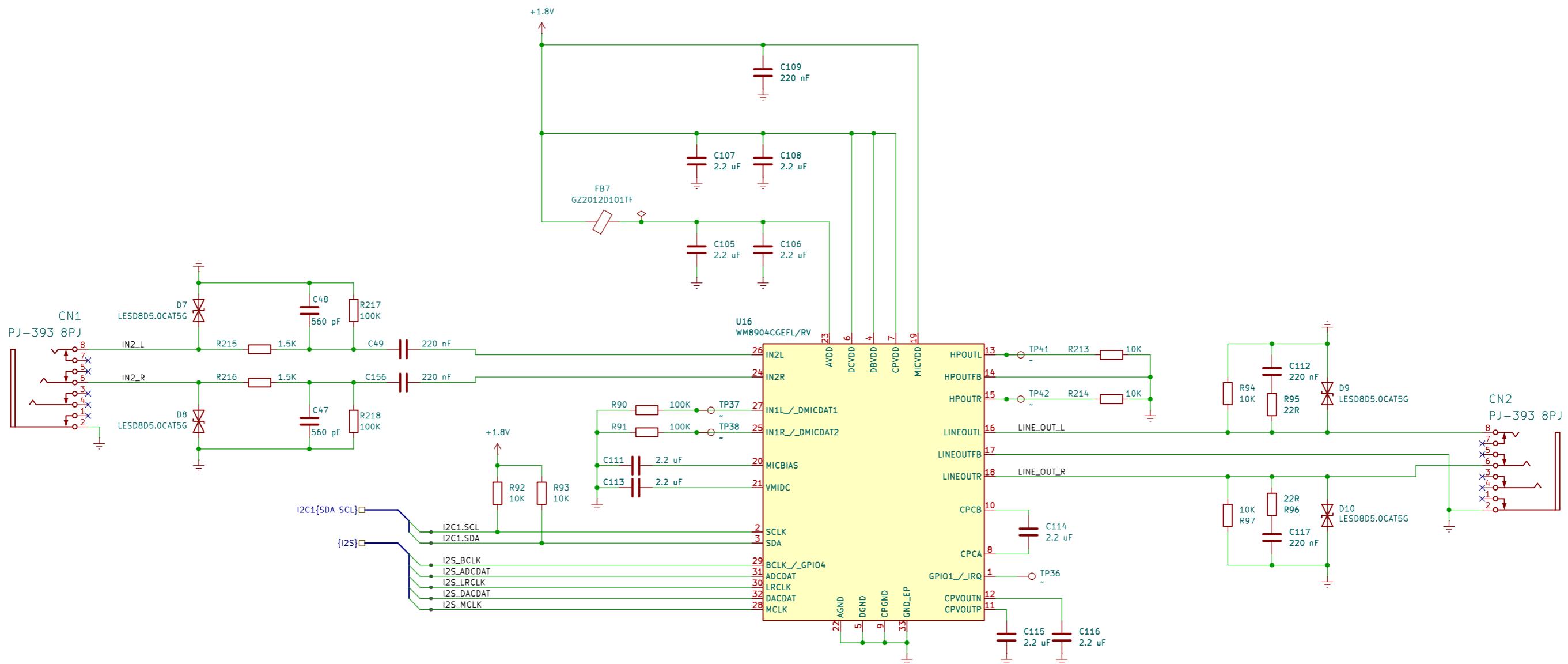
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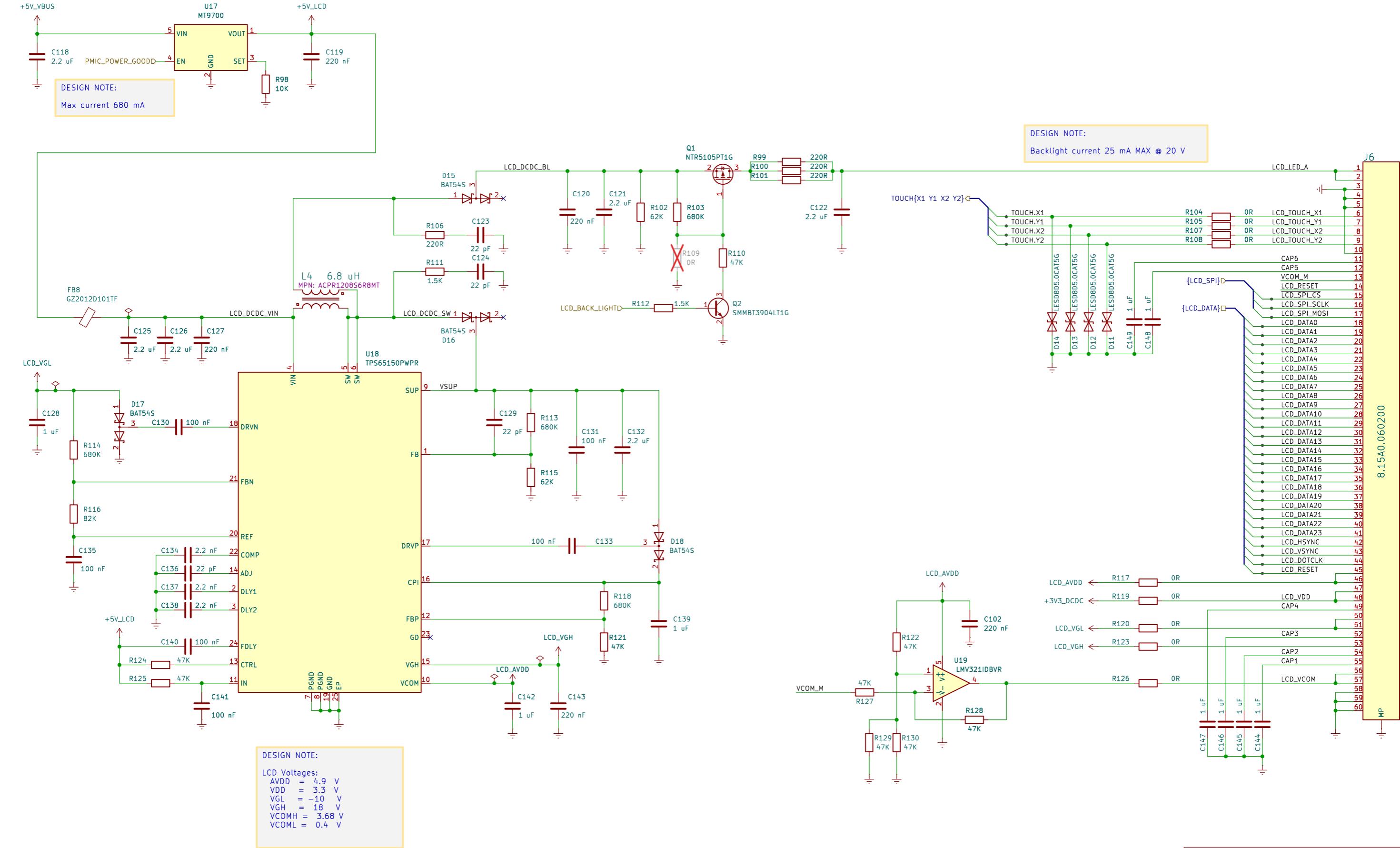


STRAPPING OPTIONS





LCD LOAD SWITCH



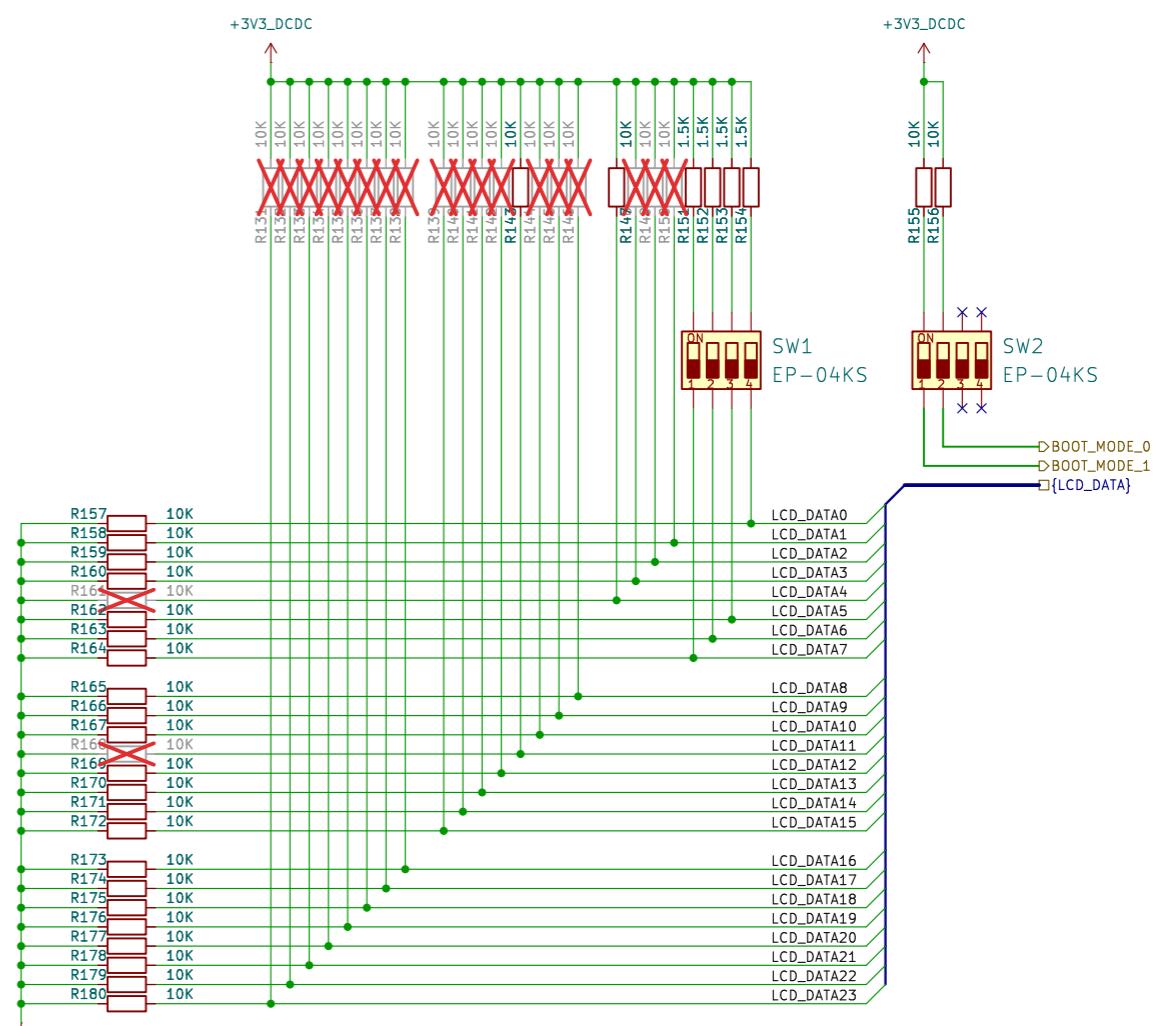
FUSE MAP <Default: QSPI BOOT>

	0/1	0/1	0/1	1	0	0	0	0	
A	TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved	DDR SMP: "000": Default "001-111"			
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved	
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved	
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	SD Power Cycle Enable: '0' - power cycle '1' - Enabled via USDHCRST pad (USDHC3 & 4 only)	SD Loopback Clock Source Select for SDR50 and SDR104 only: '0' - through SD pad '1' - direct		
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1 - Normal	Fast Boot Acknowledge Disable: 0 - Boot Ad. Enabled 1 - Boot Ad. Disabled	SD Loopback Clock Source Select for SDR50 and SDR104 only: '0' - No power cycle '1' - Enabled via USDHCRST pad (USDHC3 & 4 only)		
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved	Row Address Bytes: 00 - 3 01 - 2 10 - 4 11 - 5			

	0	0	0	0	1	0	0	0	
C	TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	HSPHS Half Speed Phase Selection 0 - selected sampling at non-inverted clock 1 - selected sampling at inverted clock	HSDLY Half Speed Delay selection 0 - one clock delay 1 - two clock delay	FSPIHS Full Speed Phase Selection 0 - selected sampling at non-inverted clock 1 - selected sampling at inverted clock	FSIDLY Full Speed Delay selection 0 - one clock delay 1 - two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved	
WEIM	Mixing Scheme: 00 - A/D16 01 - A/D4H 10 - A/DL 11 - Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved	
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved	
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit		Port Select: 00 - eSDH0 01 - eSDH1 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SDI VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	
MMC/eMMC	Bus Width: 00 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC44) 110 - 8-bit DDR (MMC44) B1 - reserved		Port Select: 00 - eSDH0 01 - eSDH1 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SDI VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved		
NAND	Toggle Mode: 32MHz Preable Delay, Read Latency: '000' - 16 GPMIOK cycles '001' - 1 GPMIOK cycles '010' - 2 GPMIOK cycles '011' - 3 GPMIOK cycles '100' - 4 GPMIOK cycles '101' - 5 GPMIOK cycles '110' - 6 GPMIOK cycles '111' - 7 GPMIOK cycles		BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time 0' - 12ms 1' - 22ms (L84 Nand)	Reserved		

	0	0	0	0	0	0	0	0	
D	TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CSselect (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)	Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved			
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved	
0x460	Reserved (DDR3 config options)								
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE '0' - Disabled '1' - Enabled	SIC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved	
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved		
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU_DISABLE	Override Pad Settings (using PAD_SETTINGS value)	
0x470	Reserved for unexpected requirements	EMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHCPAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_BMMC_22K_PULLUP 0 - 47k pullup 1 - 22k pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDHCIOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	USDHCIOMUX_SRE_ENABLE 0 - Disable 1 - Enable	
0x470	USDHCI_CMD_OE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR-Bus) 00 - LPB Disable 01 - 1 GPIO (def freq) 10 - Div by 2 11 - Div by 4		BT_LPB_POLARITY (GPIO polarity)	POWER_MNG_CFG (LDO's DCDCs) (Reserved - NOT USED)				
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.							

BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved



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File: BOOT_CONFIG.kicad_sch

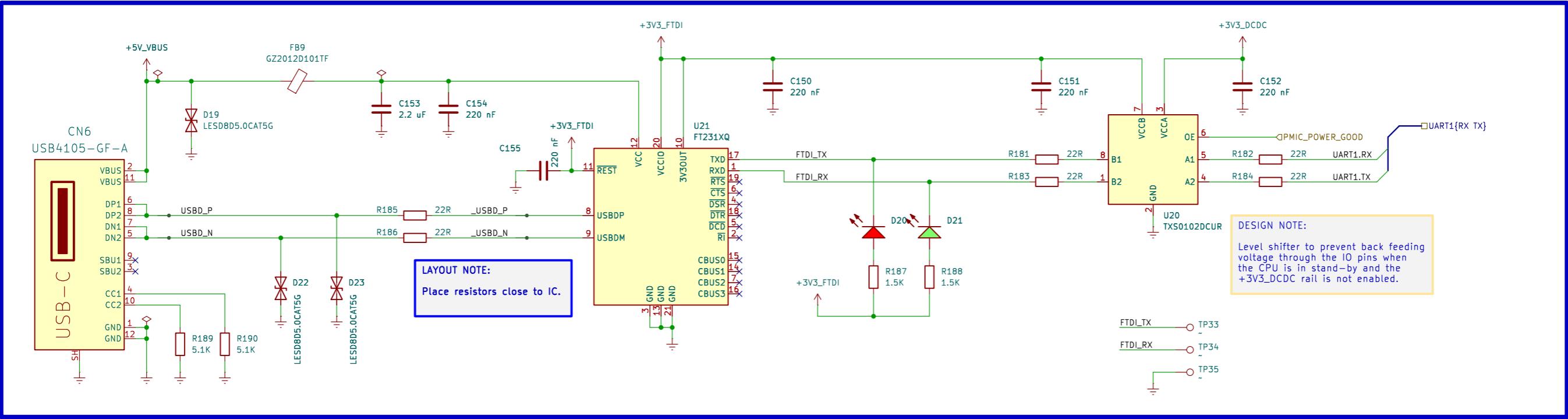
Author: ts-manuel

Date: 2026-02-16 Rev: 01

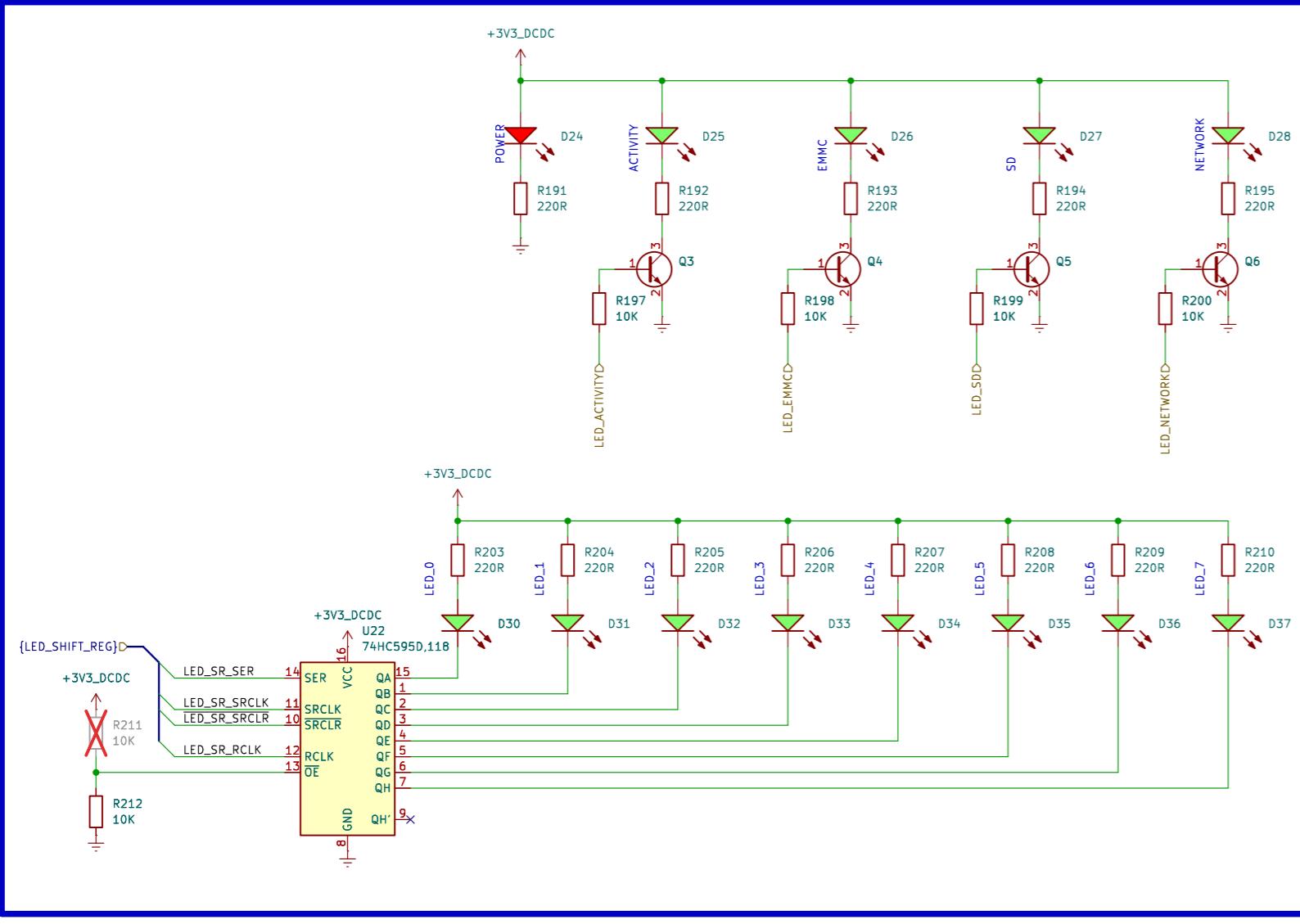
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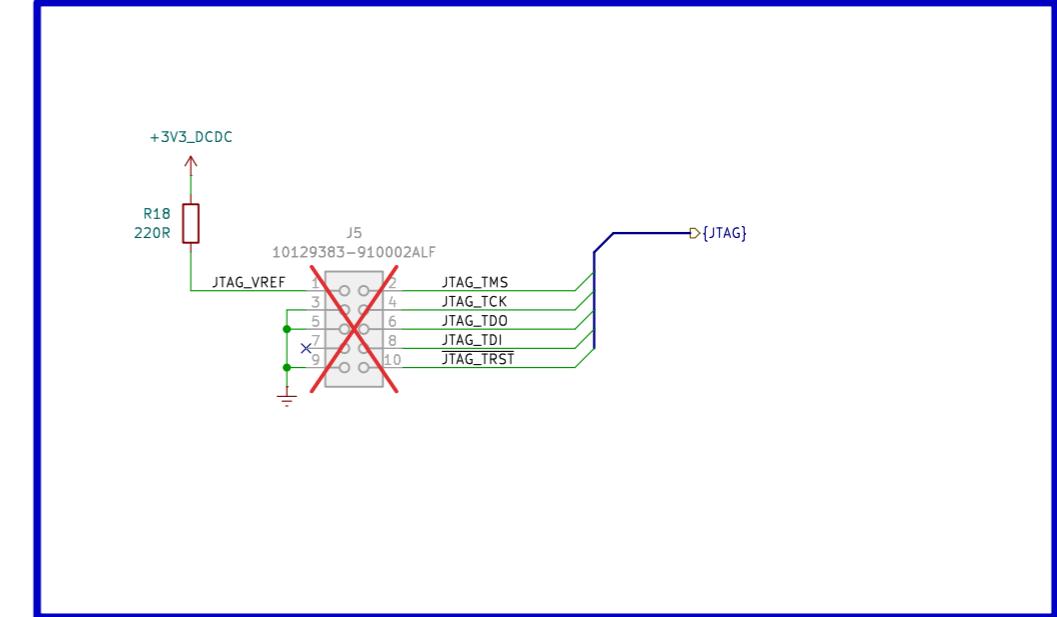
USB-C POWER & DEBUG UART



LEDs



JTAG



Title: i.MX6 Demo Board

File: CONTROL_GPIO.kicad_sch

Author: ts-manuel

Date: 2026-02-16 Rev: 01

KiCad E.D.A. 9.0.7 Size: A3 Id: 13/13

