i.MX6 Demo Board

Rev: 00 2024-05-26

INDEX:

PCB:

Number of Layers:	6
Thickness:	1.6 mm ±10%
Overall Dimensions:	80.00 x 70.00 mm
Silkscreen:	White
Solder Mask:	Green
Via Solder Tenting:	YES
Copper Finish:	ENIG
Min Track / Spacing:	0.12 mm / 0.12 mm
Min Hole Diameter:	0.20 mm

DESIGN CONSIDERATIONS

DESIGN NOTE:

Example text for informational design notes

DEBUG NOTE:

Example text for debug notes

DESIGN NOTE:

Example text for critical design notes

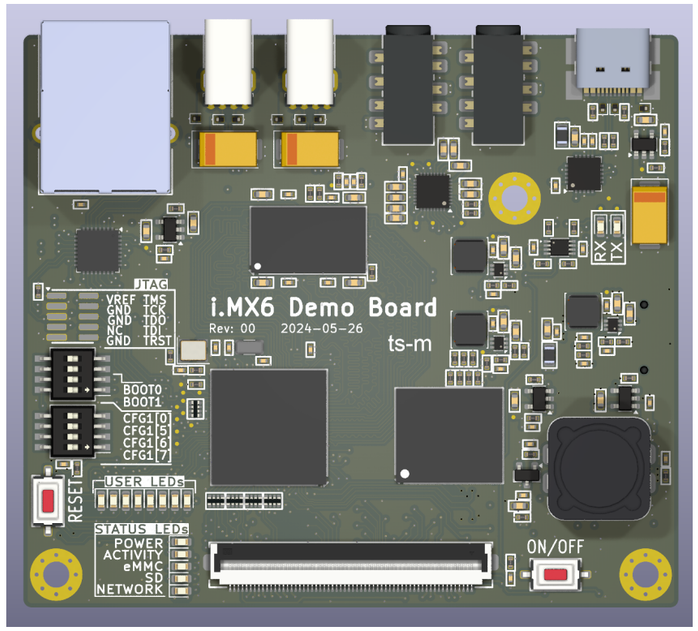
LAYOUT NOTE:

Example text for design notes

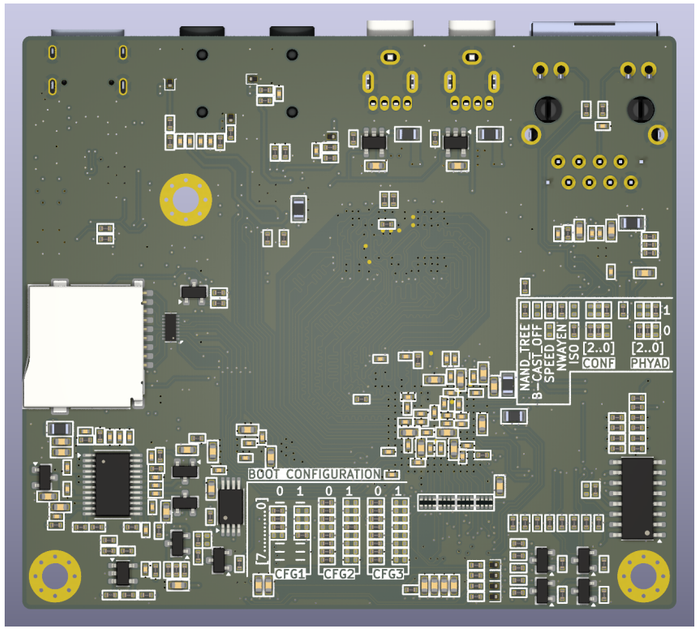
POWER TREE

i.MX6ULL MAIN

TOP VIEW

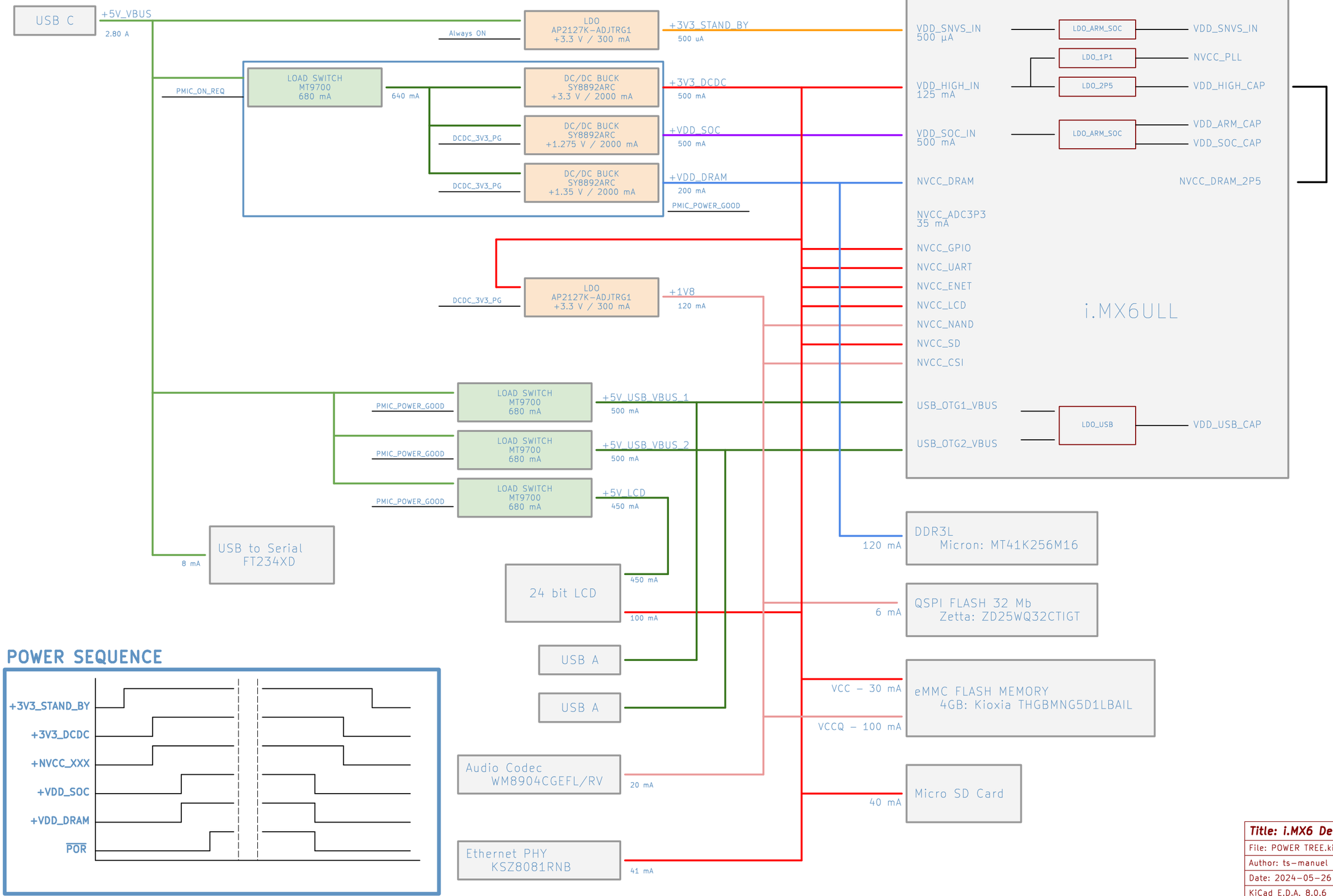


BOTTOM VIEW



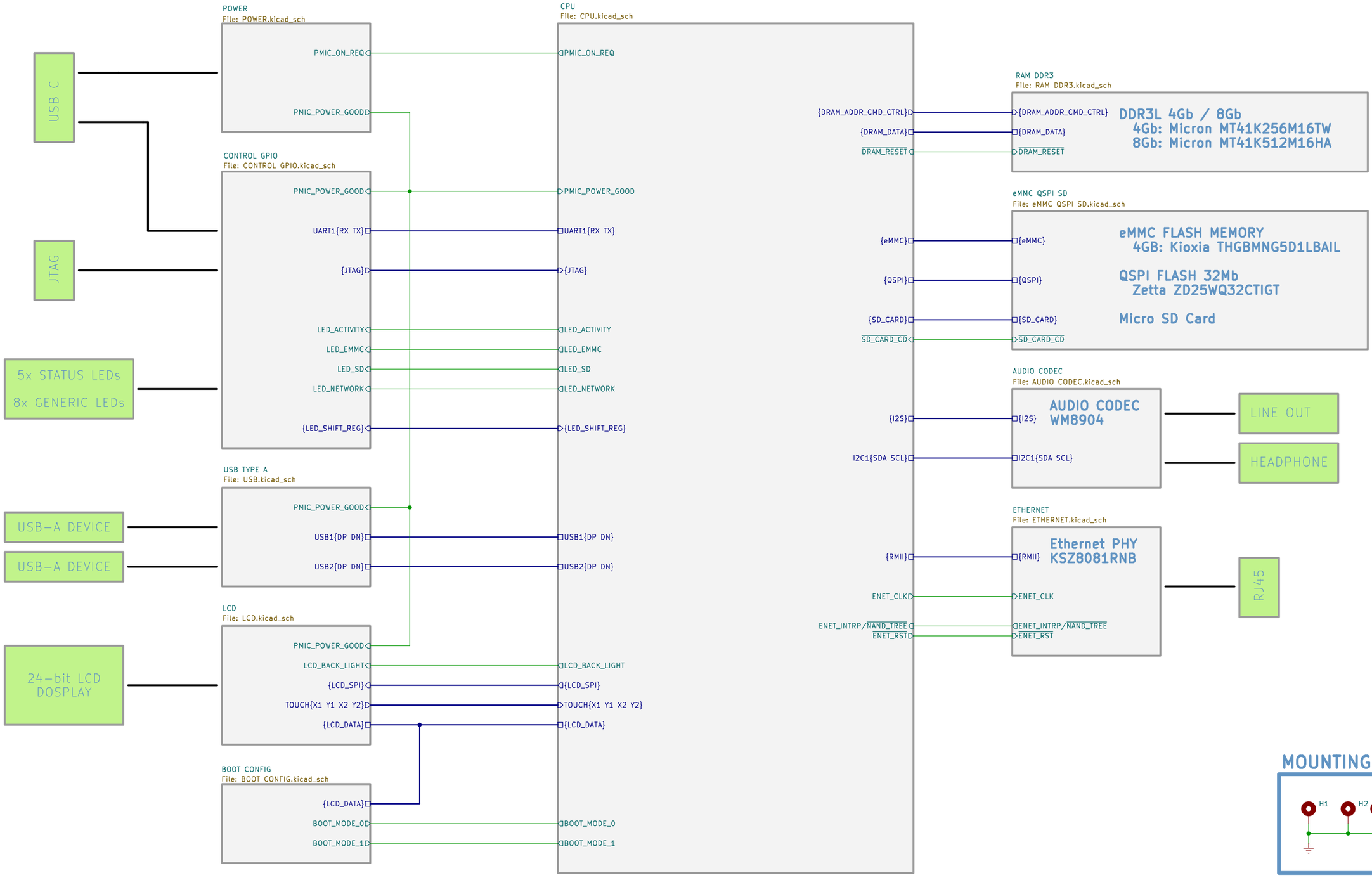
Title: i.MX6 Demo Board	
File: iMX6 Demo Board.kicad_sch	
Author: ts-manuel	
Date: 2024-05-26	Rev: 00
KiCad E.D.A. 8.0.6	Size: A3 Id: 1/13

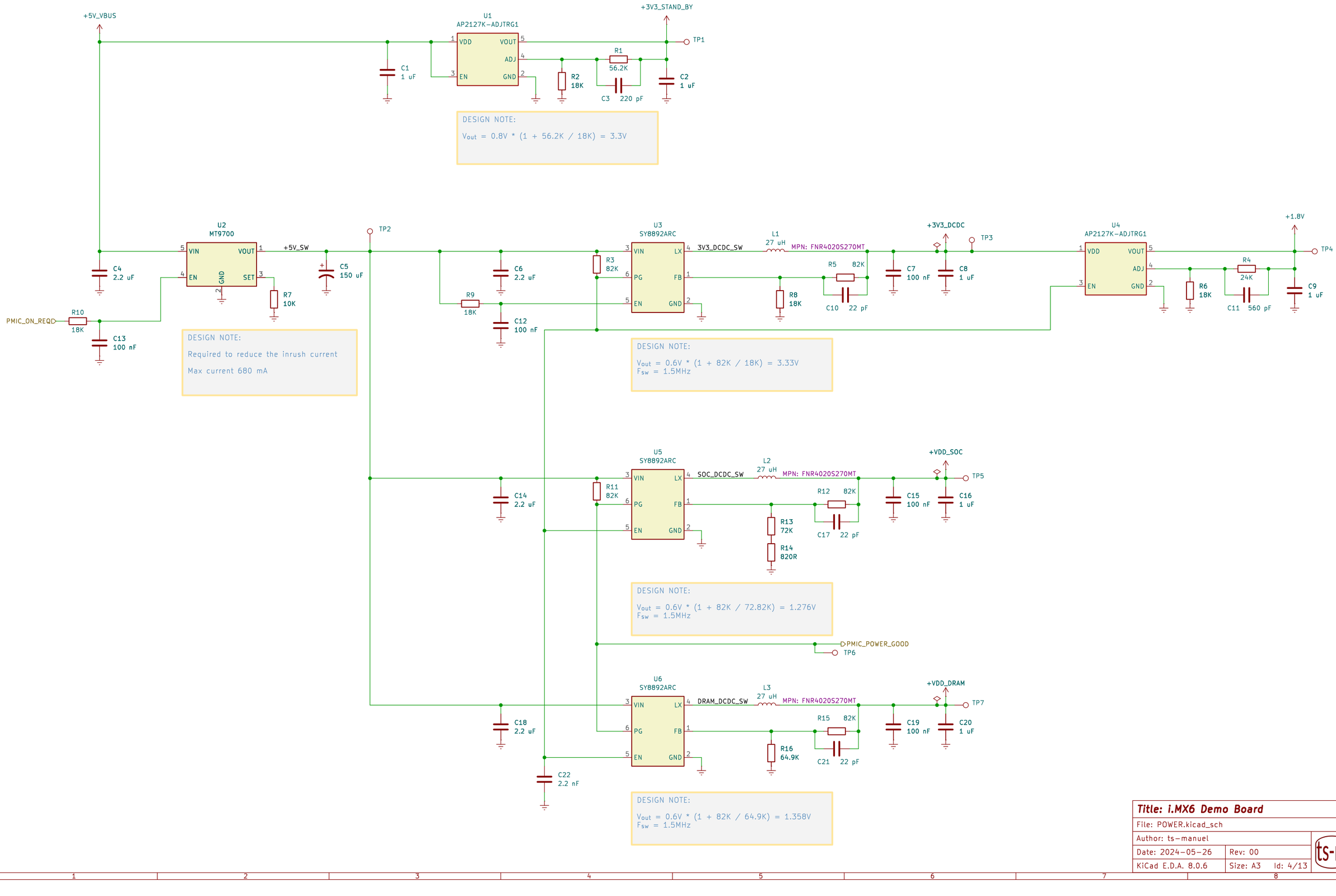
POWER TREE



POWER SEQUENCE

Title: i.MX6 Demo Board	
File: POWER TREE.kicad_sch	
Author: ts-manuel	
Date: 2024-05-26	Rev: 00
KiCad E.D.A. 8.0.6	Size: A3 Id: 2/13


POWER
File: POWER.kicad_sch
PMIC_ON_REQ
PMIC_POWER_GOOD
CPU
File: CPU.kicad_sch
PMIC_ON_REQ
PMIC_POWER_GOOD
USB C
CONTROL GPIO
File: CONTROL GPIO.kicad_sch
PMIC_POWER_GOOD
UART1{RX TX}
{JTAG}
LED_ACTIVITY
LED_EMMC
LED_SD
LED_NETWORK
{LED_SHIFT_REG}
JTAG
5x STATUS LEDs
8x GENERIC LEDs
USB TYPE A
File: USB.kicad_sch
PMIC_POWER_GOOD
USB1{DP DN}
USB2{DP DN}
USB-A DEVICE
USB-A DEVICE
LCD
File: LCD.kicad_sch
PMIC_POWER_GOOD
LCD_BACK_LIGHT
{LCD_SPI}
TOUCH{X1 Y1 X2 Y2}
{LCD_DATA}
24-bit LCD DOSPLAY
BOOT CONFIG
File: BOOT CONFIG.kicad_sch
{LCD_DATA}
BOOT_MODE_0
BOOT_MODE_1
UART1{RX TX}
{JTAG}
LED_ACTIVITY
LED_EMMC
LED_SD
LED_NETWORK
{LED_SHIFT_REG}
USB1{DP DN}
USB2{DP DN}
LCD_BACK_LIGHT
{LCD_SPI}
TOUCH{X1 Y1 X2 Y2}
{LCD_DATA}
BOOT_MODE_0
BOOT_MODE_1
{DRAM_ADDR_CMD_CTRL}
{DRAM_DATA}
DRAM_RESET
{eMMC}
{QSPI}
{SD_CARD}
SD_CARD_CD
{I2S}
I2C1{SDA SCL}
{RMII}
ENET_CLK
ENET_INTRP/NAND_TREE
ENET_RST
RAM DDR3
File: RAM DDR3.kicad_sch
{DRAM_ADDR_CMD_CTRL}
{DRAM_DATA}
DRAM_RESET
DDR3L 4Gb / 8Gb
4Gb: Micron MT41K256M16TW
8Gb: Micron MT41K512M16HA
eMMC QSPI SD
File: eMMC QSPI SD.kicad_sch
{eMMC}
{QSPI}
{SD_CARD}
SD_CARD_CD
eMMC FLASH MEMORY
4GB: Kioxia THGBMNG5D1LBAIL
QSPI FLASH 32Mb
Zetta ZD25WQ32CTIGT
Micro SD Card
AUDIO CODEC
File: AUDIO CODEC.kicad_sch
{I2S}
I2C1{SDA SCL}
AUDIO CODEC
WM8904
LINE OUT
HEADPHONE
ETHERNET
File: ETHERNET.kicad_sch
{RMII}
ENET_CLK
ENET_INTRP/NAND_TREE
ENET_RST
Ethernet PHY
KSZ8081RNB
RJ45
MOUNTING HOLES
H1
H2
H3
Title: i.MX6 Demo Board
File: i.MX6ULL MAIN.kicad_sch
Author: ts-manuel
Date: 2024-05-26
Rev: 00
KiCad E.D.A. 8.0.6
Size: A3
Id: 3/13
ts-m



Title: i.MX6 Demo Board		
File: POWER.kicad_sch		
Author: ts-manuel		
Date: 2024-05-26	Rev: 00	
KiCad E.D.A. 8.0.6	Size: A3 Id: 4/13	

POWER

U7A
MCIMX6Y2CVM08AB

i.MX6ULL – POWER

+VDD_SOC
C27 22 uF
C28 220 nF
C29 220 nF
C30 220 nF
H9 H10 J9 J10 K9 K10 VDD_SOC_IN
LDO_ARM_SOC
G9 G10 G11 H11 VDD_ARM_CAP
VDD_ARM_CAP
C23 220 nF
C24 220 nF
C25 22 uF
TP8
G8 H8 J8 J11 K8 K11 L8 L9 L10 L11 VDD_SOC_CAP
VDD_SOC_CAP
C31 220 nF
C32 220 nF
C33 220 nF
C34 22 uF
TP9

+3V3_DCDC
FB1
GZ2012D101TF
C37 22 uF
C38 220 nF
N13 VDD_HIGH_IN
LDO_2P5
LDO_1P1
R14 R15 VDD_HIGH_CAP
+VDD_HIGH_CAP
C35 220 nF
C36 10 uF
TP10
P13 NVCC_PLL
TP11

+3V3_STAND_BY
C41 220 nF
P12 VDD_SNVS_IN
LDO_SNVS
N12 VDD_SNVS_CAP
VDD_SNVS_CAP
C39 220 nF
C40 10 uF
TP12
C42 220 nF

+3V3_DCDC
FB2
GZ2012D101TF
C51 2.2 uF
C52 220 nF
L13 VDDA_ADC_3P3
M13 ADC_VREFH
M12 NGND_KELO
A1 A17 C3 C7 C11 C15 E8 E11 F6 F7 F8 F9 F10 F11 F12 G3 G5 G7 G12 G15 H7 H12 J5 VSS

U17 U14 U1 T14 R17 R16 R11 R7 R5 R3 N5 N3 M11 M10 M9 M8 M7 L12 L7 L3 K12 K7 J12 J7 VSS

DDR3

U7B
MCIMX6Y2CVM08AB

i.MX6ULL – DDR

{DRAM_ADDR_CMD_CTRL}
DRAM_A0 DRAM_A1 DRAM_A2 DRAM_A3 DRAM_A4 DRAM_A5 DRAM_A6 DRAM_A7 DRAM_A8 DRAM_A9 DRAM_A10 DRAM_A11 DRAM_A12 DRAM_A13 DRAM_A14 DRAM_A15
L5 H2 K1 M2 K4 L1 G2 H4 J4 L2 M4 K3 L4 H3 G1 K5 DRAM_ADDR00 DRAM_ADDR01 DRAM_ADDR02 DRAM_ADDR03 DRAM_ADDR04 DRAM_ADDR05 DRAM_ADDR06 DRAM_ADDR07 DRAM_ADDR08 DRAM_ADDR09 DRAM_ADDR10 DRAM_ADDR11 DRAM_ADDR12 DRAM_ADDR13 DRAM_ADDR14 DRAM_ADDR15
DRAM_BA0 DRAM_BA1 DRAM_BA2
M1 H1 K2 DRAM_SDBA0 DRAM_SDBA1 DRAM_SDBA2
DRAM_CS0 DRAM_CS1
N2 H5 DRAM_CS0 DRAM_CS1
DRAM_RAS DRAM_CAS DRAM_SDWE
M5 J2 J1 DRAM_RAS DRAM_CAS DRAM_SDWE

+VDD_DRAM
C43 10 uF
C44 220 nF
C45 220 nF
C46 220 nF
M6 L6 K6 J6 H6 G6 NVCC_DRAM
+VDD_HIGH_CAP
C53 220 nF
N6 NVCC_DRAM_2P5
DRAM_VREF
P4 DRAM_VREF
C54 220 nF

T4 U6 T6 U7 U8 T8 T5 U4 P6 P7 T7 DRAM_DATA00 DRAM_DATA01 DRAM_DATA02 DRAM_DATA03 DRAM_DATA04 DRAM_DATA05 DRAM_DATA06 DRAM_DATA07 DRAM_SDQS0_P DRAM_SDQS0_N DRAM_DQM0
DRAM_DATA0 DRAM_DATA1 DRAM_DATA2 DRAM_DATA3 DRAM_DATA4 DRAM_DATA5 DRAM_DATA6 DRAM_DATA7 DRAM_DQSL_P DRAM_DQSL_N DRAM_DML
U2 U3 U5 R4 P5 P3 R2 R1 T1 T2 T3 DRAM_DATA08 DRAM_DATA09 DRAM_DATA10 DRAM_DATA11 DRAM_DATA12 DRAM_DATA13 DRAM_DATA14 DRAM_DATA15 DRAM_SDQS1_P DRAM_SDQS1_N DRAM_DQM1
DRAM_DATA8 DRAM_DATA15 DRAM_DATA10 DRAM_DATA13 DRAM_DATA12 DRAM_DATA11 DRAM_DATA14 DRAM_DATA9 DRAM_DQSU_P DRAM_DQSU_N DRAM_DMU
{DRAM_DATA}

M3 J3 DRAM_SDCKE0 DRAM_SDCKE1
P1 P2 DRAM_SDCLK0_P DRAM_SDCLK0_N
F1 N1 DRAM_ODT1 DRAM_ODT0
G4 DRAM_RESET
N4 DRAM_ZQPAD
R17 240R 1%
DRAM_CLK_EN0 DRAM_CLK_EN1 DRAM_CLK_P DRAM_CLK_N DRAM_ODT1 DRAM_ODT0
{DRAM_ADDR_CMD_CTRL}
DRAM_RESET

eMMC QSPI SD

U7C
MCIMX6Y2CVM08AB

i.MX6ULL – NAND

+1.8V
C26 220 nF
E7 NVCC_NAND
C5 NAND_CE0
B5 NAND_CE1
B4 NAND_ALE
A4 NAND_CLE
D8 NAND_RE
C8 NAND_WE
D5 NAND_WP
A3 NAND_READY
E6 NAND_DQS
D7 B7 A7 B6 C6 B6 A6 A5 NAND_DATA00 NAND_DATA01 NAND_DATA02 NAND_DATA03 NAND_DATA04 NAND_DATA05 NAND_DATA06 NAND_DATA07
eMMC_RESET eMMC_CLK eMMC_CMD QSPI_DATA3 QSPI_SCLK QSPI_DATA0 QSPI_CS eMMC_DATA0 eMMC_DATA1 eMMC_DATA2 eMMC_DATA3 eMMC_DATA4 eMMC_DATA5 eMMC_DATA6 eMMC_DATA7
{eMMC} {QSPI}
QSPI_DATA1 QSPI_DATA2

U7I
MCIMX6Y2CVM08AB

i.MX6ULL – SD

+3V3_DCDC
C50 220 nF
C4 NVCC_SD1
C1 SD1_CLK
C2 SD1_CMD
B3 SD1_DATA0
B2 SD1_DATA1
B1 SD1_DATA2
A2 SD1_DATA3
SD_CARD_SCLK SD_CARD_CMD SD_CARD_DATA0 SD_CARD_DATA1 SD_CARD_DATA2 SD_CARD_DATA3
{SD_CARD}

CONTROL

DESIGN NOTE:
RESET Output remains low while V CC is below the reset threshold [2.63V], and for at least 140ms after VCC rises above the reset threshold

+3V3_DCDC
R23 10K
R24 10K
U8
UM803RS
VCC RESET GND
3 2 1
R21 0R
PMIC_POWER_GOOD
R22 1.5K
PB1
PB2
C57 100 nF
C58 100 nF

U7J
MCIMX6Y2CVM08AB

i.MX6ULL – CONTROL

ONOFF R8
POR P8
BOOT_MODE_0 T10
BOOT_MODE_1 U10
R25 0R N7
TEST_MODE
SNVS_TAMPER0 R10
SNVS_TAMPER1 R9
SNVS_TAMPER2 P11
SNVS_TAMPER3 P10
SNVS_TAMPER4 P9
SNVS_TAMPER5 N8
SNVS_TAMPER6 N11
SNVS_TAMPER7 N10
SNVS_TAMPER8 N9
SNVS_TAMPER9 R6
ENET_INTRP/NAND_TREE
R26 22R
TP16 U9
PMIC_ON_REQ T9
CCM_PMIC_STBY_REQ
SNVS_PMIC_ON_REQ
VDD_SNVS_IN

R39 220R
R40 1M
Y1 24 MHz
C65 22 pF
C66 22 pF
T17 XTAL_O
T16 XTAL_I
NVCC_PLL

U11 RTC_XTAL_O
T11 RTC_XTAL_I
Y2 32.768 KHz
C67 22 pF
C68 22 pF
VDD_SNVS_CAP

R13 GPANIO
VDD_HIGH_IN

NVCC_GPIO
JTAG_TCK M14
JTAG_TMS P14
JTAG_TDI N16
JTAG_TDO N15
JTAG_TRST_B N14
JTAG_MOD P15
{JTAG}
R29 10K
CCM_CLK1_P P17
CCM_CLK1_N P16
TP13
TP14
TP15
VDD_HIGH_CAP

+3V3_DCDC
NVCC_UART H13
UART1_TX_DATA K14
UART1_RX_DATA K16
UART1_RTS J14
UART1_CTS K15
UART1{RX TX}
SD_CARD_CD
UART2
UART2_TX_DATA J17
UART2_RX_DATA J16
UART2_RTS H13
UART2_CTS J15
TP17
TP18
LED_NETWORK
UART3_TX_DATA H17
UART3_RX_DATA H16
UART3_RTS G14
UART3_CTS H15
LED_SD
LED_EMMC
LED_ACTIVITY
LED_BACK_LIGHT
UART4_TX_DATA G17
UART4_RX_DATA G16
LED_SR_RCLK
LED_SR_SRCLR
UART5_TX_DATA F17
UART5_RX_DATA G13
LED_SR_SRCLK
LED_SR_SER
{LED_SHIFT_REG}
NVCC_UART

PERIPHERALS

U7D
MCIMX6Y2CVM08AB

i.MX6ULL – CSI

+1.8V
C56 220 nF
F4 NVCC_CSI
F5 E5 F2 F3 E4 E3 E2 E1 D4 D3 D2 D1 CSI_MCLK CSI_PIXCLK CSI_VSYNC CSI_HSYNC CSI_DATA00 CSI_DATA01 CSI_DATA02 CSI_DATA03 CSI_DATA04 CSI_DATA05 CSI_DATA06 CSI_DATA07
I2C1.SDA I2C1.SCL I2S_MCLK I2S_LRCLK I2S_BCLK I2S_ADCDAT I2S_DACDAT
{I2C1{SDA SCL}
{I2S}

U7H
MCIMX6Y2CVM08AB

i.MX6ULL – USB

+5V_VBUS_USB1
C55 220 nF
T12 USB_OTG1_VBUS
LDO_USB
R12 VDD_USB_CAP
+5V_VBUS_USB2
C59 220 nF
U12 USB_OTG2_VBUS
U15 T15 U16 USB_OTG1_DP USB_OTG1_DN USB_OTG1_CHD
U13 T13 USB_OTG2_DP USB_OTG2_DN
USB1.DP USB1.DN USB2.DP USB2.DN
{USB1{DP DN}
{USB2{DP DN}
C60 220 nF
C61 22 uF

U7G
MCIMX6Y2CVM08AB

i.MX6ULL – LCD

+3V3_DCDC
C63 1 uF
C64 220 nF
E13 NVCC_LCD
A8 RN10D 4 5 22R LCD_DOTCLK
LCD_CLK
B8 LCD_ENABLE
D9 RN13D 4 5 22R LCD_HSYNC
C9 RN10C 3 6 22R LCD_VSYNC
E9 RN10B 2 7 22R LCD_RESET
LCD_HSYNC LCD_VSYNC LCD_RESET
B9 RN9B 7 2 22R LCD_DATA0
A9 RN9C 6 3 22R LCD_DATA1
E10 RN13B 2 7 22R LCD_DATA2
D10 RN13C 3 6 22R LCD_DATA3
C10 RN10A 1 8 22R LCD_DATA4
B10 RN14D 5 4 22R LCD_DATA5
A10 RN9A 8 1 22R LCD_DATA6
D11 RN13A 1 8 22R LCD_DATA7
B11 RN14B 7 2 22R LCD_DATA8
A11 RN14C 6 3 22R LCD_DATA9
E12 RN15C 3 6 22R LCD_DATA10
D12 RN15A 1 8 22R LCD_DATA11
C12 RN15D 4 5 22R LCD_DATA12
B12 RN16D 5 4 22R LCD_DATA13
A12 RN14A 8 1 22R LCD_DATA14
D13 RN11C 3 6 22R LCD_DATA15
C13 RN15B 2 7 22R LCD_DATA16
B13 RN16B 7 2 22R LCD_DATA17
A13 RN16C 6 3 22R LCD_DATA18
D14 RN11B 2 7 22R LCD_DATA19
C14 RN11D 4 5 22R LCD_DATA20
B14 RN12D 5 4 22R LCD_DATA21
A14 RN16A 8 1 22R LCD_DATA22
B16 RN12A 8 1 22R LCD_DATA23
RN9D 6 8 22R
{LCD_DATA}

U7F
MCIMX6Y2CVM08AB

i.MX6ULL – ENET

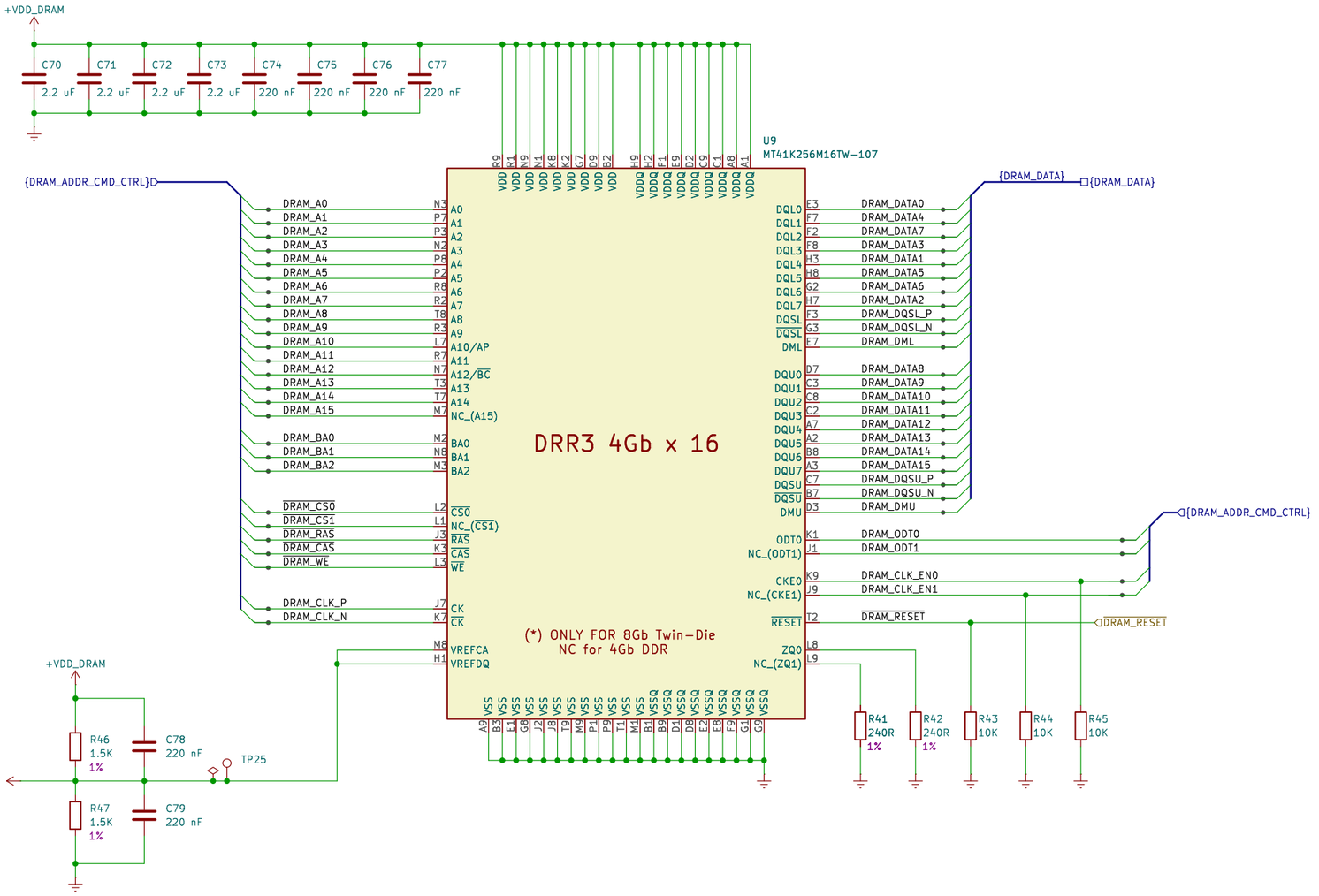
+3V3_DCDC
C62 220 nF
F13 NVCC_ENET
R38 22R
ENET_CLK
{RMII}
E15 E14 F15 F14 F16 E17 D15 E16 ENET1_TX_DATA0 ENET1_TX_DATA1 ENET1_TX_EN ENET1_TX_CLK ENET1_RX_DATA0 ENET1_RX_DATA1 ENET1_RX_ER ENET1_RX_EN
RMII_TXD0 RMII_TXD1 RMII_TXEN RMII_RXD0/DUPLEX RMII_RXD1/PHYAD2 RMII_RXER/ISO RMII_CRS_DV/CONFIG2
A15 A16 B15 D17 C17 C16 D16 B17 ENET2_TX_DATA0 ENET2_TX_DATA1 ENET2_TX_EN ENET2_TX_CLK ENET2_RX_DATA0 ENET2_RX_DATA1 ENET2_RX_ER ENET2_RX_EN
RN12B 7 2 22R
RN12C 6 3 22R
RMII_MDIO RMII_MDC
RN11A 1 8 22R
LCD_SPI_SCLK LCD_SPI_MOSI LCD_SPI_CS
{LCD_SPI}

U7E
MCIMX6Y2CVM08AB

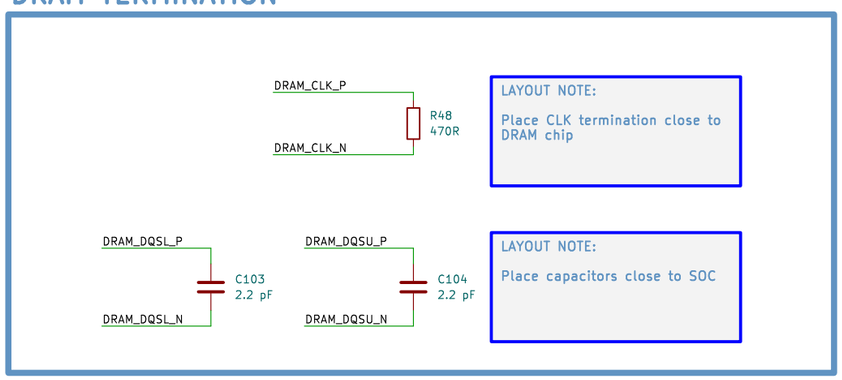
i.MX6ULL – GPIO

+3V3_DCDC
C69 220 nF
J13 NVCC_GPIO
K13 L15 L14 L17 M16 M17 K17 L16 N17 M15 GPIO1_IO00 GPIO1_IO01 GPIO1_IO02 GPIO1_IO03 GPIO1_IO04 GPIO1_IO05 GPIO1_IO06 GPIO1_IO07 GPIO1_IO08 GPIO1_IO09
TOUCH.Y1 TOUCH.Y2 TOUCH.X1 TOUCH.X2
RN1C 3 6 22R
RN1A 1 8 22R
RN1D 4 5 22R
RN1B 2 7 22R
{TOUCH{X1 Y1 X2 Y2}
TP20 TP21 TP22 TP23 TP24
ENET_RST

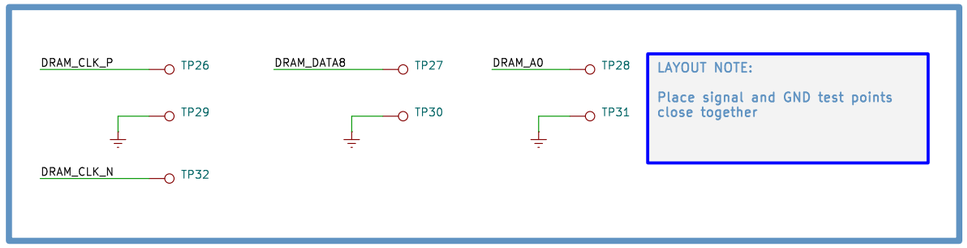
Title: i.MX6 Demo Board	
File: CPU.kicad_sch	
Author: ts-manuel	
Date: 2024-05-26	Rev: 00
KiCad E.D.A. 8.0.6	Size: A2 Id: 5/13



DRAM TERMINATION

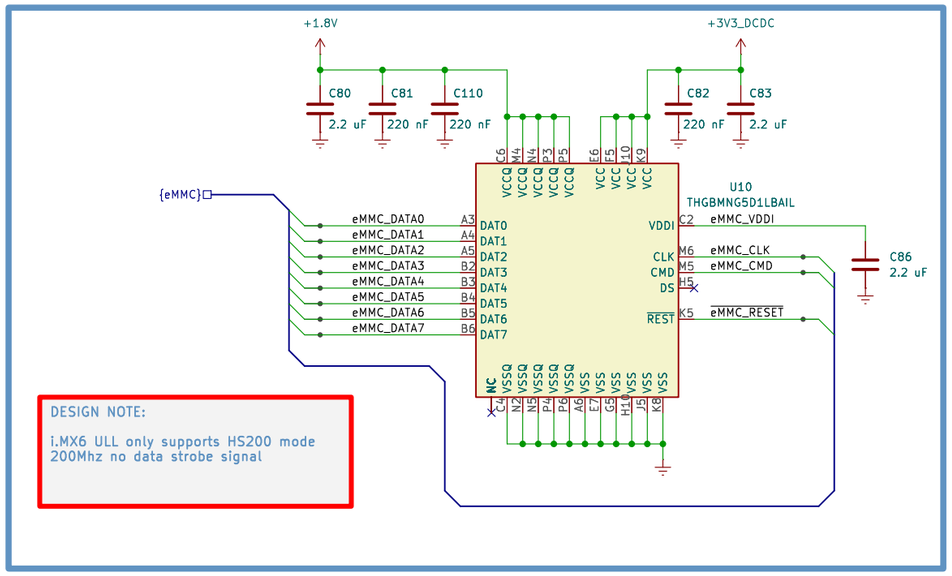


DRAM TEST POINTS

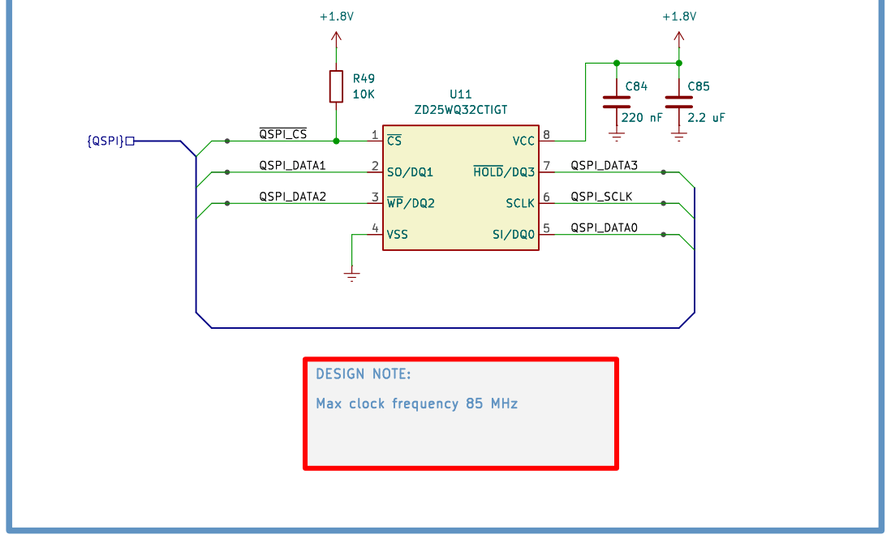


Title: i.MX6 Demo Board	
File: RAM DDR3.kicad_sch	
Author: ts-manuel	
Date: 2024-05-26	Rev: 00
KiCad E.D.A. 8.0.6	Size: A3 Id: 6/13

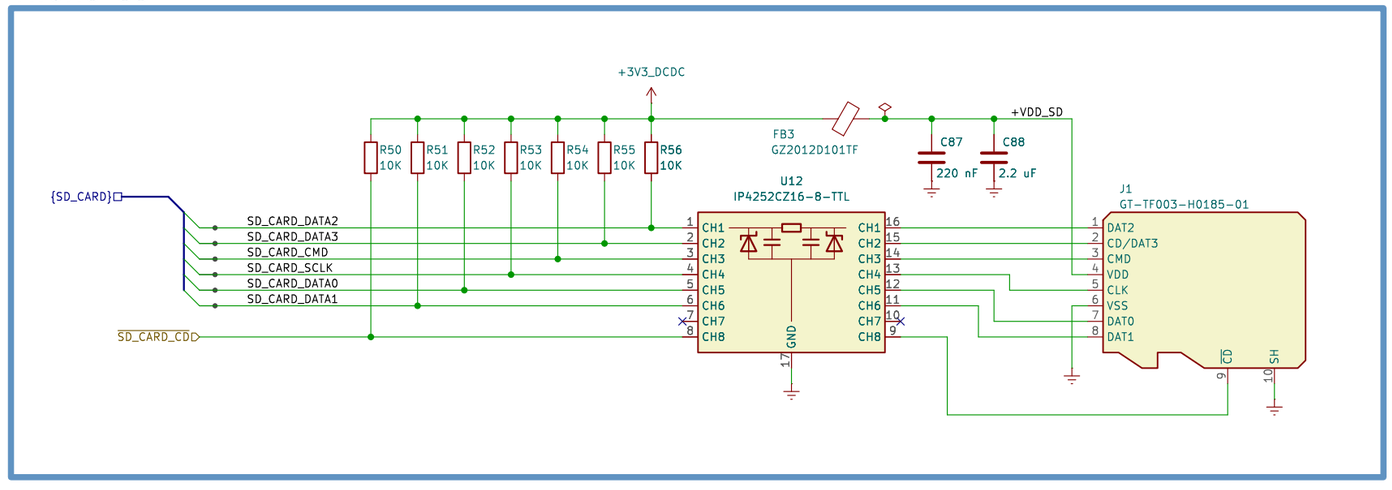
eMMC



QSPI

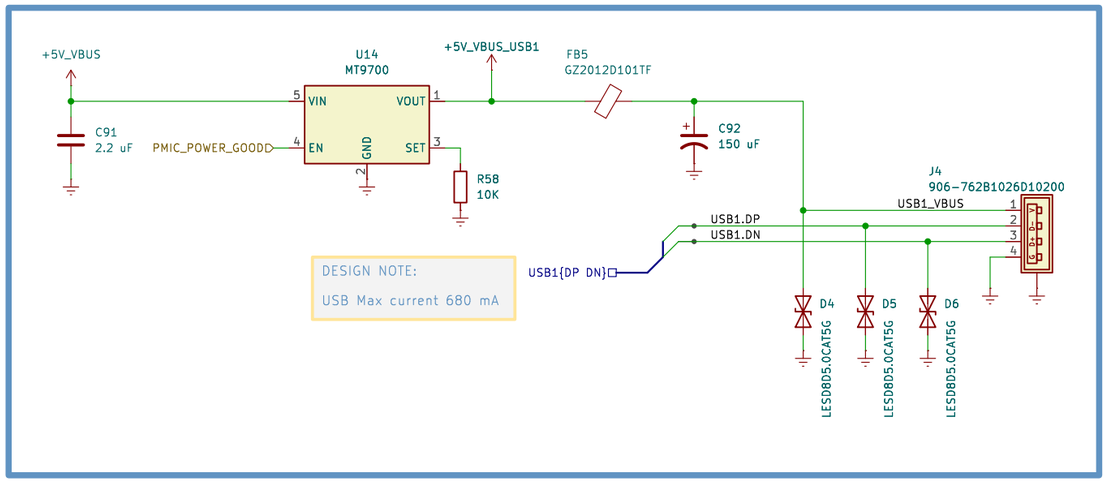


MICRO SD

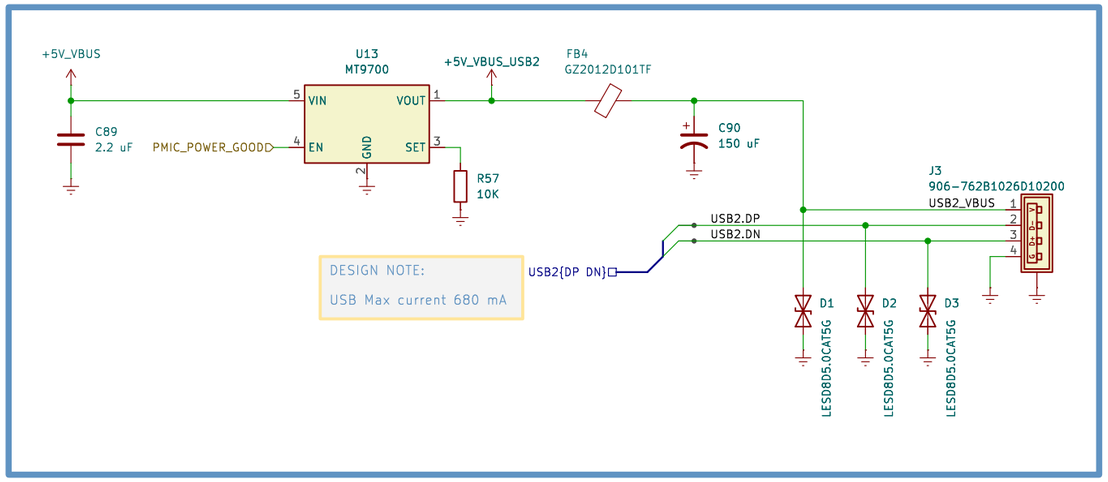


Title: i.MX6 Demo Board		
File: eMMC QSPI SD.kicad_sch		
Author: ts-manuel		
Date: 2024-05-26	Rev: 00	
KiCad E.D.A. 8.0.6	Size: A3	Id: 7/13

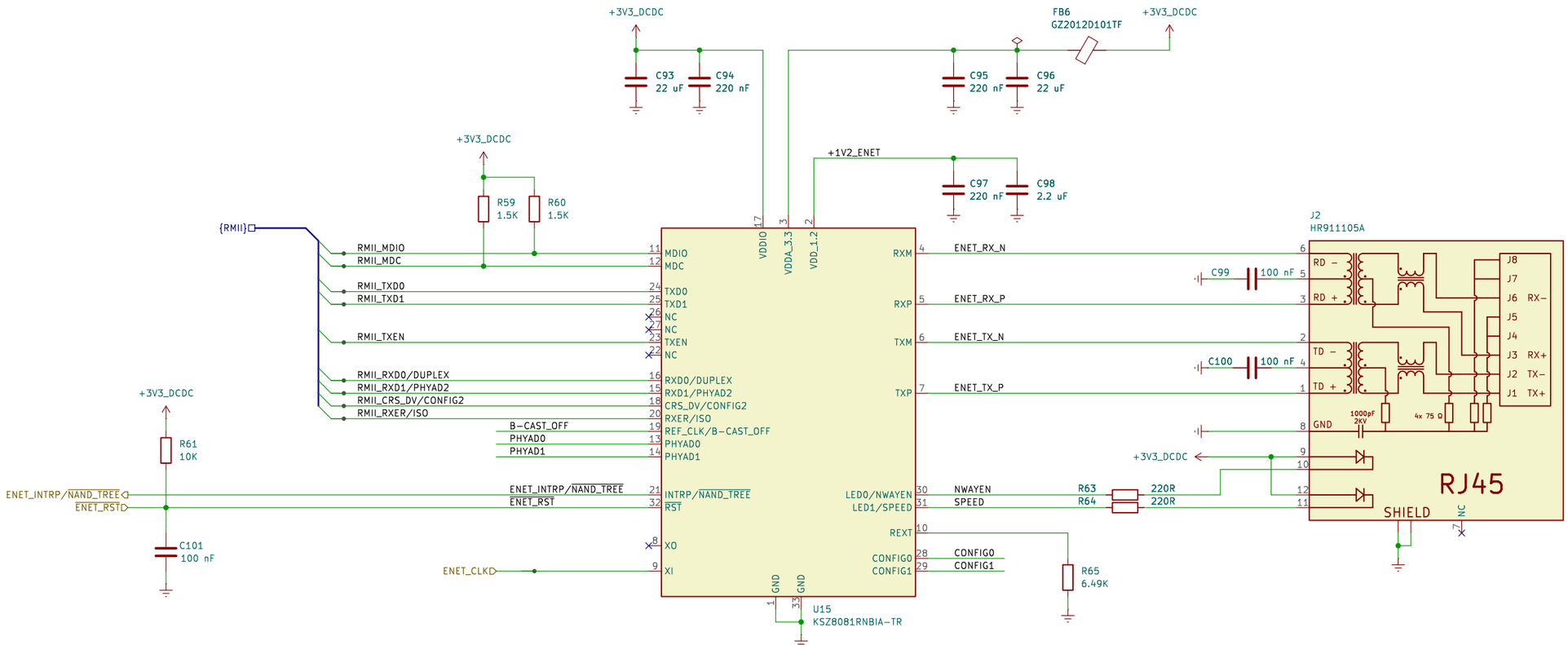
USB1



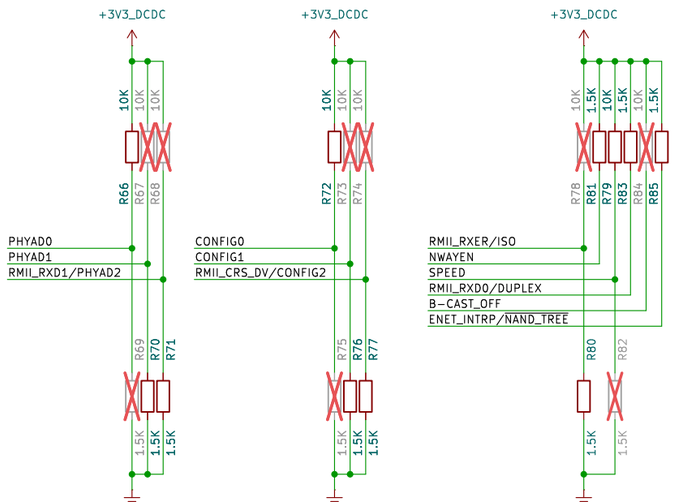
USB2



Title: i.MX6 Demo Board		
File: USB.kicad_sch		
Author: ts-manuel		
Date: 2024-05-26	Rev: 00	
KiCad E.D.A. 8.0.6	Size: A3 Id: 8/13	



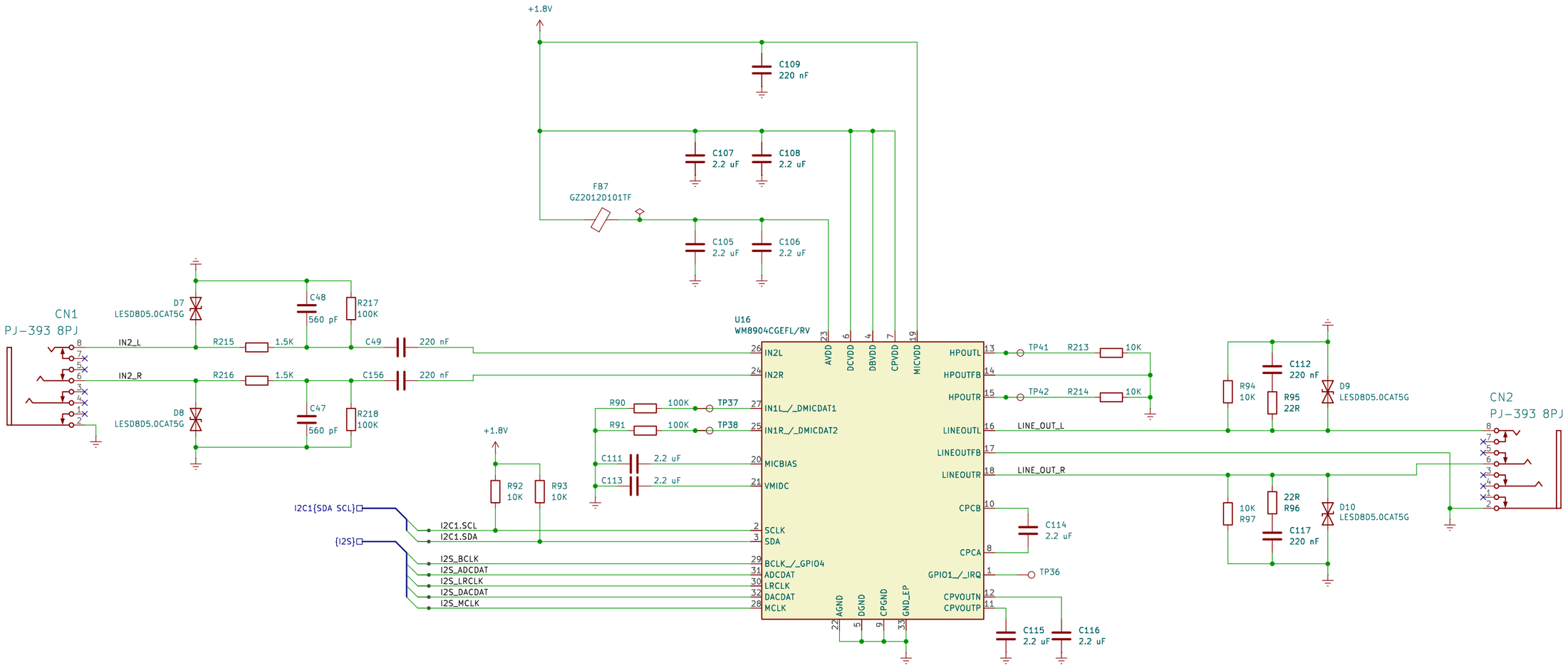
STRAPPING OPTIONS



CFG	Description
PHYAD[2:0] **00001**	PHY ADDRESS 00-XXX (00001 DEFAULT)
CONFIG[2:0] **001**	IF MODE 001 RMII 101 RMII Back-to-Back XXX Reserved not used
ISO	ISOLATE MODE Pull-up = Enable Pull-down = Disabled (default)
SPEED	SPEED MODE Pull-up = 100 Mbps (default) Pull-down = 10 Mbps

CFG	Description
DUPLEX	DUPLEX MODE Pull-up = Half Duplex (default) Pull-down = Full Duplex
NWAYEN	NWAY AUTO NEGOTIATION Pull-up = Enabled (default) Pull-down = Disabled
B_CAST_OFF	BROADCAST OFF FOR PHY ADDRESS 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down = PHY Address 0 set as broadcast PHY address (default)
NAND_TREE	NAND TREE MODE Pull-up = Disabled (default) Pull-down = Enabled

Title: i.MX6 Demo Board	
File: ETHERNET.kicad_sch	
Author: ts-manuel	
Date: 2024-05-26	Rev: 00
KiCad E.D.A. 8.0.6	Size: A3 Id: 9/13



Title: i.MX6 Demo Board	
File: AUDIO CODEC.kicad_sch	
Author: ts-manuel	
Date: 2024-05-26	Rev: 00
KiCad E.D.A. 8.0.6	Size: A3 Id: 10/13

LCD LOAD SWITCH

+5V_VBUS
U17
MT9700
VIN
VOUT
EN
GND
SET
C118
2.2 uF
PMIC_POWER_GOOD
C119
220 nF
R98
10K
+5V_LCD

DESIGN NOTE:
Max current 680 mA

DESIGN NOTE:
Backlight current 25 mA MAX @ 20 V

Q1
NTR5105PT1G
R99
R100
R101
220R
220R
220R
LCD_DCDC_BL
LCD_LED_A
J6
D15
BAT54S
C120
220 nF
C121
2.2 uF
R102
62K
R103
680K
C122
2.2 uF
R106
220R
C123
22 pF
R111
1.5K
C124
22 pF
R109
0R
R110
47K
L4 6.8 uH
MPN: ACPR1208S6R8MT
FB8
GZ2012D101TF
LCD_DCDC_VIN
LCD_DCDC_SW
LCD_BACK_LIGHT
R112
1.5K
Q2
SMMBT3904LT1G
BAT54S
D16
C125
2.2 uF
C126
2.2 uF
C127
220 nF
U18
TPS65150PWPR
VIN
SW
SW
SUP
VSUP
LCD_VGL
C128
1 uF
D17
BAT54S
C130
100 nF
DRVN
C129
22 pF
R113
680K
C131
100 nF
C132
2.2 uF
FB
R115
62K
R114
680K
FBN
R116
82K
REF
C135
100 nF
C134
2.2 nF
C136
22 pF
C137
2.2 nF
C138
2.2 nF
COMP
ADJ
DLY1
DLY2
DRVP
C133
100 nF
D18
BAT54S
CPI
R118
680K
C139
1 uF
FBP
R121
47K
GD
LCD_VGH
+5V_LCD
C140
100 nF
R124
47K
R125
47K
FDLY
CTRL
IN
VGH
VCOM
LCD_AVDD
C141
100 nF
PGND
PGND
GND
EP
C142
1 uF
C143
220 nF

TOUCH{X1 Y1 X2 Y2}
TOUCH.X1
TOUCH.Y1
TOUCH.X2
TOUCH.Y2
R104
R105
R107
R108
0R
0R
0R
0R
LCD_TOUCH_X1
LCD_TOUCH_Y1
LCD_TOUCH_X2
LCD_TOUCH_Y2
LESDB05.0CAT5G
D14
D13
D12
D11
C149
1 uF
C148
1 uF
{LCD_SPI}
{LCD_DATA}
CAP6
CAP5
VCOM_M
LCD_RESET
LCD_SPI_CS
LCD_SPI_SCLK
LCD_SPI_MOSI
LCD_DATA0
LCD_DATA1
LCD_DATA2
LCD_DATA3
LCD_DATA4
LCD_DATA5
LCD_DATA6
LCD_DATA7
LCD_DATA8
LCD_DATA9
LCD_DATA10
LCD_DATA11
LCD_DATA12
LCD_DATA13
LCD_DATA14
LCD_DATA15
LCD_DATA16
LCD_DATA17
LCD_DATA18
LCD_DATA19
LCD_DATA20
LCD_DATA21
LCD_DATA22
LCD_DATA23
LCD_HSYNC
LCD_VSYNC
LCD_DOTCLK
LCD_RESET
8.15A0.060200
MP

LCD_AVDD
C102
220 nF
R122
47K
U19
LMV321IDBVR
V+
V-
VCOM_M
47K
R127
R128
47K
R129
47K
R130
47K
LCD_AVDD
+3V3_DCDC
LCD_VGL
LCD_VGH
R117
R119
R120
R123
R126
0R
0R
0R
0R
0R
LCD_VDD
CAP4
CAP3
CAP2
CAP1
LCD_VCOM
C147
1 uF
C146
1 uF
C145
1 uF
C144
1 uF

DESIGN NOTE:

LCD Voltages:
AVDD = 4.9 V
VDD = 3.3 V
VGL = −10 V
VGH = 18 V
VCOMH = 3.68 V
VCOML = 0.4 V

Title: i.MX6 Demo Board	
File: LCD.kicad_sch	
Author: ts−manuel	
Date: 2024−05−26	Rev: 00
KiCad E.D.A. 8.0.6	Size: A3 Id: 11/13

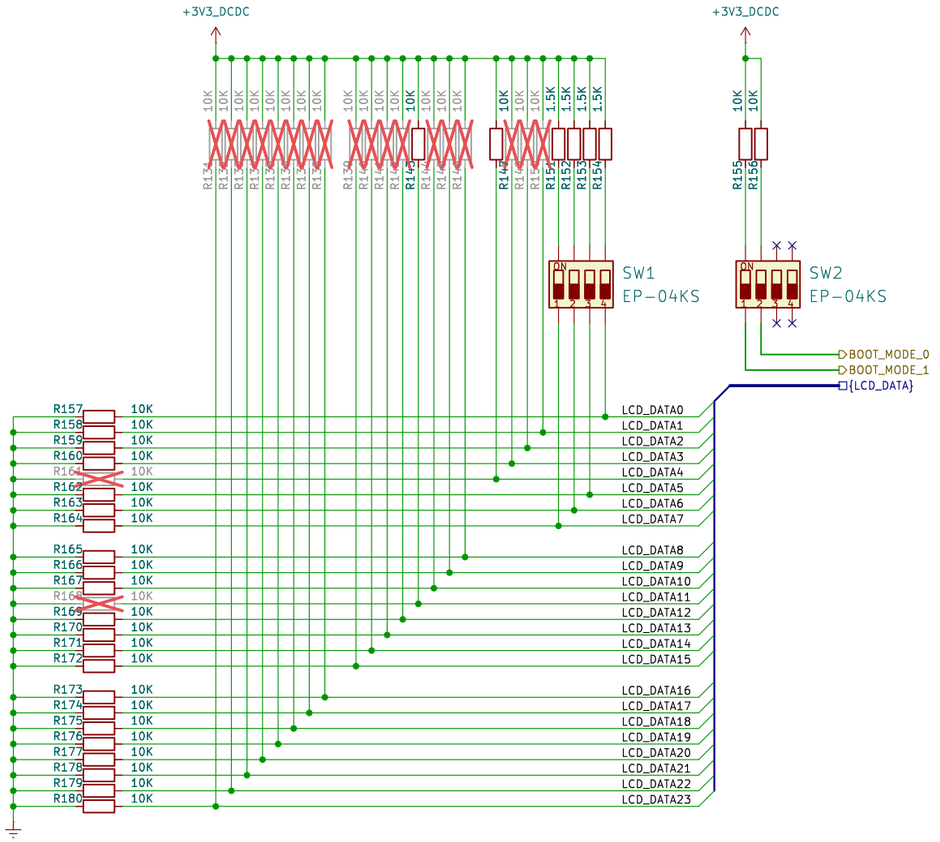
FUSE MAP <Default: QSPI BOOT>

	0/1	0/1	0/1	1	0	0	0	0
TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved	DDRSMP: "000" : Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		*SD Power Cycle Enable* *'0' - No power cycle* *'1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)*	*SD Loopback Clock Source Sel(for SDR50 and SDR104 only)* *'0' - through SD pad* *'1' - direct*
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High! 1- Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	*SD Power Cycle Enable* *'0' - No power cycle* *'1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)*	*SD Loopback Clock Source Sel(for SDR50 and SDR104 only)* *'0' - through SD pad* *'1' - direct*
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		*Nand_Row_address_bytes:* *00 - 3* *01 - 2* *10 - 4* *11 - 5*	

	0	0	0	0	1	0	0	0
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	HSPHS: Half Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay selection 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	FSDLY: Full Speed Delay selection 0: one clock delay 1: two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11- Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select:: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC4.4) 110 - 8-bit DDR (MMC4.4) Else - reserved.			Port Select:: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles.			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	*Reset Time* *'0' - 12ms* *'1' - 22ms (LBA Nand)*	Reserved

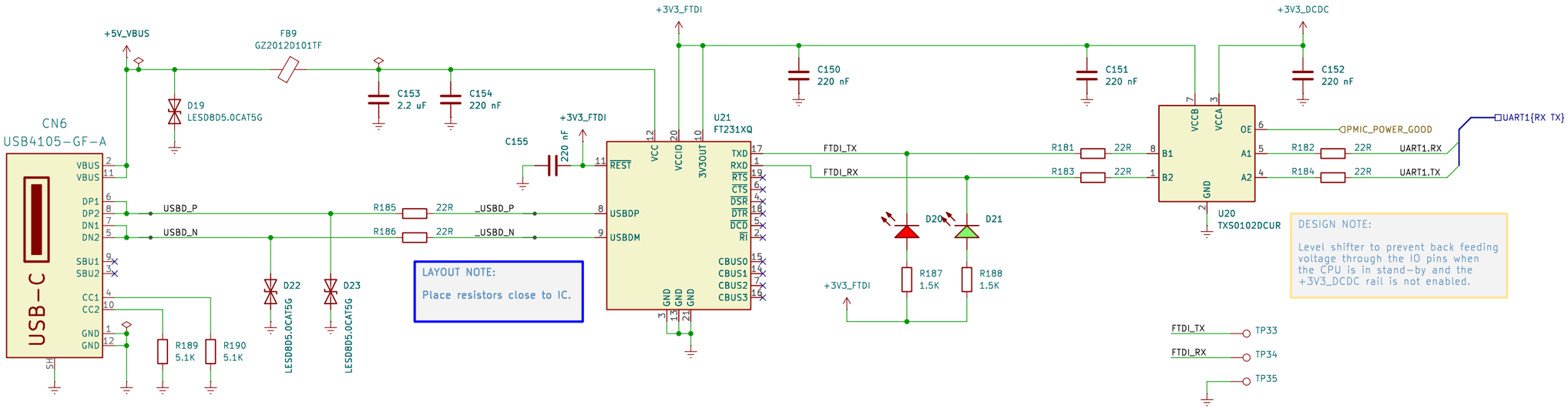
	0	0	0	0	0	0	0	0
TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	*DLL_ENABLE* *0 - Disable DLL for SD/eMMC* *1 - Enable DLL for SD/Emmc*
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	*BT_MMU_DISABLE*	*Override Pad Settings (using PAD_SETTINGS value)*
0x470	Reserved for unexpected requirements	eMMC4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	*ADD_DS_SET_GPR1_16* *0 - Set* *1 - Don't set*	*USDHC_IOMUX_SION_BIT_ENABLE* *0 - Disable* *1 - Enable*	*USDHC_IOMUX SRE Enable* *0 - Disable* *1 - Enable*
0x470	USDHC_CMD_OE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR- Bus) '00' - LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)			
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

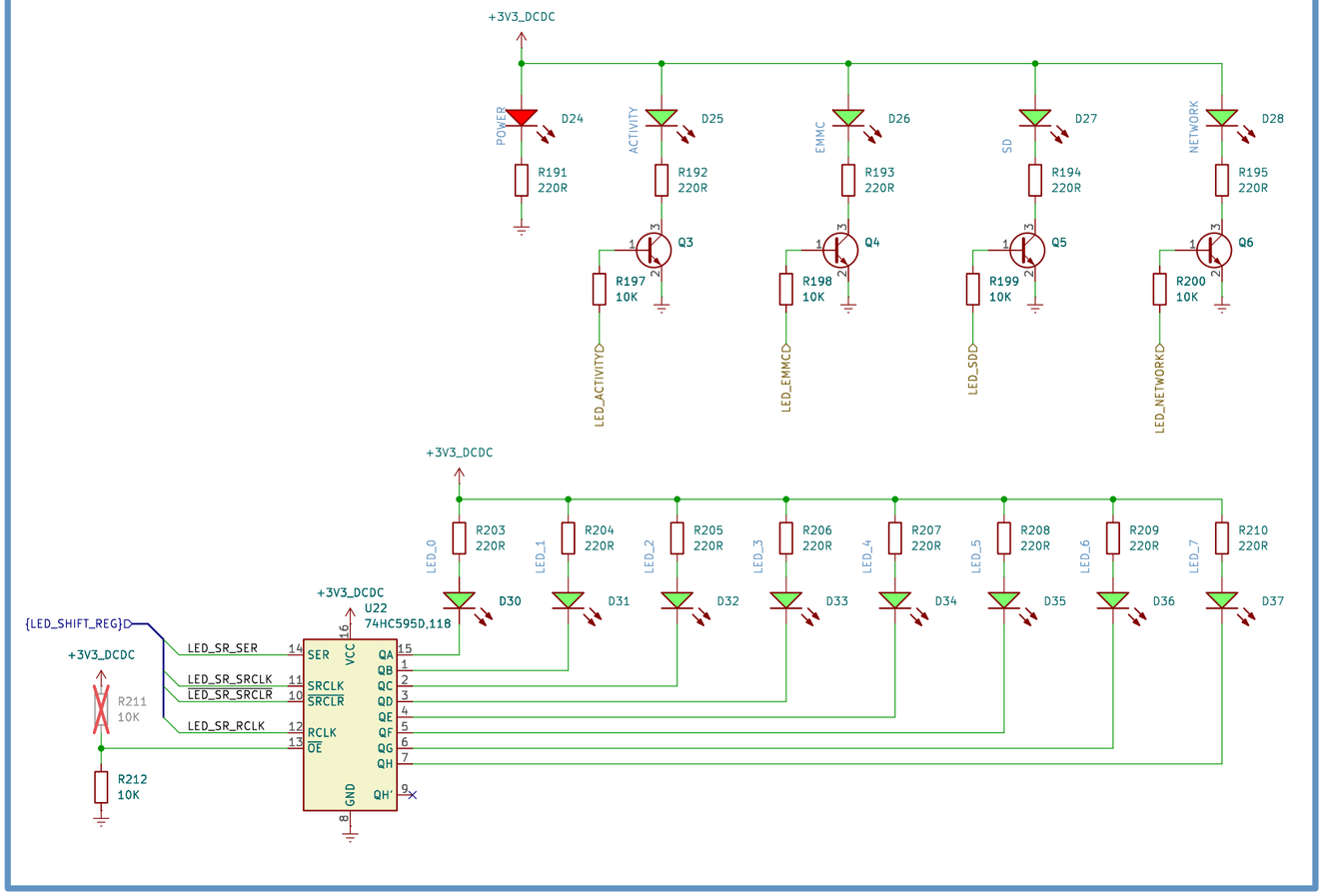


Title: i.MX6 Demo Board	
File: BOOT CONFIG.kicad_sch	
Author: ts-manuel	
Date: 2024-05-26	Rev: 00
KiCad E.D.A. 8.0.6	Size: A3 Id: 12/13

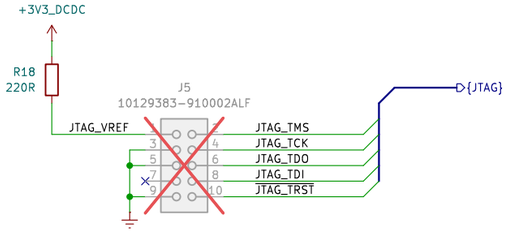
USB-C POWER & DEBUG UART



LEDs



JTAG



Title: i.MX6 Demo Board	
File: CONTROL GPIO.kicad_sch	
Author: ts-manuel	
Date: 2024-05-26	Rev: 00
KiCad E.D.A. 8.0.6	Size: A3 Id: 13/13