DSD Final Project Scores

1. BrPred

(1) Total execution cycles of given I mem BrPred:

截圖: 2062.5(ns)

(2) Total execution cycles of given I_mem_hasHazard:

截圖: 10617.5(ns)

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um²)

Baseline with sdc2.9

```
Total cell area: 235290.191633
Total area: 2218680.395307
```

BrPred with sdc2.9

```
Number of ports: 1557
Number of nets: 21014
Number of cells: 18942
Number of combinational cells: 14537
Number of sequential cells: 4268
Number of macros/black boxes: 0
Number of buf/inv: 3583
Number of references: 151

Combinational area: 147234.172982
Buf/Inv area: 25264.101541
Noncombinational area: 130889.905945
Macro/Black Box area: 0.000000
Net Interconnect area: 278124.078927
Total cell area: 278124.078927
Total area: 2611375.996193
```

差距:42833.887294(um^2)

2. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um²)

截圖:

```
Number of ports:
Number of nets:
Number of cells:
                                                          21014
                                                          18942
Number of combinational cells:
Number of sequential cells:
Number of macros/black boxes:
Number of buf/inv:
Number of references:
                                                           3583
                                                            151
Combinational area:
                                              147234.172982
                                             25264.101541
130889.905945
Buf/Inv area:
Noncombinational area:
Macro/Black Box area:
Net Interconnect area:
                                                     0.000000
                                             2333251.917267
                                             278124.078927
2611375.996193
Total cell area:
```

差距: 42833.887294(um^2)

(2) Total Simulation Time of given I mem compression: (ns)

截圖: 2442.5ns

(3) Area*Total Simulation Time: (um² * ns)

2442.5*278124.078927 = 6.793E8

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns) 5ns

3. Q sort

(1) Area: (um²)

截圖: 278124.078927(um^2)

```
Number of ports:
                                         1557
Number of nets:
                                        21014
Number of cells:
                                        18942
                                        14537
Number of combinational cells:
Number of sequential cells:
                                         4268
Number of macros/black boxes:
                                            0
Number of buf/inv:
                                         3583
Number of references:
                               147234.172982
Combinational area:
Buf/Inv area:
                                25264.101541
                               130889.905945
Noncombinational area:
Macro/Black Box area:
                                     0.000000
                               2333251.917267
Net Interconnect area:
Total cell area:
                                278124.078927
Total area:
                               2611375.996193
```

(2) Best Total Simulation Time : (ns)

(either using compressed or uncompressed instructions)

截圖: 431248.85(ns)

```
START!!! Simulation Start ....

Simulation FINISH !!------

\(^\circ^\)/ CONGRATULATIONS!! The simulation result is PASS!!!

finish called from file "Final_tb_v2.v", line 144.

finish at simulation time 431248850

V C S S im u l at i o n R e p o r t

Time: 431248850 ps

CPU Time: 50.200 seconds; Data structure size: 5.1Mb

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CPU time: 3.974 seconds to compile + 1.400 seconds to elab + 1.441 seconds to link + 50.249 seconds in simulation
```

- (3) Area*Total Simulation Time: (um² * ns)
- 431248.85(ns)* 278124.078927(um^2) = 1.199E11
- (4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns) 2.9(ns)