DSD Final Project Scores

1. BrPred

(1) Total execution cycles of given I_mem_BrPred:

截圖:　2062.5(ns)

```
Branch Part A is complete.

Branch Part B is complete.

Branch Part C is complete.

------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
$finish called from file "Final_tb.v", line 159.
$finish at simulation time             2062500
          V C S   S i m u l a t i o n   R e p o r t
Time: 2062500 ps
```

(2) Total execution cycles of given I_mem_hasHazard:

截圖:　10617.5(ns)

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
$finish called from file "Final_tb.v", line 159.
$finish at simulation time            10617500
          V C S   S i m u l a t i o n   R e p o r t
Time: 10617500 ps
```

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um^2)

Baseline with sdc2.9

```
Total cell area:                  235290.191633
Total area:                      2218680.395307
```

BrPred with sdc2.9

```
Number of ports:                         1557
Number of nets:                         21014
Number of cells:                        18942
Number of combinational cells:          14537
Number of sequential cells:              4268
Number of macros/black boxes:               0
Number of buf/inv:                       3583
Number of references:                     151

Combinational area:             147234.172982
Buf/Inv area:                    25264.101541
Noncombinational area:          130889.905945
Macro/Black Box area:                0.000000
Net Interconnect area:         2333251.917267

Total cell area:                278124.078927
Total area:                    2611375.996193
```

差距：42833.887294(um^2)

2. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um^2)

截圖:

```
Number of ports:                         1557
Number of nets:                         21014
Number of cells:                        18942
Number of combinational cells:          14537
Number of sequential cells:              4268
Number of macros/black boxes:               0
Number of buf/inv:                       3583
Number of references:                     151

Combinational area:             147234.172982
Buf/Inv area:                    25264.101541
Noncombinational area:          130889.905945
Macro/Black Box area:                0.000000
Net Interconnect area:         2333251.917267

Total cell area:                278124.078927
Total area:                    2611375.996193
```

差距：42833.887294(um^2)

(2) Total Simulation Time of given I_mem_compression: (ns)

截圖:　　2442.5ns

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
$finish called from file "Final_tb.v", line 159.
$finish at simulation time              2442500
          V C S   S i m u l a t i o n   R e p o r t
Time: 2442500 ps
```

(3) Area*Total Simulation Time: (um^2 * ns)

2442.5*278124.078927 = 6.793E8

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

5ns

3. Q_sort

(1) Area: (um^2)

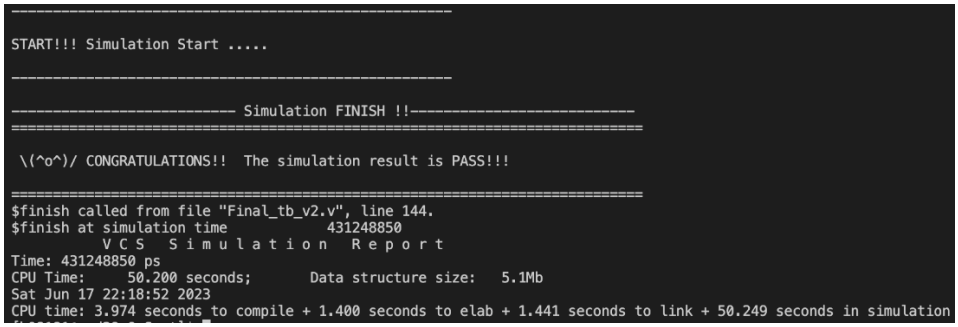
截圖:　　278124.078927(um^2)

```
Number of ports:                         1557
Number of nets:                         21014
Number of cells:                        18942
Number of combinational cells:          14537
Number of sequential cells:              4268
Number of macros/black boxes:               0
Number of buf/inv:                       3583
Number of references:                     151

Combinational area:             147234.172982
Buf/Inv area:                    25264.101541
Noncombinational area:          130889.905945
Macro/Black Box area:                0.000000
Net Interconnect area:         2333251.917267

Total cell area:                278124.078927
Total area:                    2611375.996193
```

(2) Best Total Simulation Time : (ns)

(either using compressed or uncompressed instructions)

截圖:　　431248.85(ns)



(3) Area*Total Simulation Time: (um^2 * ns)

431248.85(ns)* 278124.078927(um^2) = 1.199E11

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

2.9(ns)