

RTL Report

Testbench	Pass (Pass/Failed)
Clock Cycle	12 (ns)
Total Time	2568 (ns)

Synthesis Report

Testbench	Pass (Pass/Failed)
Clock Cycle	12 (ns)
Cell Area	152569.101180 um ² (Please report Total cell area)
Total Time	2568 (ns)
Area*Time ²	1.006135856300056*10 ¹² (um ² *ns ²)

APR Report

Testbench	Pass (Pass/Failed)
Clock Cycle	12 (ns)
Cell Area	184100.004 um ² (Please report Total area of Core)
Total Time	2568 (ns)
Area*Time ²	1.214070304778496*10 ¹² (um ² *ns ²)

How to report area in Design Vision?

➔ report_area > autoseller_area.txt, find **Total cell area**.

How to report area in Innovus?

➔ File > Report > Summary > choose Text only, file name: **summaryReport.rpt**>OK, find **Total area of Core**.

RTL Simulation Result (截圖)

```
===== The test result is ..... PASS =====

*****
**                                          **
**          Congratulations !!          **
**                                          **
** All data have been generated successfully! **
**                                          **
*****
                                          /|_____|\\
                                          (( ' - - ' ))
                                          ///      \\
                                          /||      ||\\
                                          w|\\ m      m /|w
                                          \\(o)____(o)/

=====
total cycle:          213
Simulation complete via $finish(1) at time 2568 NS + 0
```

Synthesis Simulation Result (截圖)

```
===== The test result is ..... PASS =====

*****
**                                          **
**          Congratulations !!          **
**                                          **
** All data have been generated successfully! **
**                                          **
*****
                                          /|_____|\\
                                          (( ' - - ' ))
                                          ///      \\
                                          /||      ||\\
                                          w|\\ m      m /|w
                                          \\(o)____(o)/

=====
total cycle:          213
Simulation complete via $finish(1) at time 2568 NS + 0
```

Synthesis Timing Report

Report : timing
-path full
-delay max
-max_paths 1
-sort_by group
Design : SW
Version : R-2020.09-SP5
Date : Thu Jun 9 14:17:32 2022

A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: slow Library: slow
Wire Load Model Mode: top

Startpoint: H_reg[15][1]
(rising edge-triggered flip-flop clocked by clk)
Endpoint: query_i_reg[5]
(rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port	Wire Load Model	Library
SW	tsmc13_wl10	slow

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	1.00	1.00
H_reg[15][1]/CK (DFFRQX8)	0.00	1.00 r
H_reg[15][1]/Q (DFFRQX8)	0.22	1.22 f
U5689/Y (INVX12)	0.04	1.26 r
U3958/Y (INVX6)	0.03	1.30 f
U5773/Y (NAND2B8X4)	0.08	1.38 f
U9655/Y (OAI2B8B1X4)	0.11	1.48 f
U4240/Y (NAND2X8)	0.05	1.54 r
U9658/Y (OAI2B8B1X4)	0.11	1.65 r
U9624/Y (BUF2X8)	0.09	1.74 r
U5692/Y (INVX28)	0.05	1.79 f
U3887/Y (OR2X8)	0.11	1.90 f
U4442/Y (NAND2X6)	0.07	1.97 r
U7384/Y (AOI2B8B1X4)	0.11	2.08 r
U5758/Y (OAI21X4)	0.06	2.14 f
U9668/Y (AOI22X4)	0.12	2.26 r
U4238/Y (BUF2X8)	0.09	2.35 r
U4254/Y (CLKAND2X12)	0.09	2.45 r
U4259/Y (CLKOR2X8)	0.24	2.69 f
U4188/Y (INVX6)	0.05	2.74 r
U5062/Y (NAND2X6)	0.04	2.78 f
U4851/Y (NAND2X8)	0.08	2.86 f
U4787/Y (NAND3X8)	0.09	2.95 f
U5623/Y (NAND3X8)	0.10	3.04 r
U4243/Y (INVX28)	0.06	3.10 f
U5179/Y (INVX8)	0.18	3.29 f
U3962/Y (CLKINVX8)	0.04	3.32 r
U9727/Y (OAI211X2)	0.09	3.41 f
U4852/Y (NAND3X4)	0.11	3.52 r
U6087/Y (OAI2B8B1X4)	0.15	3.66 r
U3969/Y (INVX28)	0.06	3.73 f
U4399/Y (INVX6)	0.16	3.89 f
U9731/Y (AOI211X2)	0.16	4.04 r
U9732/Y (OAI222X2)	0.13	4.17 f
U4300/Y (NAND3X4)	0.11	4.28 r
U4775/Y (NAND2X6)	0.05	4.33 f
U4776/Y (NAND2X8)	0.06	4.39 r
U4777/Y (INVX28)	0.05	4.44 f
U5653/Y (INVX4)	0.14	4.58 f
U9736/Y (AOI211X2)	0.15	4.73 r
U4860/Y (AOI21X4)	0.06	4.79 f
U9739/Y (OAI211X2)	0.17	4.95 r
U5593/Y (NAND2X4)	0.07	5.03 f
U5343/Y (NAND2X8)	0.07	5.10 r
U4180/Y (INVX28)	0.06	5.15 f
U5277/Y (INVX4)	0.09	5.25 r
U5291/Y (OAI2B8B1X4)	0.14	5.30 f
U4217/Y (NOR2X8)	0.07	5.46 r
U5629/Y (AOI21X4)	0.04	5.50 f
U9746/Y (OAI211X2)	0.17	5.67 r
U5824/Y (NAND2X4)	0.07	5.74 f
U5315/Y (NAND2X8)	0.07	5.81 r
U4232/Y (INVX28)	0.05	5.86 f
U5309/Y (INVX4)	0.10	5.96 f
U8996/Y (AOI211X2)	0.19	6.12 r
U5612/Y (AOI2B8B1X4)	0.07	6.22 f
U9749/Y (OAI211X2)	0.14	6.36 r
U5120/Y (OAI2B8B1X4)	0.14	6.50 f
U4108/Y (INVX12)	0.06	6.57 f
U4327/Y (INVX4)	0.15	6.71 f
U9751/Y (AOI211X2)	0.17	6.80 r
U4052/Y (AOI2B8B1X4)	0.09	6.98 f
U4286/Y (NOR2X8)	0.06	7.04 r
U4285/Y (NOR2X6)	0.04	7.08 f
U4033/Y (NAND2X8)	0.04	7.12 r
U3957/Y (NAND2X8)	0.04	7.16 f
U4448/Y (NAND2X8)	0.06	7.22 r
U4162/Y (INVX28)	0.04	7.27 f
U5458/Y (INVX4)	0.13	7.40 f
U5226/Y (OAI2B8B1X4)	0.13	7.53 f
U4203/Y (NOR2X8)	0.07	7.60 r
U5241/Y (AOI21X4)	0.04	7.64 f
U9758/Y (OAI211X2)	0.16	7.80 r
U4209/Y (NAND2X4)	0.07	7.87 f
U5833/Y (NAND2X8)	0.08	7.95 f
U4204/Y (CLKINVX16)	0.07	8.02 f
U5198/Y (INVX4)	0.10	8.12 f
U4713/Y (OAI2B8B1X4)	0.13	8.25 f
U5723/Y (NOR2X8)	0.07	8.32 r
U5852/Y (AOI2B8B1X4)	0.04	8.37 f
U9762/Y (OAI211X2)	0.14	8.51 r
U9763/Y (AOI22X4)	0.16	8.67 r
U5154/Y (INVX12)	0.06	8.74 f
U4670/Y (INVX4)	0.14	8.88 f
U5518/Y (OAI2B8B1X4)	0.12	9.00 f
U8880/Y (NOR2X8)	0.06	9.08 r
U4296/Y (AOI2B8B1X4)	0.04	9.18 f
U9766/Y (OAI211X2)	0.16	9.26 r
U4814/Y (NAND2X4)	0.07	9.33 f
U4815/Y (NAND2X8)	0.07	9.40 r
U5510/Y (INVX16)	0.05	9.45 f
U5513/Y (INVX4)	0.14	9.50 f
U5313/Y (OAI2B8B1X4)	0.13	9.71 f
U3838/Y (NOR2X8)	0.06	9.77 r
U5529/Y (AOI21X4)	0.04	9.81 f
U9769/Y (OAI211X2)	0.17	9.98 r
U5590/Y (NAND2X4)	0.07	10.05 f
U5591/Y (NAND2X8)	0.06	10.12 r
U4925/Y (INVX16)	0.05	10.17 f
U5753/Y (INVX4)	0.14	10.32 f
U9773/Y (AOI211X2)	0.15	10.47 r
U9774/Y (AOI2B8B1X2)	0.08	10.55 f
U5108/Y (AOI2B8B1X4)	0.14	10.70 f
U4449/Y (NAND2X6)	0.06	10.76 r
U9773/Y (NAND2X8)	0.05	10.80 f
U5446/Y (NAND2X8)	0.05	10.86 r
U5848/Y (INVX16)	0.05	10.91 f
U9618/Y (INVX6)	0.15	11.06 f
U5684/Y (AOI21X4)	0.09	11.14 r
U5662/Y (AND2X8)	0.09	11.23 r
U5276/Y (AOI211X4)	0.03	11.26 f
U9776/Y (OAI211X2)	0.16	11.43 r
U5720/Y (NAND2X4)	0.07	11.50 f
U5847/Y (NAND2X8)	0.08	11.58 r
U5840/Y (INVX28)	0.06	11.64 f
U3943/Y (CLKOR2X6)	0.16	11.80 f
U3942/Y (INVX8)	0.06	11.86 r
U5135/Y (AOI211X2)	0.07	11.93 f
U4294/Y (OR2X6)	0.15	12.08 f
U4173/Y (NAND2X8)	0.06	12.14 r
U9590/Y (AOI31X2)	0.07	12.21 f
U5523/Y (NAND2B8X4)	0.13	12.34 f
U4249/Y (AND2X8)	0.10	12.43 f
U4167/Y (CLKAND2X4)	0.14	12.57 f
U4321/Y (OR2X8)	0.11	12.68 f
U4675/Y (AND3X8)	0.09	12.78 r
U4674/Y (NAND4X4)	0.05	12.83 r
query_i_reg[5]/D (DFFRQX4)	0.00	12.83 r
data arrival time		12.83
clock clk (rise edge)	12.00	12.00
clock network delay (ideal)	1.00	13.00
clock uncertainty	-0.10	12.90
query_i_reg[5]/CK (DFFRQX4)	0.00	12.90 r
library setup time	-0.07	12.83
data required time		12.83
data required time		12.83
data arrival time		12.83
slack (MET)		0.00

Synthesis Area Report

```
*****
Report : area
Design : SW
Version: R-2020.09-SP5
Date   : Wed Jun  8 18:13:44 2022
*****
```

```
Information: Updating design information... (UID-85)
Warning: Design 'SW' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)
Library(s) Used:
```

```
    typical (File: /home/raid7_2/course/cvstd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)
```

```
Number of ports:          1291
Number of nets:           13145
Number of cells:          10942
Number of combinational cells: 9116
Number of sequential cells:  1713
Number of macros/black boxes:    0
Number of buf/inv:         1648
Number of references:       258
```

```
Combinational area:      96797.630416
Buf/Inv area:            10439.009883
Noncombinational area:   55771.470764
Macro/Black Box area:    0.000000
Net Interconnect area:   1446767.382629
|
Total cell area:         152569.101180
Total area:              1599336.483809
```

Synthesis Power Report

Report : power
-analysis_effort low

Design : SW
Version: R-2020.09-SP5
Date : Thu Jun 9 14:17:51 2022

Library(s) Used:

typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Operating Conditions: slow Library: slow
Wire Load Model Mode: top

Design	Wire Load Model	Library
SW	tsmc13_wl10	slow

Global Operating Voltage = 1.08
Power-specific unit information :
Voltage Units = 1V
Capacitance Units = 1.000000pf
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V,C,T units)
Leakage Power Units = 1pW

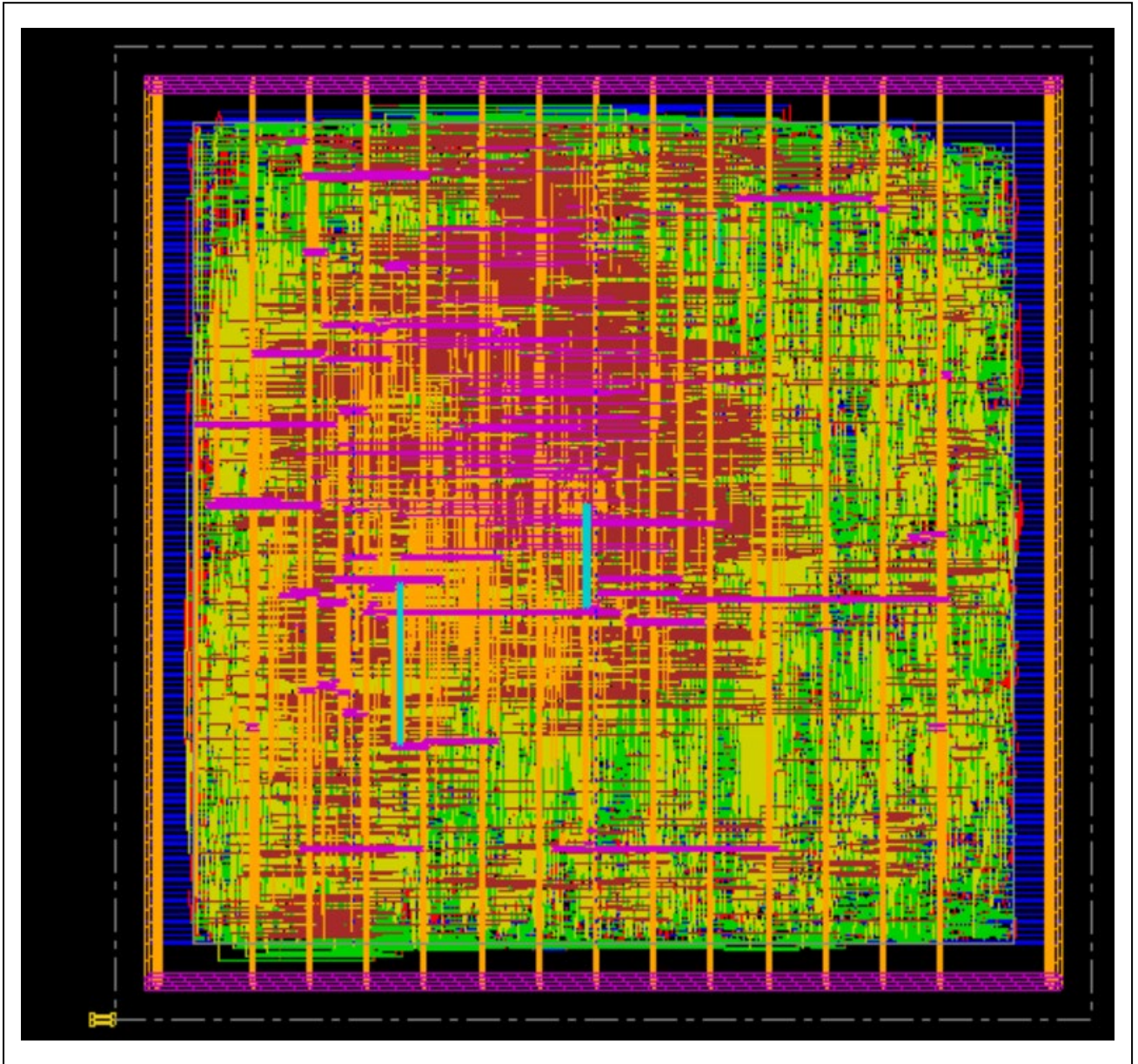
Cell Internal Power = 4.2368 mW (87%)
Net Switching Power = 620.1718 uW (13%)

Total Dynamic Power = 4.8570 mW (100%)

Cell Leakage Power = 31.9548 uW

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	4.0705	7.9914e-02	1.5139e+07	4.1655	(85.20%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	0.1664	0.5403	1.6816e+07	0.7234	(14.80%)	
Total	4.2368 mW	0.6202 mW	3.1955e+07 pW	4.8890 mW		

APR NanoRoute Innovus Result (截圖)



APR Simulation Result (截圖)

```

===== The test result is ..... PASS =====

*****
**                                          **
**          Congratulations !!          **
**                                          **
** All data have been generated successfully! **
**                                          **
*****
                                          /|_____|\\
                                          (( ' - - ' ))
                                          //      \\
                                          /||      ||\\
                                          w|\\ m      m /|w
                                          \\(o)____(o)/

=====
total cycle:          213
Simulation complete via $finish(1) at time 2568 NS + 0

```

Report

(If you don't pass APR, the score will be determined by the completeness of the report below)