Chung-Wen (Albert) Tsao

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SUMMARY

- Strong passion about STEM technology education and distance learning.
- In-depth knowledge of algorithms, data structures and programming skills.
- USA Computing Olympiad of algorithmic programming skills, Coach.
- Experienced software engineer for complex large-scale software engineering projects: problem specification, prototyping, infrastructure planning, implementation, unit and flow test scripts, and documentation.

SOFTWARE SKILLS:

Java, C++, C, HTML/CSS/JavaScript, PHP/MySQL/, Tcl, Cadence Place & Route tool, Linux/UNIX/Window, Python/NumPy/Pandas data wrangling/summarization/visualization

WORK EXPERIENCE:

California State University, East Bay, 2017-now
- Lecturer (Part-Time), C++ programming, Introduction to Computer Science II, Operating System, Computer Architecture, Automata and Computing Theory

San Jose State University, San Jose, 2017-now
- Adjunct Professor, Algorithm Design and Analysis

Cogswell College, San Jose, 2017-now
- Adjunct Professor, Linux, Advanced C++, Computer Architecture, Digital Systems, Data Structures and algorithms, Python Programming

Chabot College, Hayward, 2017-now
- Adjunct Professor, Introduction to Linux, Python Programming, Computer Literacy

San Jose City College, 2016-now
- Adjunct Professor, C++, Python Programming, HTML/CSS/JavaScript/PHP/MySQL

Silicon Valley University, 2016-2017
- Adjunct Professor, Data Structures and Algorithm, Operating Systems

Springlight Education Institute/W3 Coding School, 2014-2015

- Instructor, problem analysis, algorithm design, debugging and programming skills in JAVA/C++/C/JavsScript/Tcl/Python for programming contests
- Instructor, USA Computing Olympiad of algorithmic programming skills.
- Online Education and Distance Learning

Cadence Design Systems, 2002 – 2013
SMCS/Architect,

- Invented two-stage Clock Tree Synthesis (CTS) to effectively control clock skews and minimize buffering cost
- Researched VLSI CAD algorithm, performance-driven routing and buffering topology.

PATENT / AWARDS

- United States Patent # 7,051,310, May 23, 2006
  "Two-Stage Clock Tree Synthesis With Buffer Distribution Balancing"
- C Code for Bounded-Skew Clock Routing in VLSI, UCLA Case#. LA 97-088-01
- R&D Special Achievement Award, Cadence Design Systems, Inc., 1998

EDUCATION

Computer Science Major, University of California, Los Angeles, Ph.D. in Computer Science. October 1996.

Electrical Engineering Major, National Taiwan University, Taipei.

- B.S. in Electrical Engineering.

PUBLICATIONS: 7 conference papers (one best paper candidate) and 5 journal papers