DIGITAL LOGIC

Course Introduction

2025 Fall

baiyh@sustech.edu.cn

Course Information

- Course website:
  - Blackboard:
- Instructor:
  - Dr. Yuhui BAI (baiyh@sustech.edu.cn)
  - Office: 411 College of Engineering South
  - Office hour: Tue. 10:00-12:00 (by appointment)
- Lecture
  - 14:20-15:50 Tue., 208 Lecture Hall #3 (Bilingual)
  - 16:20-18:10 Tue., 103 Business Hall (English)
- Lab
  - 16:20 -18:10 Tue., 511 Lecture Hall #3 (Wei WANG, Bilingual)
  - 10:20 -12:10 Wed., 511 Lecture Hall #3 (Wei WANG, Bilingual)
  - 10:20 -12:10 Wed., 510 Lecture Hall #3 (Yuhui BAI, English)
  - 14:00 -15:50 Wed., 511 Lecture Hall #3 (Wei WANG, Bilingual)
  - 10:20 -12:10 Fri., 511 Lecture Hall #3 (Wei WANG, Bilingual)

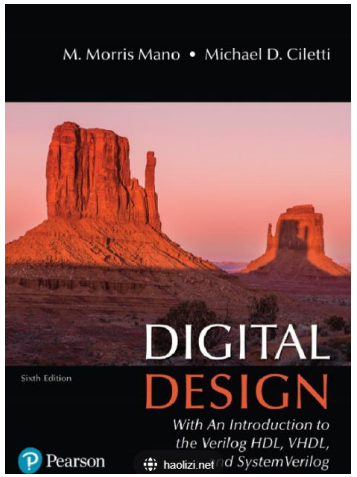
Grading criteria

- Lecture (20%)
  - 10% Weekly In Class Quiz (open book)
  - 10% Homework
- Exam (55%)
  - 20% Mid-term Examination (W8 weekend)
  - 35% Final Examination
- Lab (25%)
  - 5% Lab Attendance + Practices
  - 5% Lab Assignments (OJ)
  - 15% Lab Project
    - In groups of 2~3. Please team up as soon as possible. You are allowed to form teams across different lab groups, but all team members must be present during the project inspection.

- All assignments/projects this semester will be checked for plagiarism. Violators will be handled according to the undergraduate course plagiarism policy:
  - First offense: A warning and a zero on the work.
  - Second offense: A zero for the entire course.

Textbook

- Textbook:
  - Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog by *M. Morris Mano and Michael D. Ciletti*, 6th edition.



- Reference book:
  - Digital Principles and Logic Design by A. Saha and N. Manna.
  - Digital Logic Design by B. Holdsworth and C. Woods

Course Outline

- Schedule
  - Refer to Blackboard->Schedule
- Outline:
  1. Digital Systems and Binary Numbers
     Binary Systems, Conversions, Signed Binary, Codes
  2. Boolean Algebra and Logic Gates
     Theorems, Boolean Functions, operators, gates
  3. Gate-level Minimization
     Truth table, K Map, two-level implementations, NAND, NOR
  4. Combinational Logic
     Combinational circuits, arithmetic logic, mux, de-mux, encoder, decoder
  5. Synchronous Sequential Logic
     Sequential circuit, Latches, Flip flops, State Machines
  6. Registers and Counters
  7. Memory and Programmable Logic
     RAM, ROM, FPGA
  8. Verilog (Lab)

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