DIGITAL DESIGN

LAB1　USING VIVADO + FPGA DEVELOPMENT BOARD(EGO1)

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TOPICS

- Experimental Platform

  EDA tool (Vivado 2017.4) + FPGA Development Board(EGO1)

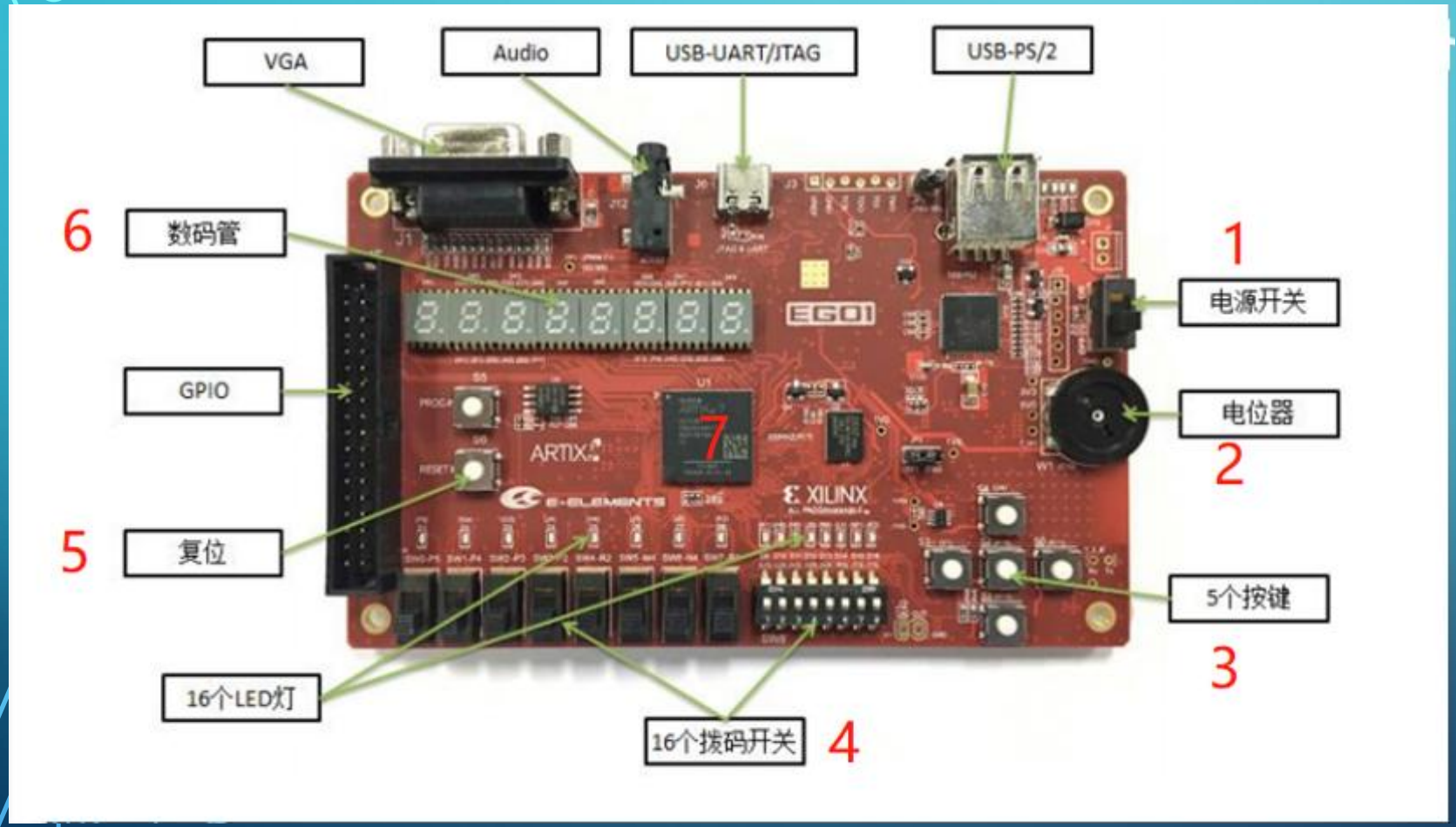
  - Vivado installation tips
  - FPGA Development Board(EGO1) introduction
- 1st Lab on Digital Logic course
  - Build a Vivado project, add circuit design file and constraint file
  - Connect Vivado with FPGA Development Board and program the FPGA chip
  - Test the circuit which runs on the FPGA chip
- Questions and Exercises

EXPERIMENTAL PLATFORM: EDA + FPGA DEVELOPMENT BOARD

- Vivado (a type of EDA tools):
  - Vivado is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors.
  - Vivado enables developers to synthesize (compile) their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.
  - The version we choose is Vivado 2017.4

- Installation of Vivado (20 G free hard disk space is suggested)
  - Attention: the name of the directory which includes installation package MUST NOT containing Chinese and space characters.

FPGA DEVELOPMENT BOARD(EGO1)



- Power Switch (1)
- Potentiometer (2)
- Button * 5 (3)
- Dial switch * 16 (4)
- **Reset Button (5)**
- **Seven-Segment Digital Tube * 8** (6)
- **Artix 7 FPGA chip** (7)

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VIVADO(2017.4) INSTALLATION (TIPS1)

Attention: Before coping, make sure there is enough free space(**20G+**) in the destination disk.

Two files are needed for the installation:
1) Installation package: "Xinlinx_Vivado_SDK_2017.4_1216_1.tar.gz"
2) Lisence file: "xinlin_ise_vivado_2017.lic"

How To Get the installation package and lisence file:

Get installation package from the websit: https://dl.cra.moe/download/FPGA/
Get lisence file from the "labs" directory of the course BlackBoard websit

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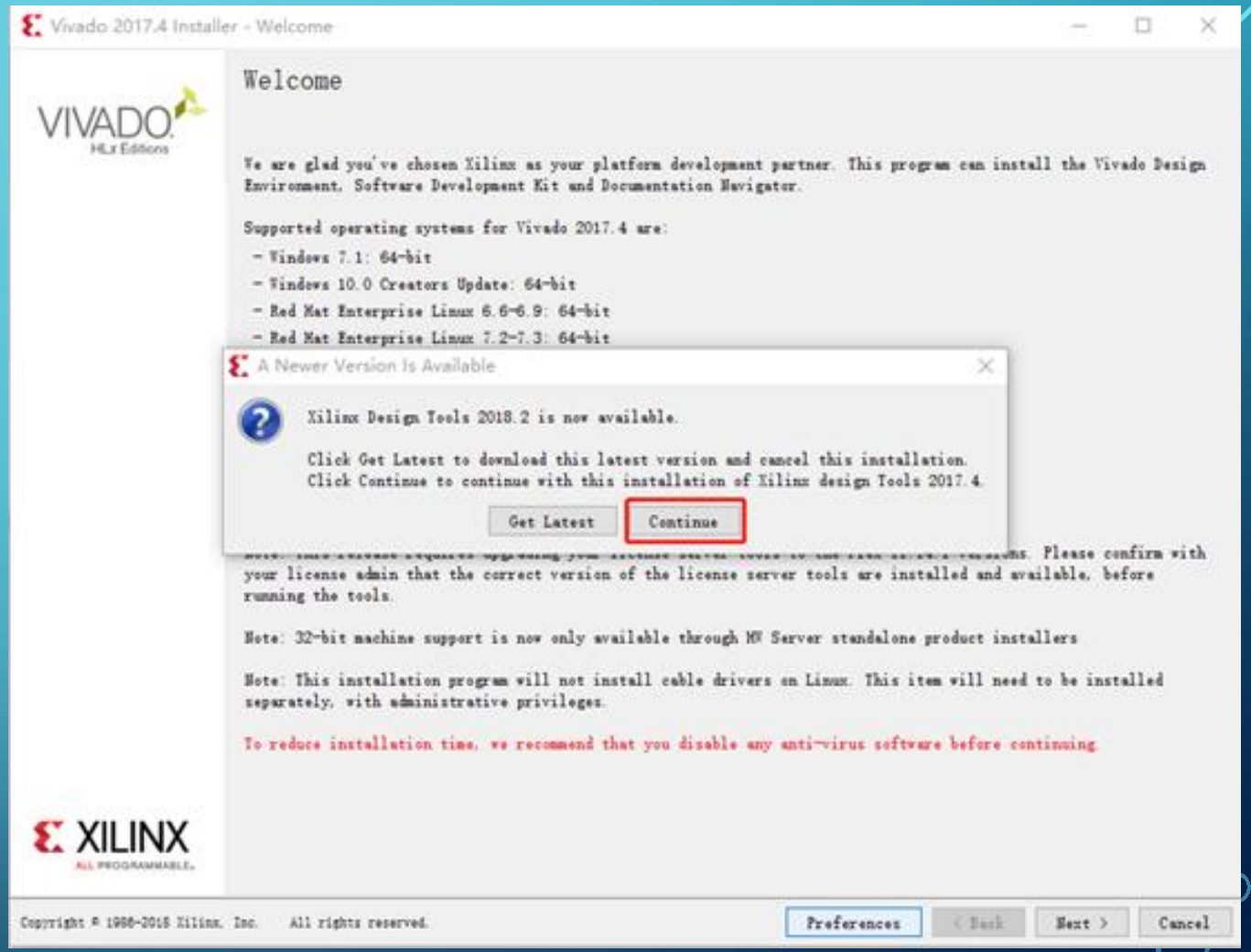
VIVADO(2017.4) INSTALLATION (TIPS2)

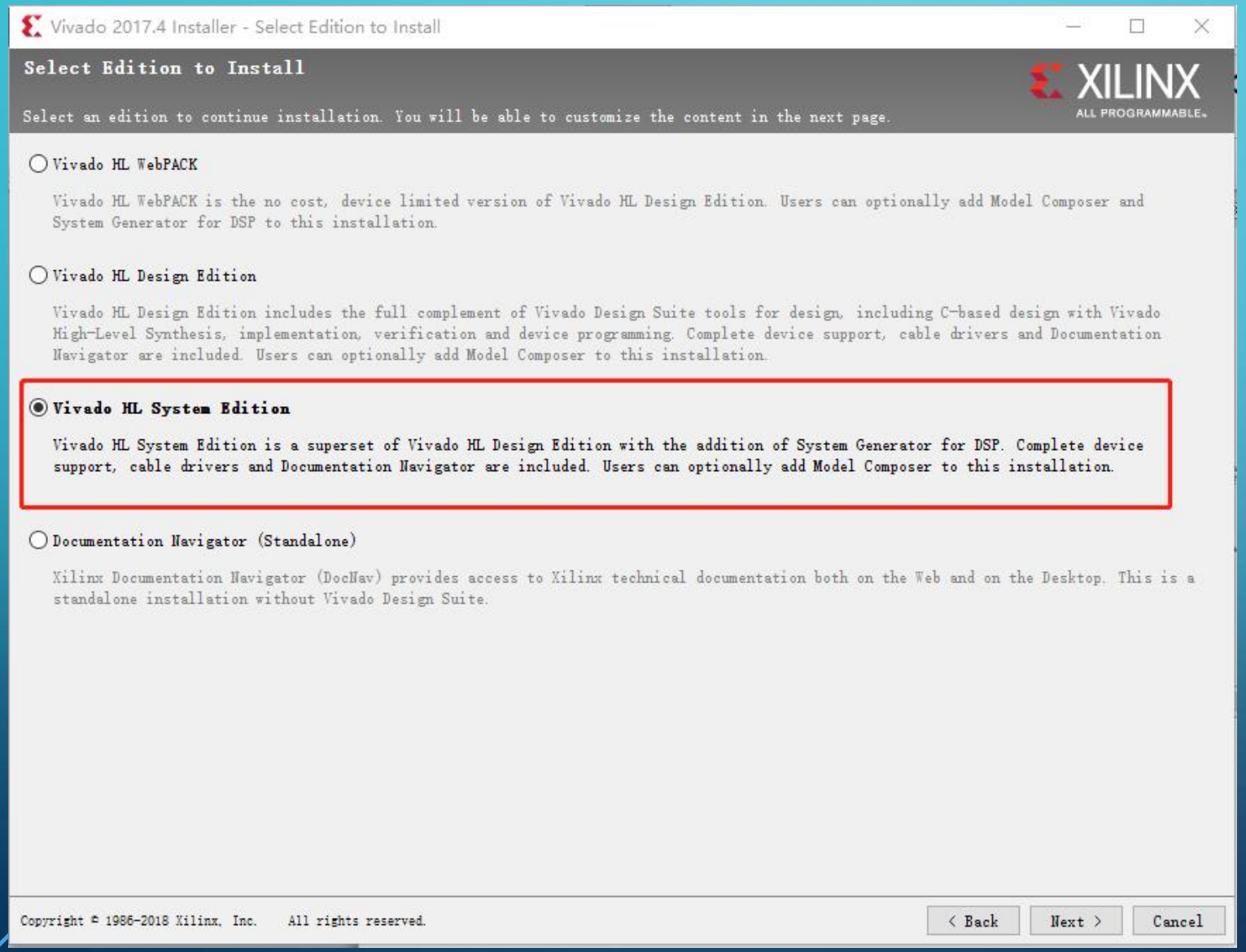
Decompress the installation package "Xinlinx_Vivado_SDK_2017.4_1216_1.tar.gz", find the file "**xsetup.exe**", **double click** it to start the installation.

Attention: Location of the vivado installation **MUST NOT containing Chinese characters and nonregular characters.**

Follow the steps on the right hand->

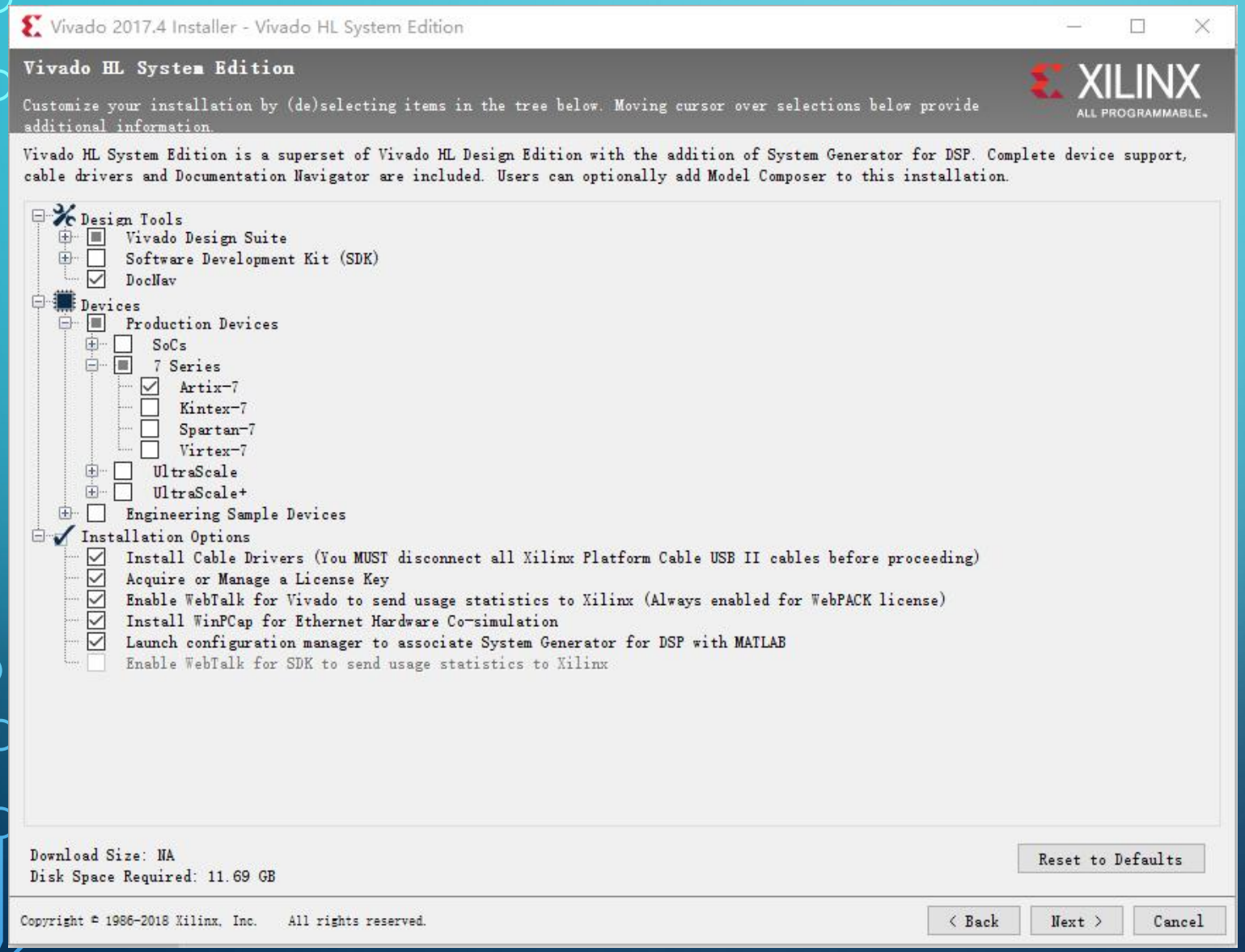


VIVADO(2017.4) INSTALLATION (TIPS3)



It's suggested to install the "Vivado HL System Edition" because of its "complete device support" and "Documention Navigator" .

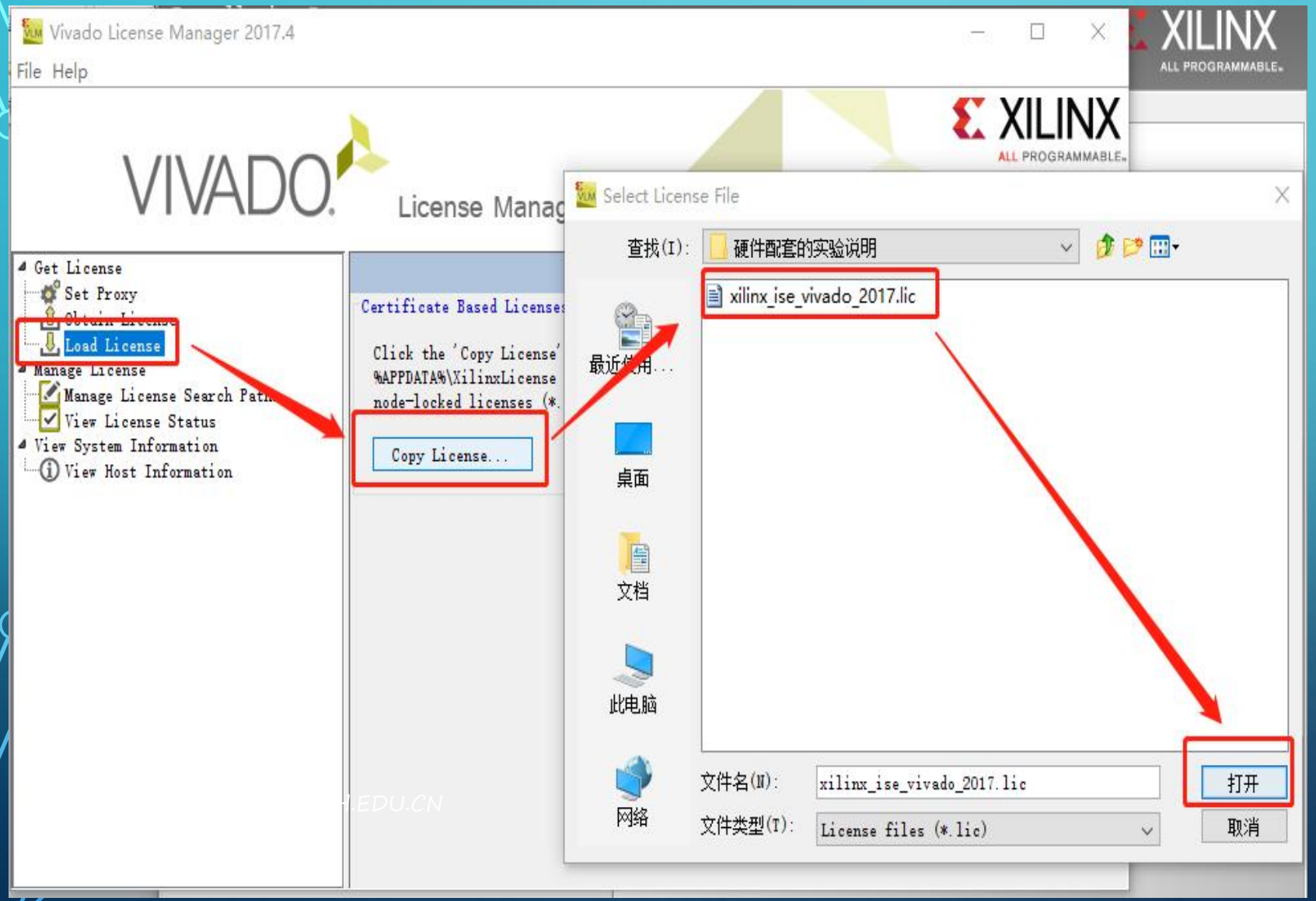
VIVADO(2017.4) INSTALLING (TIPS4)



The size of “Vivado HL system Edition” is huge.
It is strongly recommended to select **ONLY WHAT IS NEEDED TO INSTALL**!!

The options in the left figure are enough for both the Digitial Logic course and Computer Orgnization course.

VIVADO INSTALLING (TIPS4)



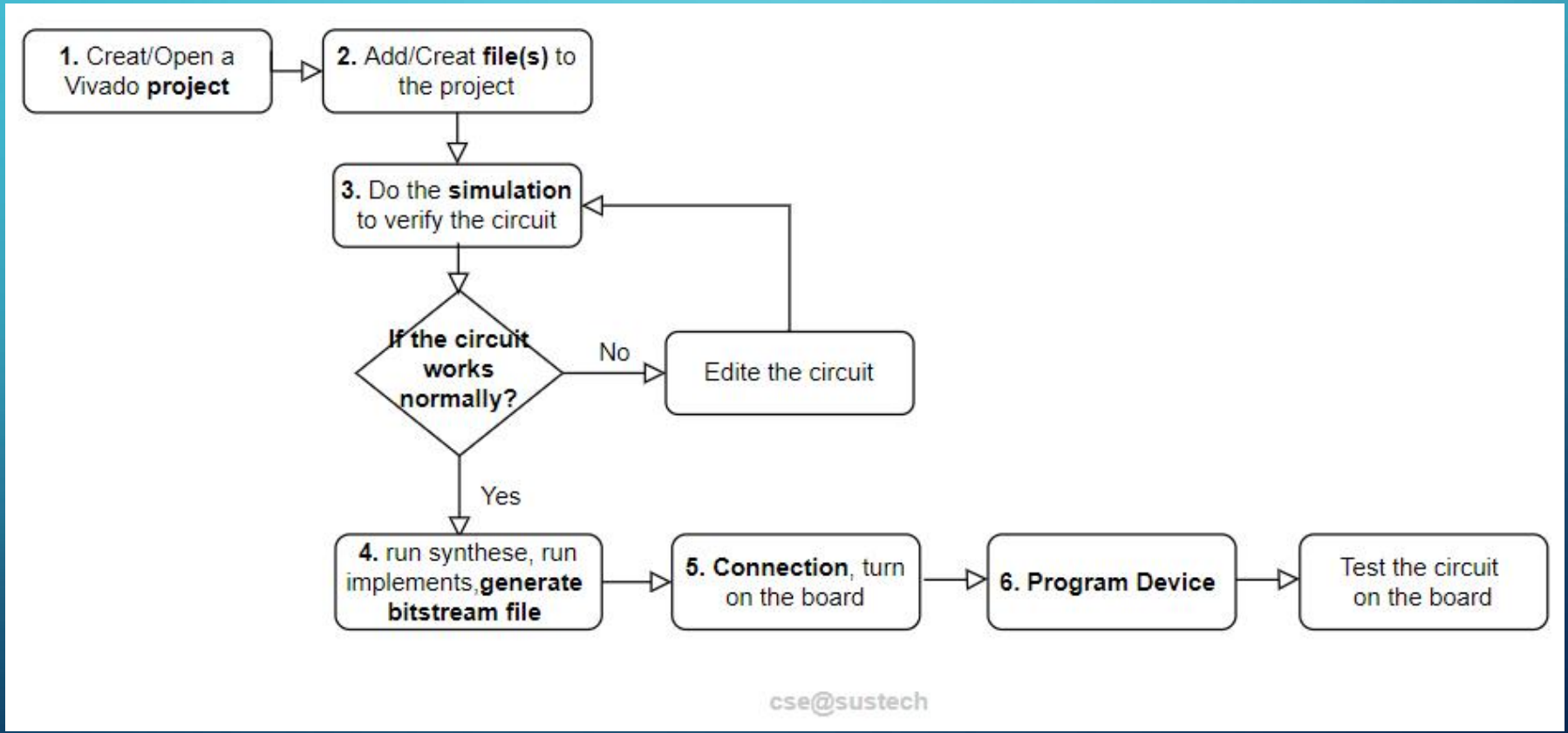
At the end of the installing, **load license** as shown in the left figure.

ATTENTION:
The license file(with ".lic" as its suffix) could be in **ANYWHERE** of your computer which is now doing the Vivado installation.

The directory "硬件配置的实验说明" here is just a demo on my computer where the license file is, **NOT MUST.**

USING VIVADO + FPGA DEVELOPMENT BOARD

Follow the Following steps to make your designed circuit implement on the FPGA chip, test the circuit on the board which is embeded with the FPGA chip and other input/output device(s).



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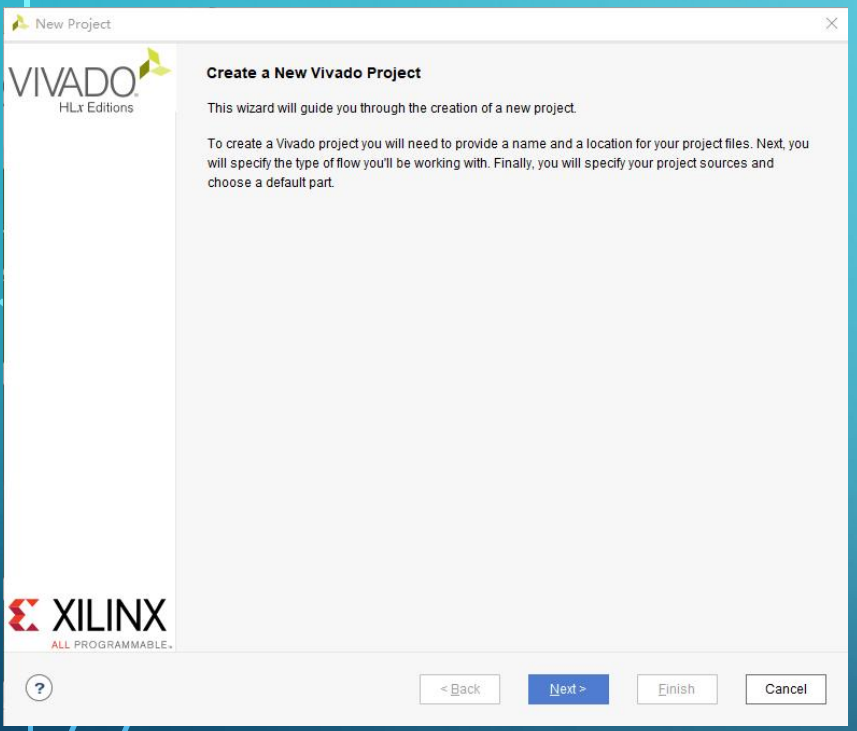
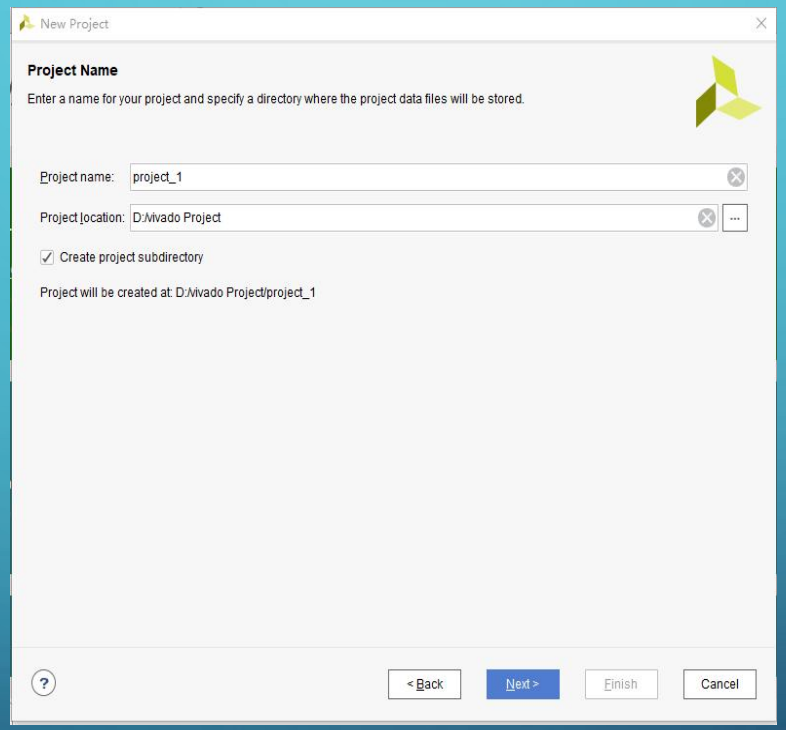
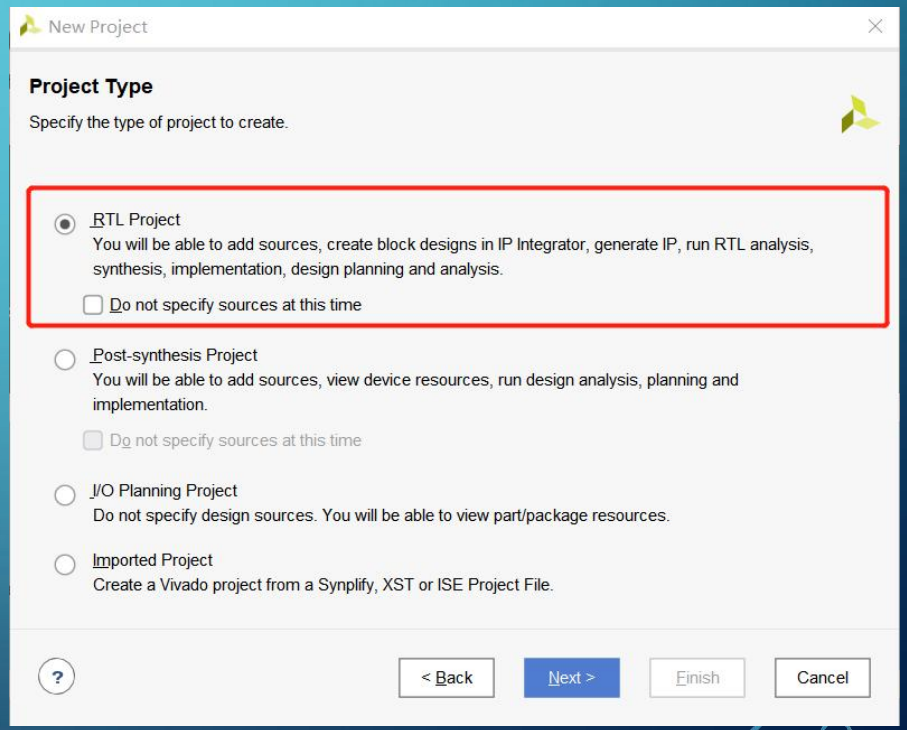
USING VIVADO + FPGA DEVELOPMENT BOARD(1-1)

STEP1-1. **Create project**, determin the **project's name and location**(the name and location of the project **MUST NOT containing Chinese characters**), select "RTL Project" as its **type,**.







Attention: the value of project name and location in the middle figure is just a demo, all of them should be upto you.

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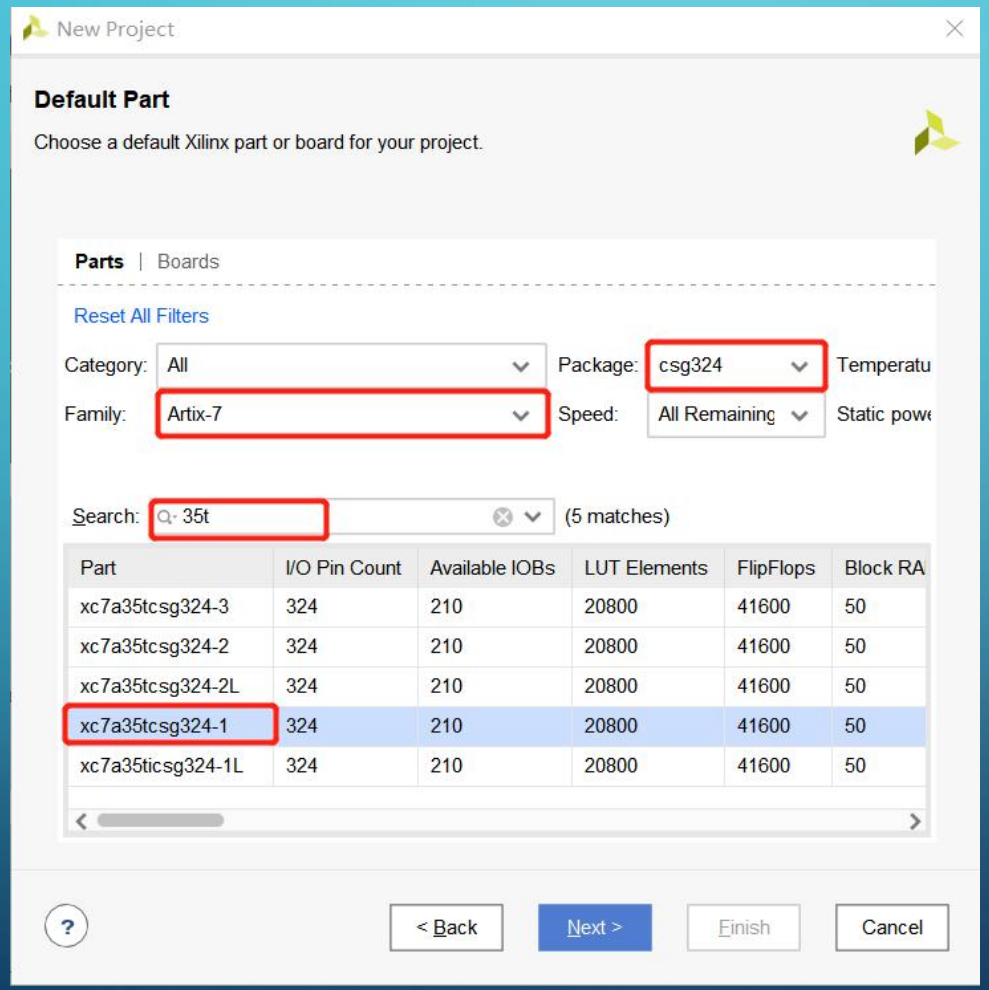
USING VIVADO + FPGA DEVELOPMENT BOARD(1-2)

STEP1-2. select the corresponding FPGA chip. The version of FPGA chip in **EGO1** is Artix 7 xc7a35t CSG324-1.



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USING VIVADO + FPGA DEVELOPMENT BOARD(2)

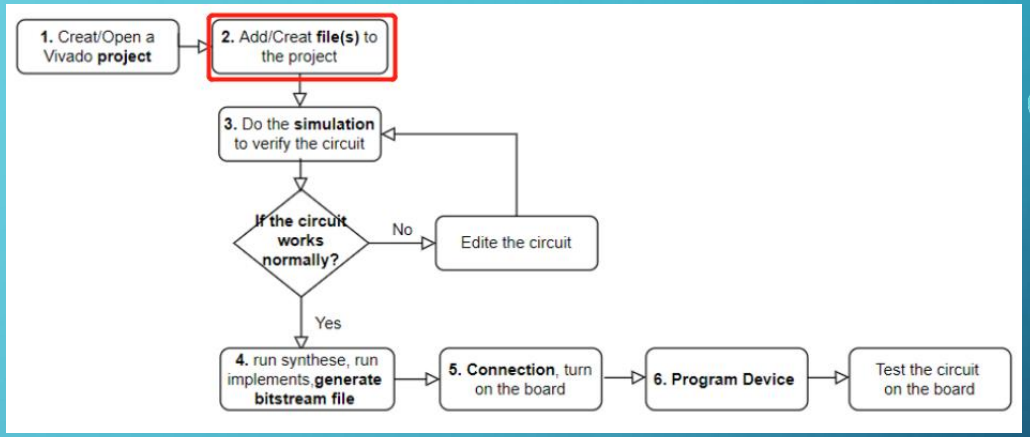
STEP2. Adding source file(s) to the project, including **design** file(s), **simulation** file(s) and **constraints** file(s). There are **two ways** to add file(s):

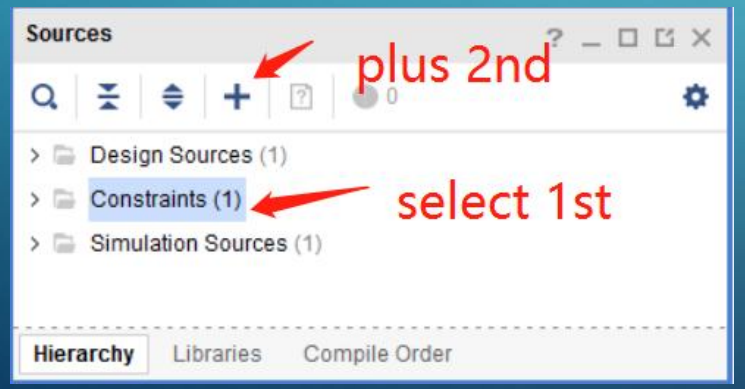
1) Adding file(s) **while creating project** (as shown in the left figure below). TIPS: If there's NO file, you can cread file(s) or just skip the adding files while creating the project.

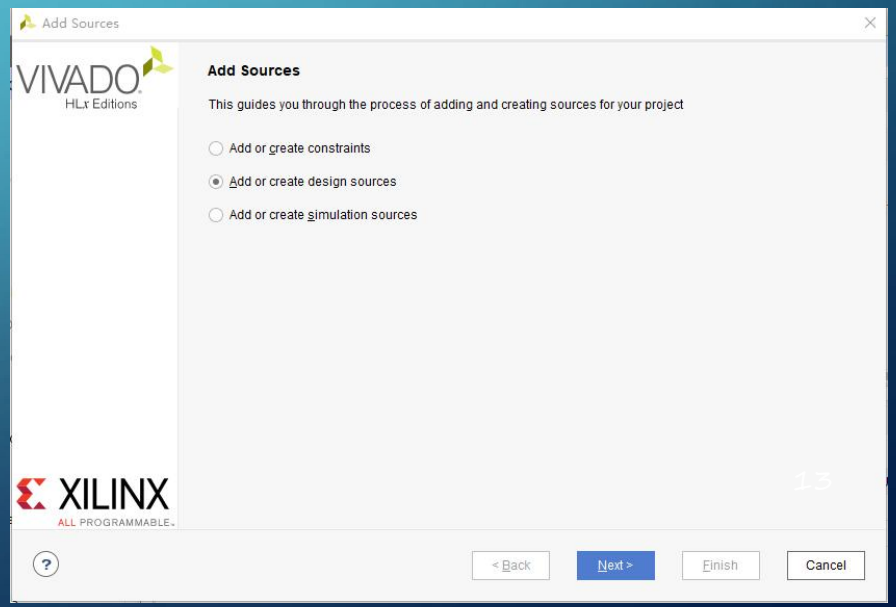
2) Adding file(s) **after the project is created** (as shown in the figures below).

Attention:

In both ways, You should **first select the file type**(disign, constraint or simulation) **then add or creat a file**.







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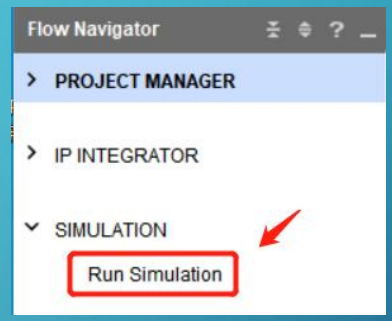
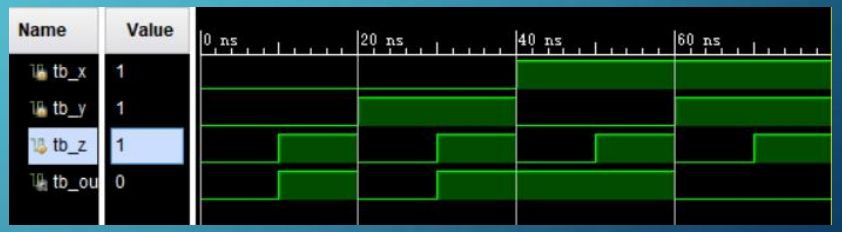
USING VIVADO + FPGA DEVELOPMENT BOARD(3)

STEP3. Do the **simulatoin**(as the right figure on the top) to **verify the function** of your designed circuit.



TIPS1: The design source file(s) and it's simulation source file should be added to the project before the simulation.

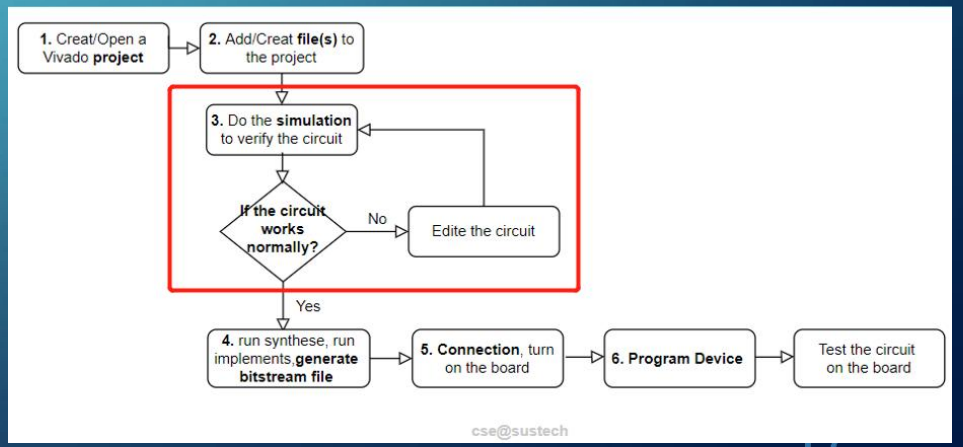
After simulation, there will be a waveform(as the right figure in the middle) which records the states of circuit's input and output signals.



TIPS2:

1) **If the** function of the circuit is NOT ok, you should **modify the design file(s)**, then do the simulation again the verigy the function of circuit. Subsequent steps can ONLY be started after the function verification is passed

2) If the function of the circuit is ok, continue the following step.



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USING VIVADO + FPGA DEVELOPMENT BOARD(4)

STEP4. If the function of the circuit is ok(verified by step 3) , then

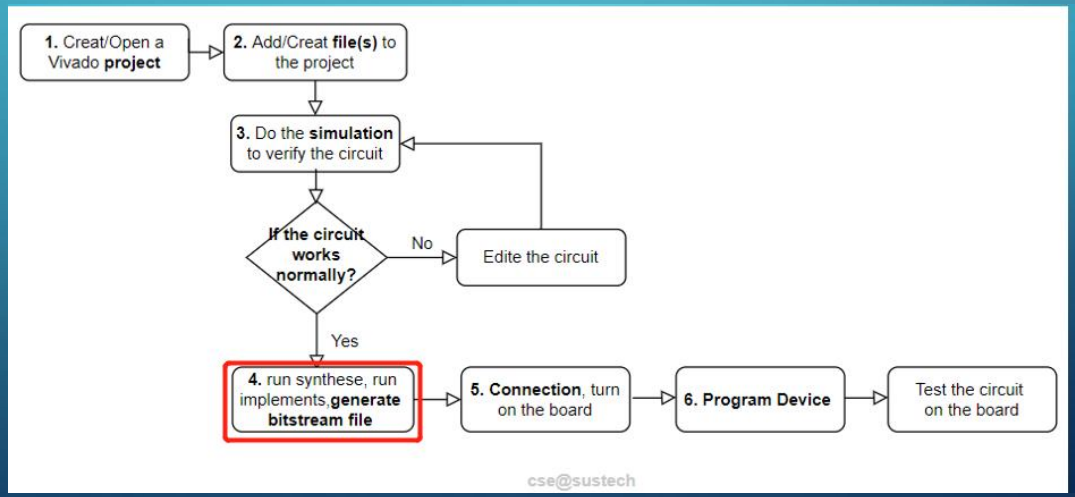
4-1. “**Run synthesis**”(**step4-1 in the right figure**)

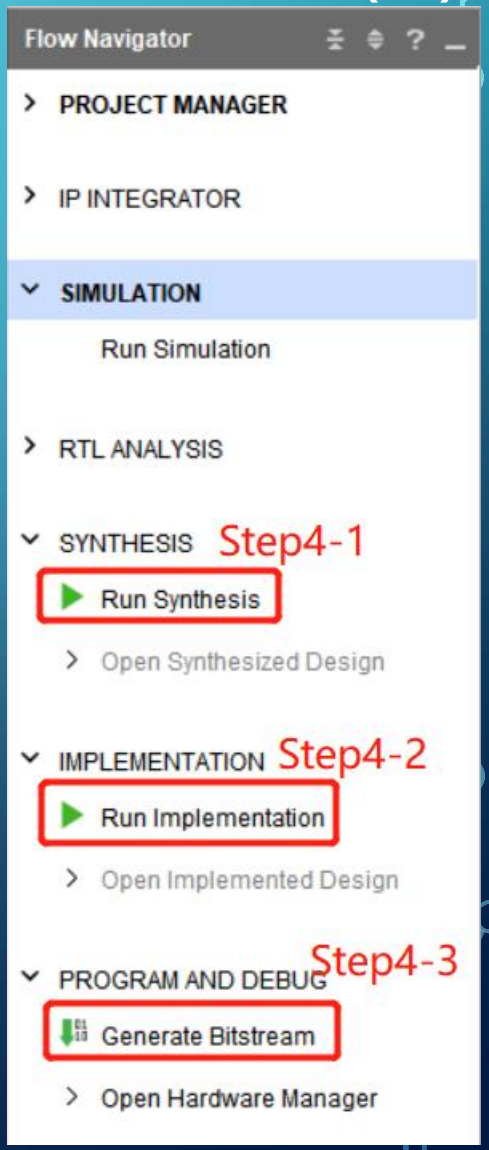
4-2. “**Run implements**”(**step4-2 in the right figure**)

4-3. “**Generate Bitstream**”(**Step4-3 in the right figure**) to generate **a bitstream file**(with “**.bit**” as its suffix) .

Attention:

If there is any error or critical warning durning the step4, check the project settings, design and constraint source file(s) and correct them, then redo the step4 to generate a correct bitstream file.





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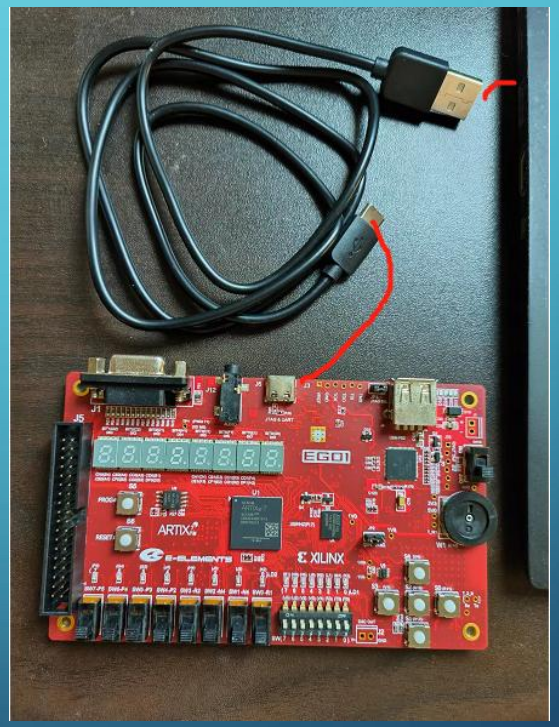
USING VIVADO + FPGA DEVELOPMENT BOARD(5-1)

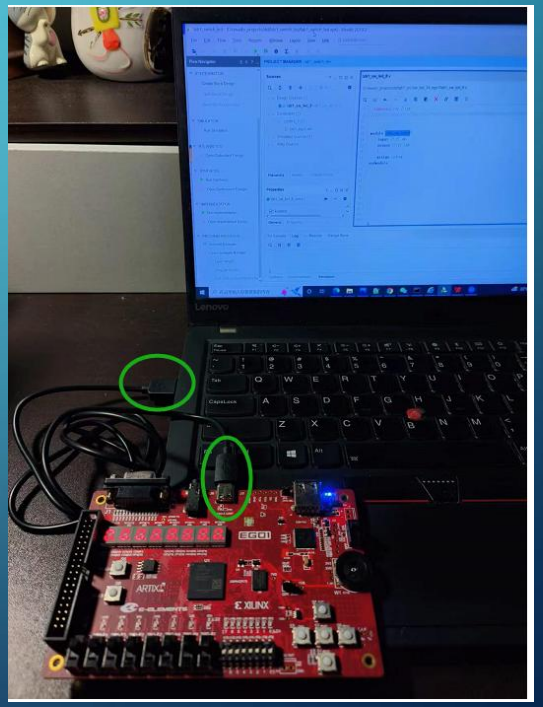
STEP5-1): Connect the EGO1 board and the PC

First **Connect** EGO1 board with PC which runs the Vivado project, then **turn on** the EGO1 board.

TIPS：Using **USB-UART/JTAG** interface of the EGO1 board for the connection.

Here is a demo of connection between EGO1 board and the PC which runs the vivado projet.





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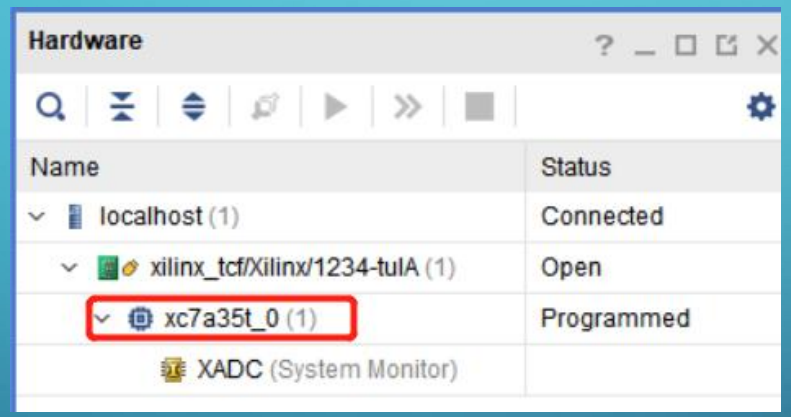
USING VIVADO + FPGA DEVELOPMENT BOARD(5-2)

STEP5-2). 'Connect' the Vivado project and the FPGA chip

In the Vivado project, first Click "**Open Hardware Manager**", then click"**open Target** " (as shown in the left figure below) to '**connect' the Vivado project with FPGA chip** which is embeded in the EGO1 board.



Attention:

1) If the FPGA chip is found by the Vivado project, the chip type could be found in the "**Hardware**" window(as shown in the right figure)

2) If there is **no** info about the chip in the "**Hardware**" window, check the chip-type first, after checking, you should redo the STEP5-1 on last page and the STEP5-2 on this page untile the FPGA chip is found in the vivado project.

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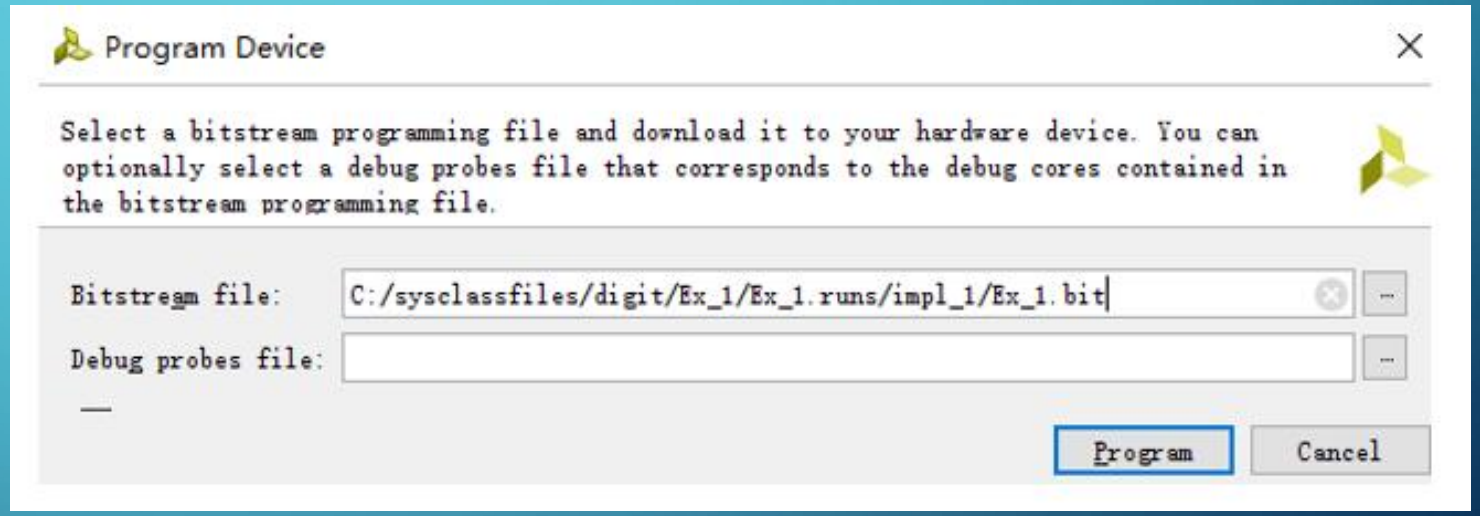
USING VIVADO + FPGA DEVELOPMENT BOARD(6)

STEP6. Click "Program Device", then choose the device name(as shown in the left figure below), select the **bitstream file**(with ".bit" as its suffix) , click "**Program**" button(as shown in the right figure below).



While the the led of "Done" on EGO1 is on, it means the bit file is written into the device and your circuit is implemented on its FPGA chip, Congratulations!!

Is your circuit functioning properly ? Testing it on the EGO1 board.

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A 8-INPUTS-8-OUTPUTS CIRCUIT ON EGO1

lab1_sw_led_8.v

```
module lab1_sw_led_8(
    input [7:0] sw,
    output [7:0] led
    );
    assign led=sw;
endmodule
```

lab1_sw_led_8_sim.v

```
`timescale 1ns / 1ps

module lab1_sw_led_8_sim( );

reg [7:0] tb_sw=24'h000000;
wire [7:0] tb_led;

lab1_sw_led_8 usrc1(
.sw(tb_sw),
.led(tb_led)
);

always #10 tb_sw=tb_sw+1;
endmodule
```

lab1_ego1.xdc

```
set_property IOSTANDARD LVCMOS33 [get_ports {led[7]}]
...
set_property IOSTANDARD LVCMOS33 [get_ports {led[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw[7]}]
...
set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
set_property PACKAGE_PIN F6 [get_ports {led[7]}]
...
set_property PACKAGE_PIN K2 [get_ports {led[0]}]
set_property PACKAGE_PIN P5 [get_ports {sw[7]}]
...
set_property PACKAGE_PIN R1 [get_ports {sw[0]}]
```

Q: If “lab1_sw_led_8_sim.v” is removed from the Vivado project, will the circuit on the FPGA chip work or not?

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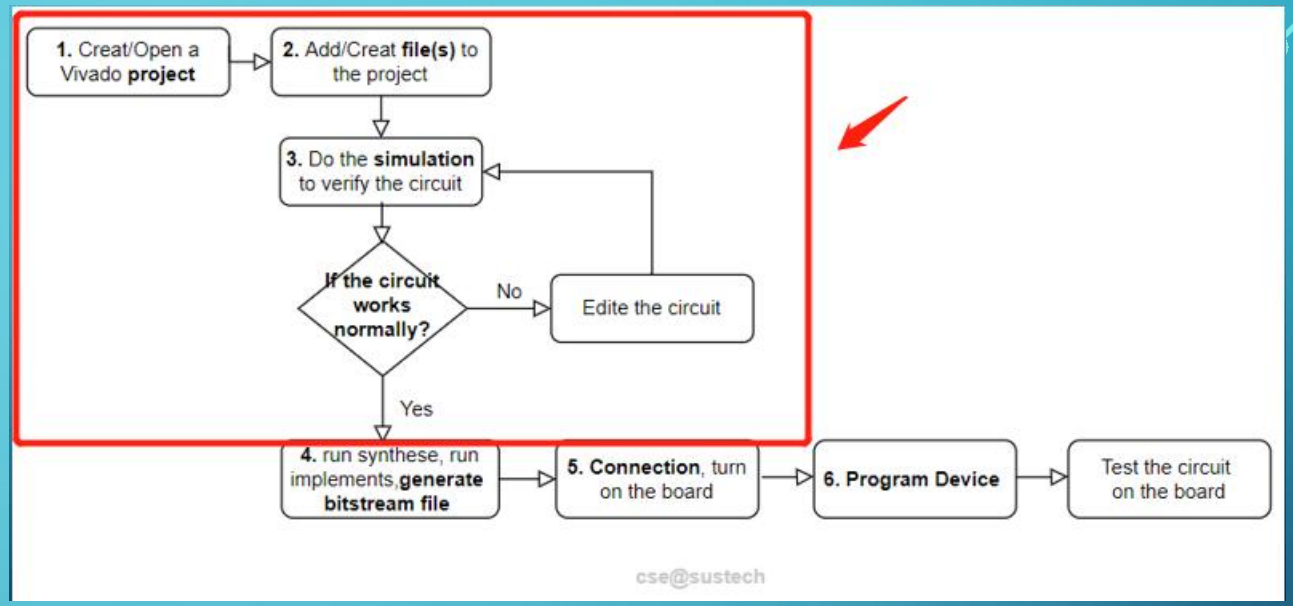
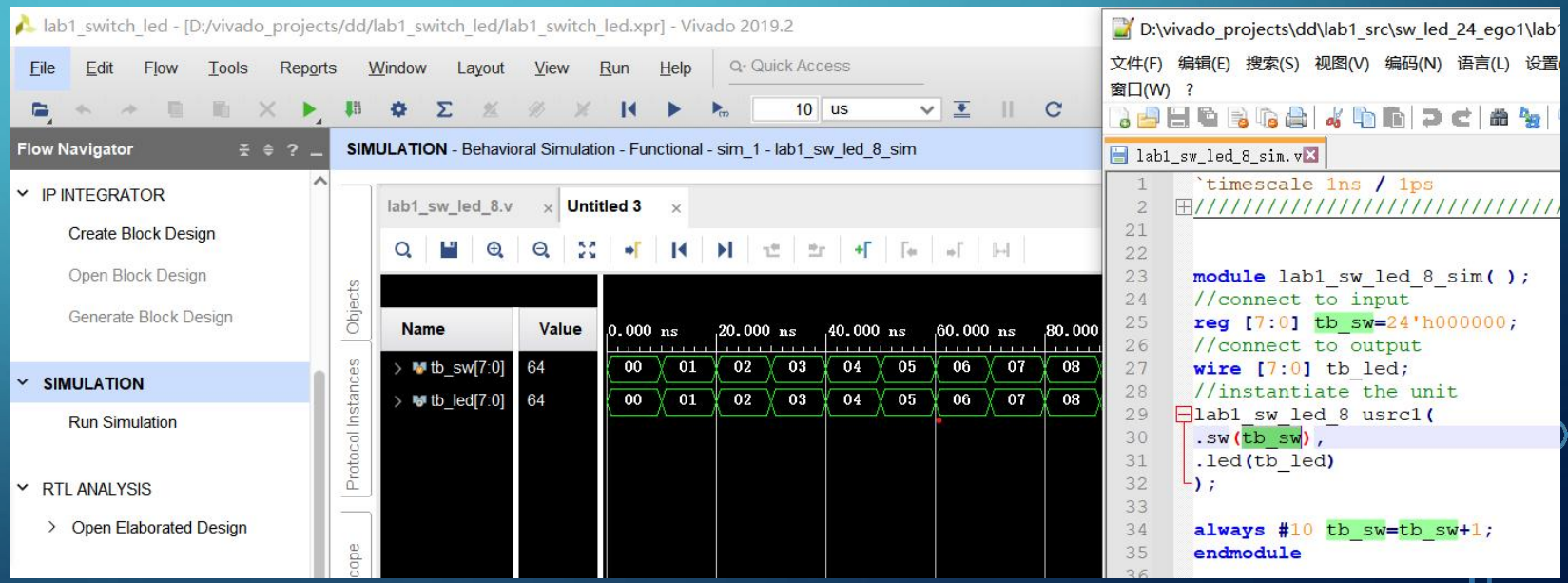
PRACTICE1

- If you have NOT got the board(with FPGA chip embeded), do practice1, following the steps shown in the top figure on the right side.
- A waveform would be generated to show the logic relationship between the input and output of the designed circuit.
- Is the logic relationship shown in the waveform same with your design?





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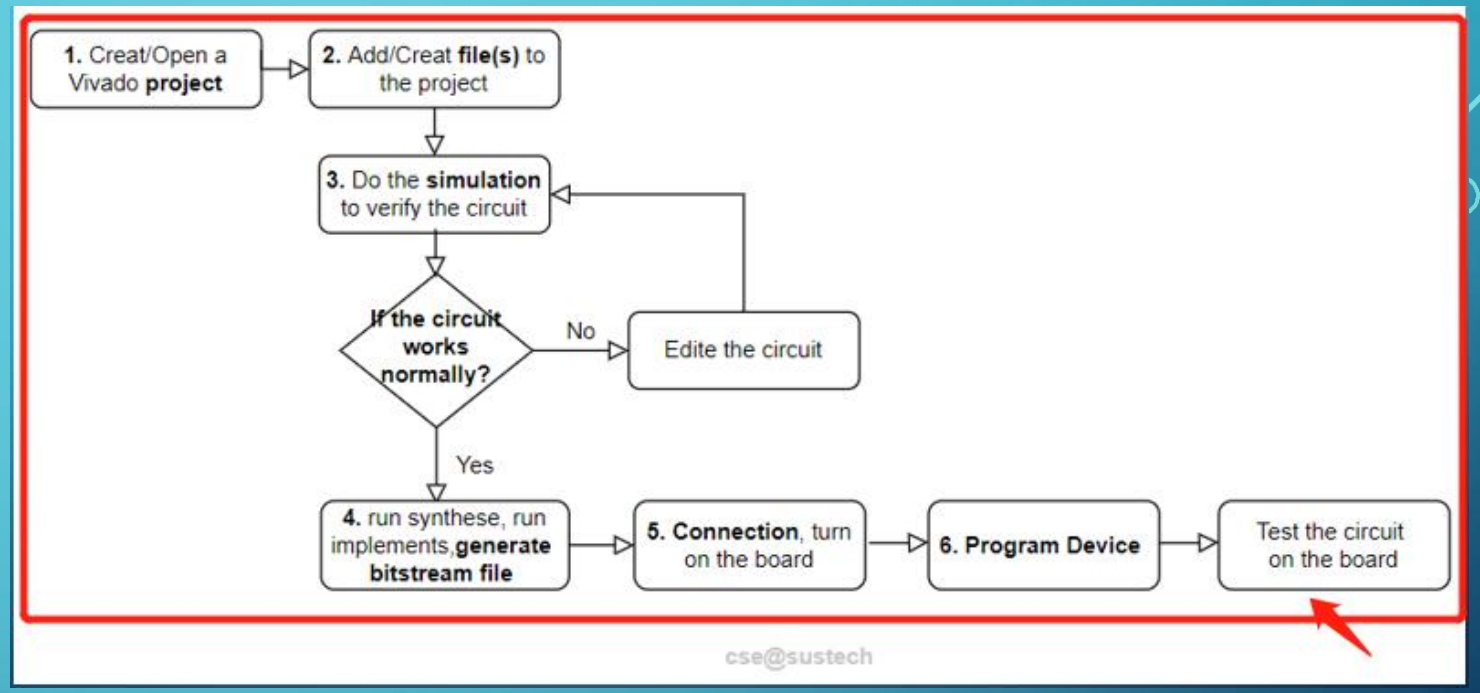
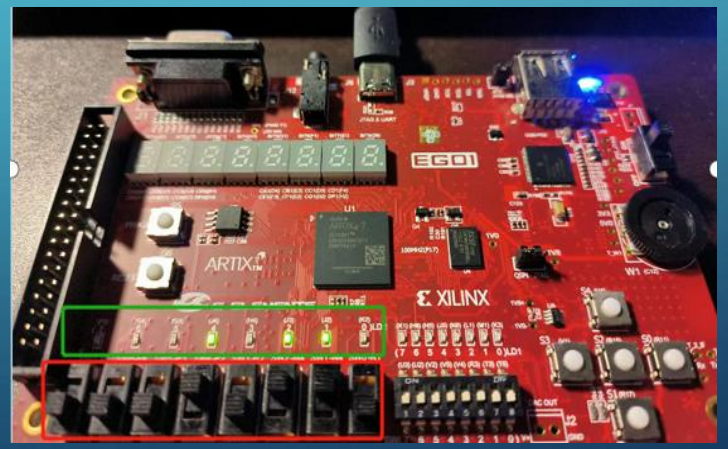
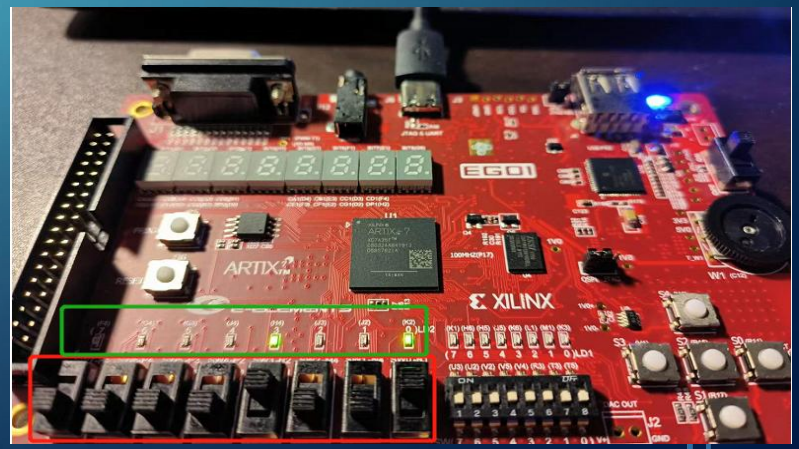
PRACTICE2

- If you HAVE got the board(with FPGA chip embeded), do practice2, following the steps shown in the top figure on the right side.
- Test the designed circuit on the board, change the input(here is the dail switch of EGO1) to absert to state of output(here is the led of EGO1).
- Is the logic relationship between the input and the output same with your design?







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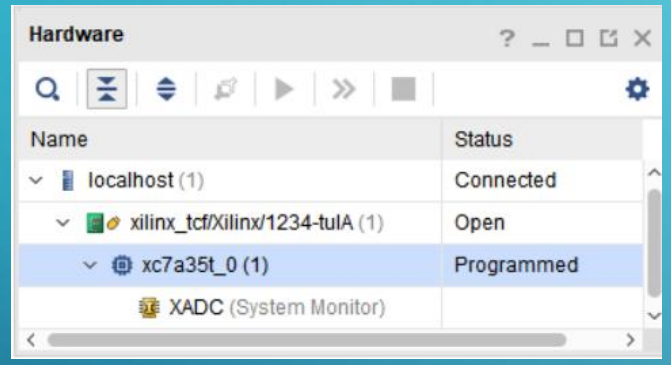
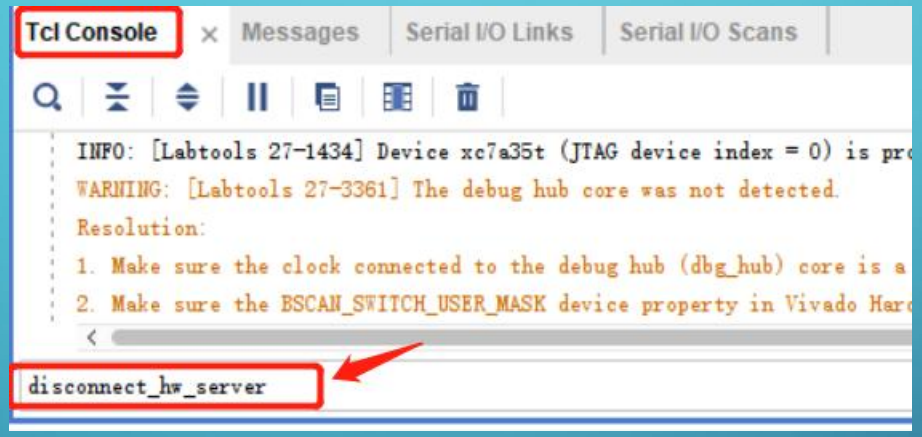
TIPS1: HOW TO DO THE DISCONNECTION

After the using EGO1 board, it is strongly suggested to follow the following steps(**MUST do Step1 befor Step2**) to do the disconnection:

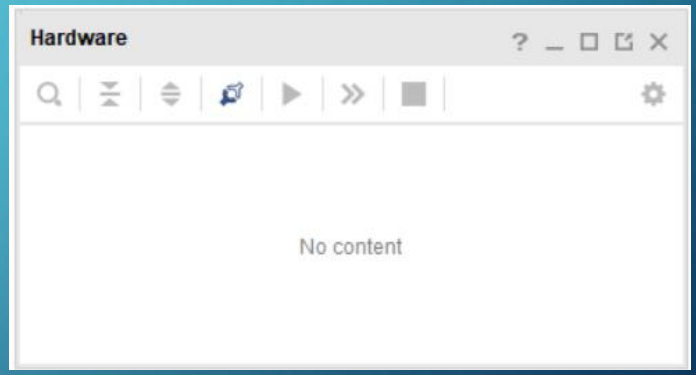
Step1. 'disconnect' the vivado project and the FPGA chip: run the command "disconnect_hw_server" in the Tcl Console window of vivado project



before the 'disconnection'



do the 'disconnection' between vivado project and FPGA chip



after the 'disconnection'

Step2: disconnect the PC and the EGO1 board : turn off the EGO1 board, then disconnect the PC and the EGO1 board.

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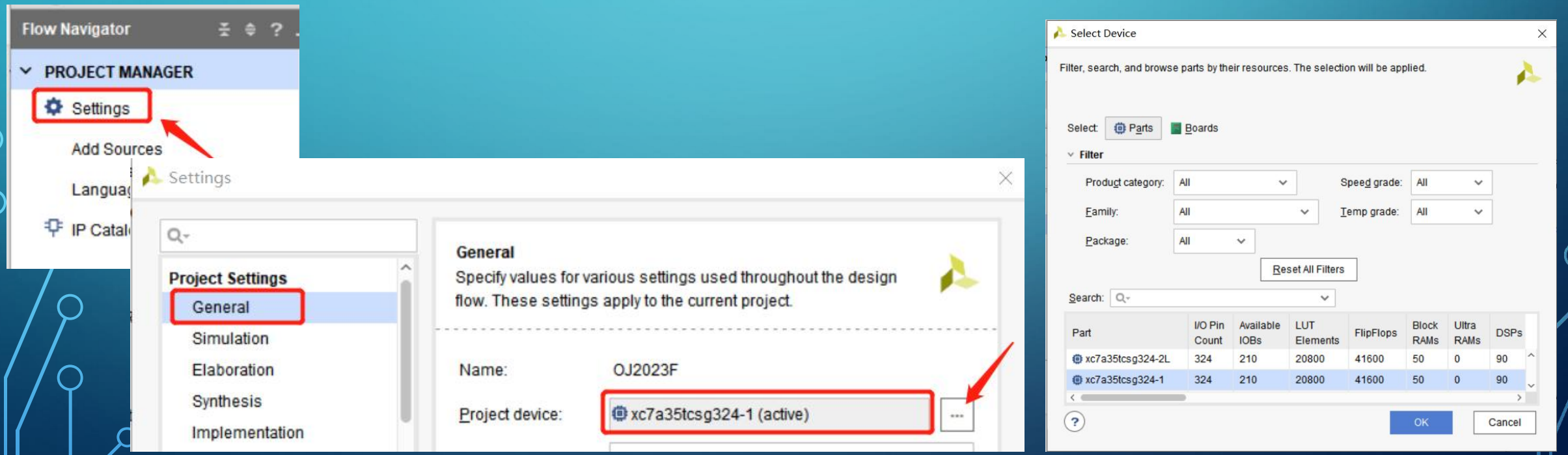
TIPS2: HOW TO RESET THE DEVICE IN VIVADO(1)

If the ‘Project device’ needs to be reset in the vivado project, do the following steps:

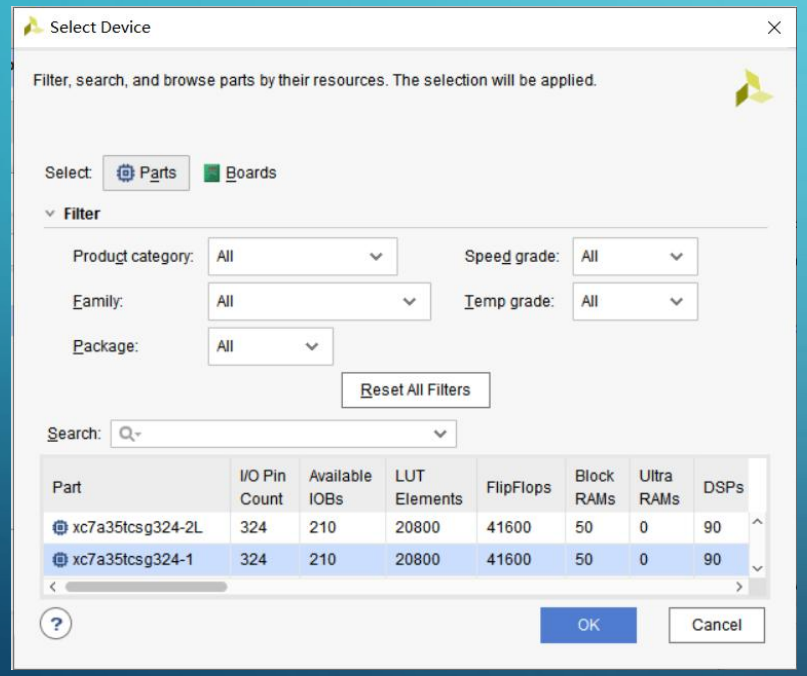
Step1. Click the “Settings” of “**PROJECT MANAGER**” in “**Flow Navigator**” to invoke the “Settings”.
Step2. Click “General” , then click the “...” button on the right side of “Project device” to invoke the “Select Device”

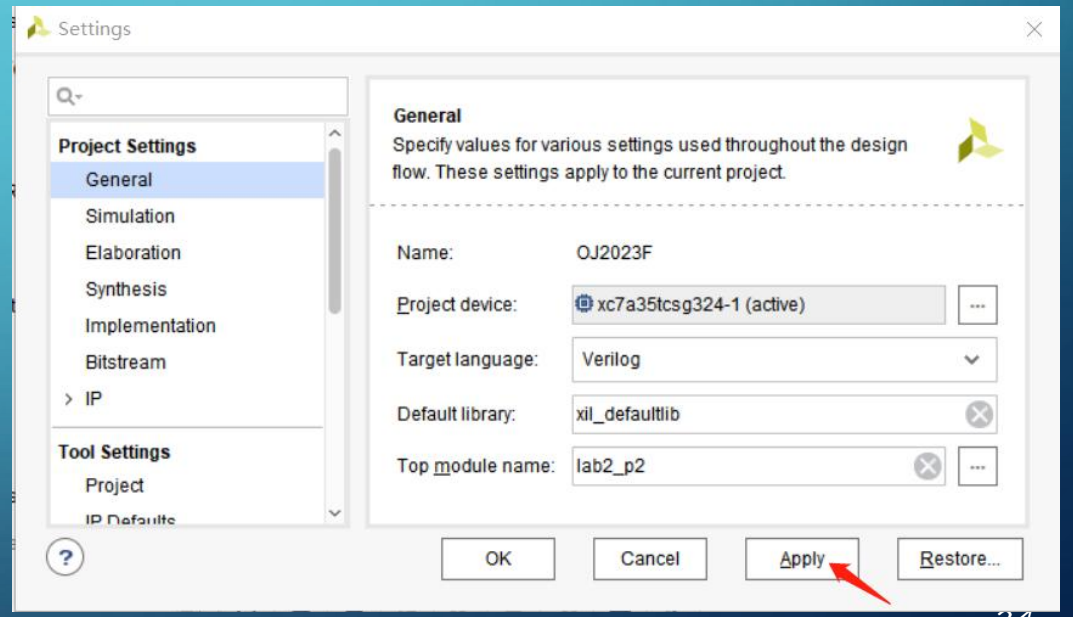


TIPS2: HOW TO RESET THE DEVICE IN VIVADO(2)

Step3. Select the chip-type of the FPGA chip which would be programed with the bitstream file(the bitstream file is generated based on the vivado project), then click "OK"

Step4. Click "Apply" button in the "Settings" window to finish the resetting(s).





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