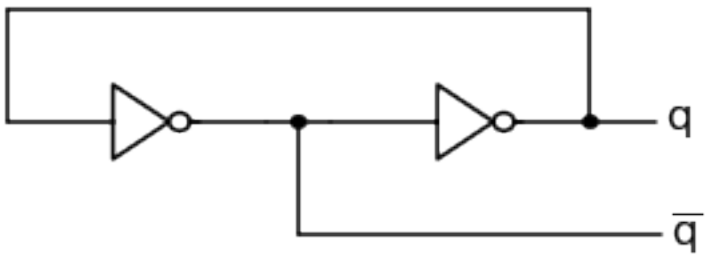
06-LAT-Memory_FlipFlops

August 22, 2019

1 06 - LAT - Memory & FlipFlops

1.1 Latch

The simplest memory element consists of two inverters. The inverters are lloped so that the saved signal is trapped.



1.2 SR-Latch

$$q = s + \overline{r}q$$

s	r	q	$\overline{q}$	Function
0	0	unchanged	unchanged	Storage
0	1	0	1	Set to Zero
1	0	1	0	Set to One
1	1	0	0	Not allowed

1.3 D-FlipFlop

1.4 E-FlipFlop

1.5 T-FlipFlop