Time	0 100 ns 200 m	ns 300 ns 400 hs	hs 500 hs 600	ts 700 ts 80	tis 900 tis	us 1100 tis	1210 ts 1310	ds 1400 nds	1500 ns	1600 ns 1700 ns	1800 ns
en=0			, , , , , , , , , , , , , , , , , , , ,								
			innandaanar			danaadaa			7000000		
in_portA[31:0]=0	0 Y1 Y2 Y3	Y4 Y5 Y6 Y	V7 Y8 Y9 Y10	Y11 Y12 Y13	Y14 Y15 Y16	Y17 Y18 Y19	Y20 Y21	Y22 Y23 Y2	4 Y25 Y26	Y27 Y28	Y29 Y30
in_portB[31:0]=0	0 Y2 Y3 Y4	V5 V6 V7 V	X8 Y9 Y10 Y11	V12 V13 V14	V15 V16 V17	V18 V19 V20	Y21 Y22	X23 X24 X2	5 <b>X</b> 26 <b>X</b> 27	Y28 Y29	X30 X31
	0 X3 X4 X5	X6	X9 Y10 Y11 Y12	V13 V14 V15	V16 V17 V18	V19 V20 V21	Y22 Y23	X24 X25 X2			X31 X32
m_clk=0				П						, a , , , a	_ \( \)
port_out[31:0]=0	0	4 X5 X4 X5 X6 X5 X6 X7 X6 X7 X8	X8 X7 X8 X9 X8 X9 X+ X9 X+ X+	<del>\( \) \( \)</del>	<del>\( \) \( \)</del>	X+ X	(+ X+	X+ X+ X+ X+ X+ X+ X+	X+ X+ X+ X+ X+ X+ X+	X+ X+ X+ X+ X+ X+ X	+ X+ X+ X+ X+ X+ X
interBank_data_ram0[31:0]=0		(4 X5 X4 X5 X6 X5 X6 X7 X0							X+ X+ X+ X+ X+ X0		
interBank_data_ram1[31:0]=0			<u>/8                                    </u>	X+ X+ X+ X0						<u> </u>	+ \( \tau + \( \tau + \( \tau + \( \tau + \) \)
interBank_data_ram2[31:0]=0	0			X+ X+ X+ X+ X+ X+ X+	<del>X+ X+ X+ X+ X+ X+ X+ X</del> 0						
interBank_data_ram3[31:0]=0	0					<u> </u>	<del>(+ \( \) + \( \) + \( \) + \( \) + \( \) 0</del>				
ram_sel[1:0]=0	0	χ1		χ2	χ3		X0		χ1		
page_addr_ram0[4:0]=0	0 <u>X1 X2 X3 X4 X5 X6 X</u> 7	7 X8 X9 X+ X+ X+ X+ X+ X0		,	<u> </u>		χ1	X2 X3 X4 X5 X6 X7 X8	X9 X+ X+ X+ X+ X0		
page_addr_ram1[4:0]=0	0		<u> </u>	<del>X+ X+ X+ X</del> 0						<u> </u>	7 X8 X9 X+ X+ X+ X
page_addr_ram2[4:0]=0	0				<u> </u>						
page_addr_ram3[4:0]=0	0				X	X2 X3 X4 X5 X6 X7 X8 X	(9 <b>X</b> + <b>X</b> + <b>X</b> + <b>X</b> + <b>X</b> 0				