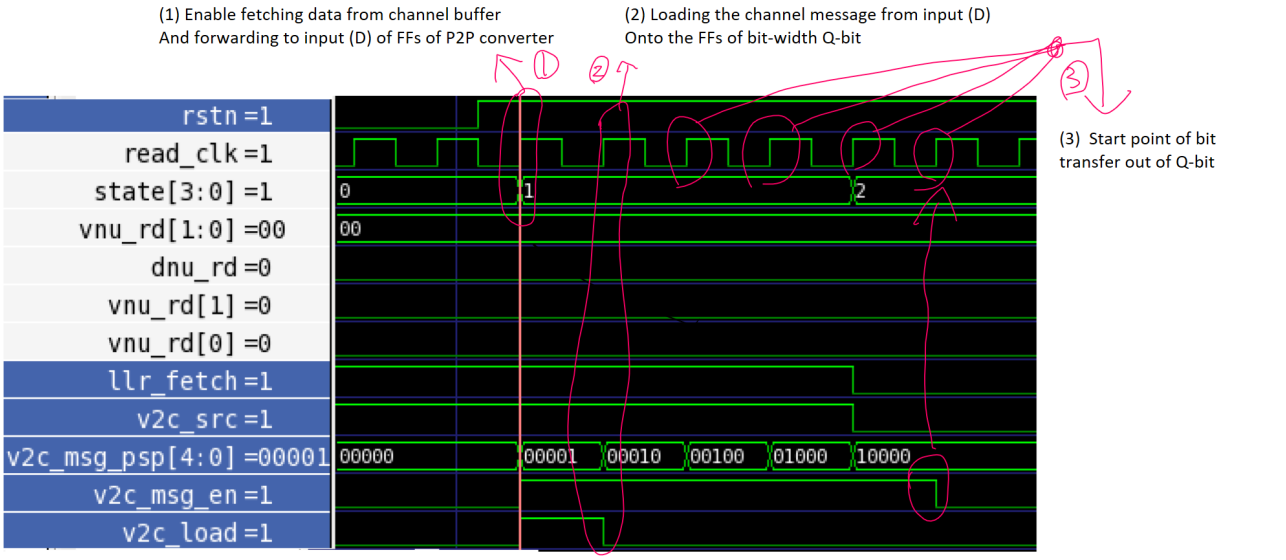
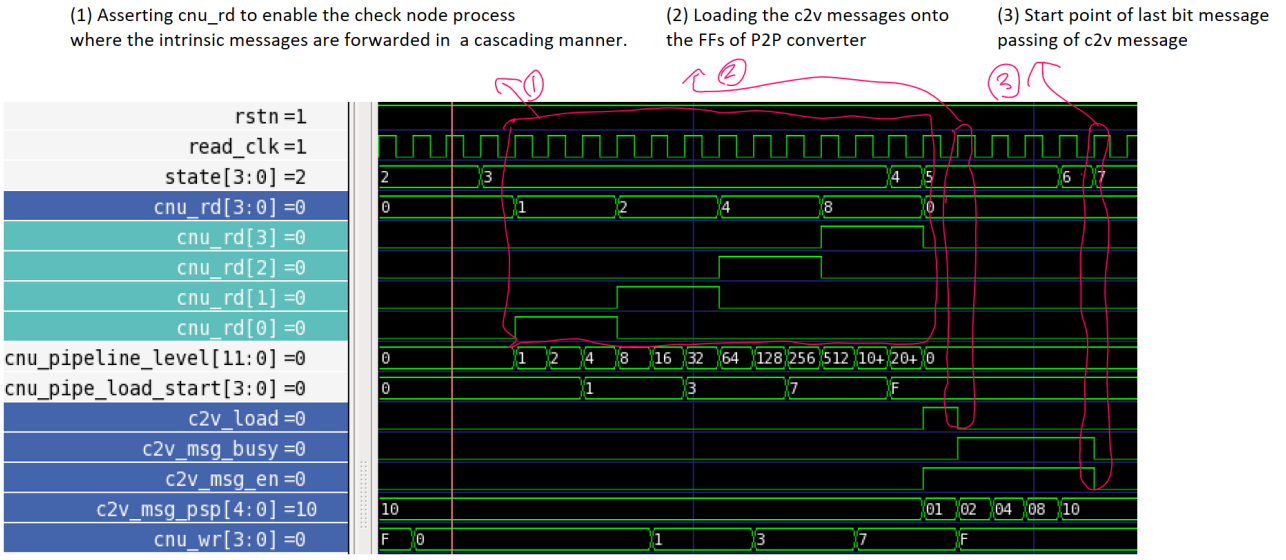
Control Signals – Initially loading channel message and message passing to CNU

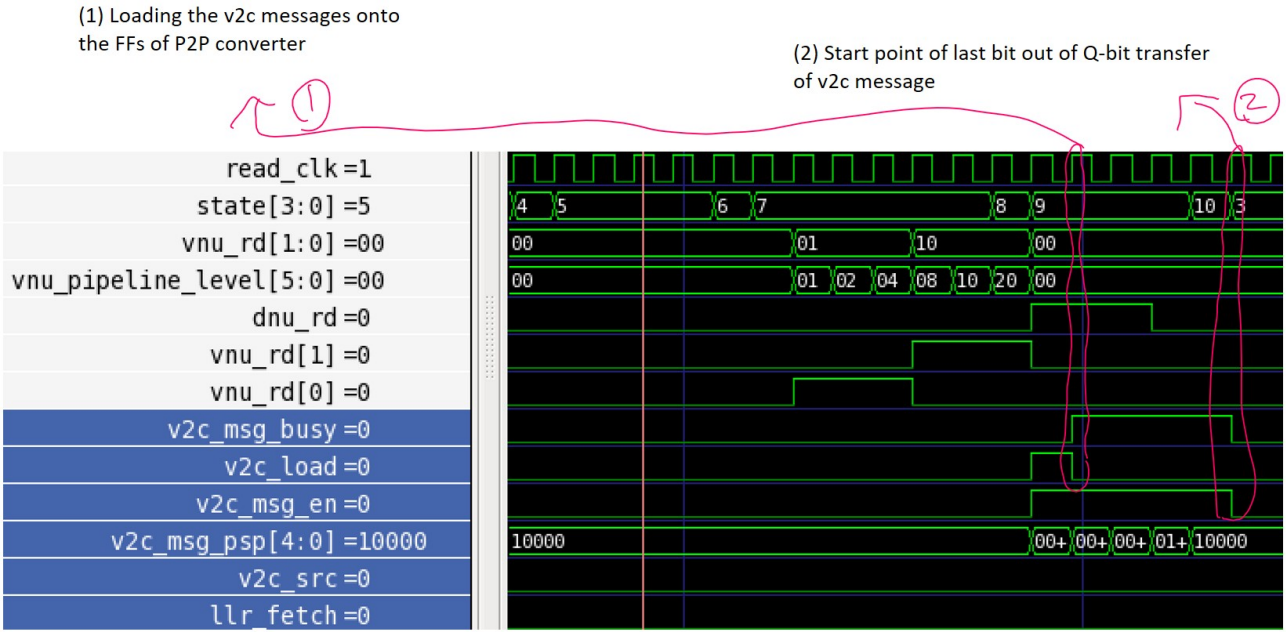
- **Signal instantiation:** llr_fetch, v2c_src, v2c_msg_en, v2c_load
- Note
  - Although one codeword decoding process is only required fetching the channel messages from channel buffer in one clock cycle, the llr_fetch is still asserted for four rising edges of read clock. This is because the propagation delay from channel buffer till VNUs may be so long that message passing cannot be completed in one clock cycle. Thus the additional Q-bit registers of depth 4 are inserted in between.



- **Signal instantiation:** cnu_rd, c2v_load, c2v_msg_busy, c2v_msg_en and c2v_msg_psp



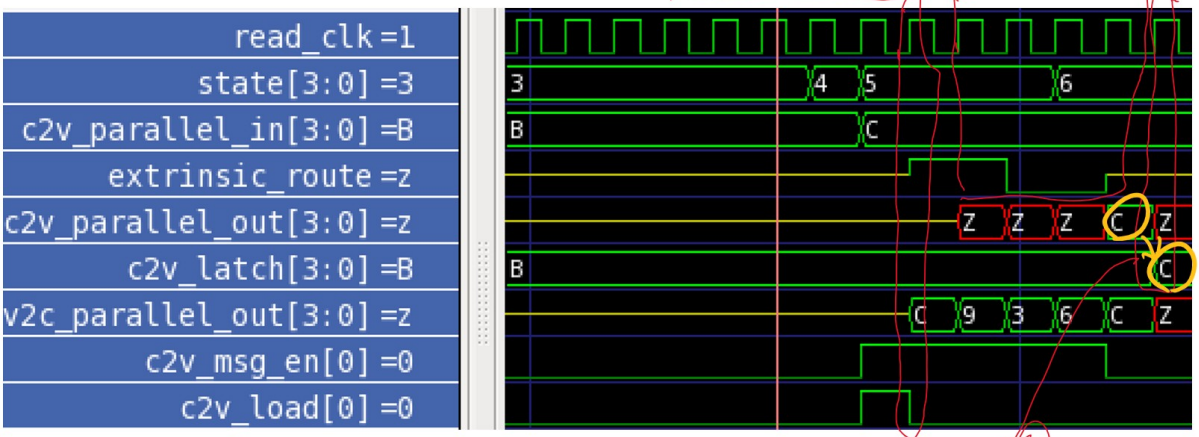
- **Signal instantiation:** v2c_msg_busy, v2c_load and v2c_msg_en



Signal instantiation: c2v_parallel_in, extrinsic_route, c2v_parallel_out, c2v_latch, c2v_msg_en, c2v_load

(1) PSP convert latched the c2v_load control signal and load the c2v message from last 2-LUT of CNU

(2) Transmitting c2v message in a bit-serial manner, started from MSB.



(3) Once clock cycle right after completion of transmission, the c2v buffer latches the received c2v parallel message which will be fetched by VNU. That is, c2v_latch latches the data from c2v_parallel_out