Test Plan for Base Port





Test Plan for Base Port

1 Outline

This document is for the Base Port (including MSL) in Linux kernel of MVF TOWER BOARD (XTWR-VF600) with VF6XX SoC, and describes test plan for each API and feature of such unit.

2 Test Environment

Toolchain: The latest Linaro toolchain

Bootloader: u-boot 2011.12

Kernel: Freescale i.MX Rootfs: rootfs on NFS Freescale i.MX Linux 3.0.15 kernel

3 Target Module of the Test

Platform Core

MSL

Posix Timer

Clock

NOTE:

Memory map of peripheral devices must be able to access to relevant driver

Tests of driver-dependent codes are included in the test of each driver (IOMUX, GPIO. DMA and such).

4 Test Plan

Carry out both basic test using busybox/memtool and test by LTP.

5 Test Tools

busybox

memtool

ltp

NOTE:

memtool command is ported from the imx-test-12.03.00 package of sample BSP (L3.0.15_12.03.00_SS_source.tar.gz).

LTP is Timesys LinuxLink ltp-20100430.

Refer to the following page for details of LTP.

http://ltp.sourceforge.net/

Test Plan for Base Port Datails

No.	Head	Item	Procedure	Points to be checked	Judge	Note
1	Clock/posix timer	Clock, posix timer	Execute following command on the target's console. # date; sleep 60; date	Sleep command terminates after specified periods. (time with a stopwatch) Verify time course of sleep by comparing date command output between before and after sleep command.		
2	Memory	Read/write	# ./memtool -32 0x82000000 1 # ./memtool -32 0x82000000=0xAABBCCDD	Arbitrary memory address (that is free of untoward effects) can be read and written.		
3	L2 Cache	L2 Cache	Boot kernel (with CONFIG_CACHE_L2X0 option enabled) on the target.	Kernel works properly.		
4	LTP	Basic functions of the kernel	Execute following commands on the target's console. # cd /usr/local/ltp # ./runltp	Implemented functions pass relevant tests in LTP.		