Test Plan for eDMA

Test Plan for eDMA

1 Outline

This document is for the eDMA driver in Linux kernel of MVF TOWER BOARD (XTWR-VF600) with VF6XX SoC, and describes test plan for each API/feature of such unit.

2 Test Environment

Toolchain: The latest Linaro toolchain
Bootloader: u-boot 2011.12
Kernel: Freescale i.MX Linux 3.0.15 kernel
Rootfs: rootfs on NFS

3 Target Module of the Test

eDMA

4 Test Plan

Create and use a new driver for DMA test.
Test will be done with DMATESTconfig enabled in kenel.

5 Conditions

Actual transfer test to device driver will be carried out as device drivers supporting DMA are enabled.

6 Testing Method

1. Preparation

Have the following setting in kernel configuration ON.
[*] DMA Engine support --->
<*> DMA Test client
Replace drivers/dma/dmatest.c with test_program/dmatest.c.

2. Execution method of Memcpy test

Test runs automatically as booting the kernel built by #1 above.

3. DMA CYCLIC transfer test

Enable the comment below (at the beginning of dmatest.c) by removing comment out, then compile and boot the kernel.
#define DMA_CYCLIC_TEST
Mount rootfs and check number of interruption by cat /proc/interrupt.
Number of completed interruption of cyclic transfer (9000 times approx) within 3000msec can be confirmed.

Test plan for eDMA

Datails

No.	Head	Item	Procedure	Points to be checked	Judge	Note
1	DMA Driver Test using dmatest.c	Driver initialization	Define eDMA resource.	Normal interrupt of eDMA0 (eDMA1 as well if enabled) and Err interrupt are installed in cat /proc/interrupt.	OK	Enable CONFIG_DMATEST (Enable driver/dma/dmatest.c)
2		DMA channel allocation	Allocate channel from driver module.	Channel is allocatable.	OK	
3		Execute memcpy function	Allocate two DMA buffers by driver module and transfer by memcpy function.	Transfer complete interrupt occurs. Transferred contents are identical.	OK	
4		Change in transfer parameter by device config	Configure word size by 4, 2, and 1 byte, and complete transfer.	Transfer complete interrupt occurs. Transferred contents are identical for each byte.	OK	
5		DMA CYCLIC transfer test	Transfer in CYCLIC mode.	Interrupt (estimated from total traffic and traffic for one transfer) increases at the time of transfer. All the elements of Scatter List are transferred.	OK	Modify to enable #define DMA_CYCLIC_TEST in dmatest.c and make it testable
6		Kernel output	Output DMA test module as kernel boots.	Memory transfer and buffer verification are successfully shown in boot message.	OK	Confirm 64 channel of output for DMA0/DMA1.