Tanay Sharma

tanays@umich.edu | +1(408)666-6065 | www.linkedin.com/in/tsha256/ | github.com/tsha-256

EDUCATION

University of Michigan | Ann Arbor, MI *Aug 2023 - May 2027*

BSE Electrical Engineering

Relevant Coursework: Computer Architecture, Microarchitecture, VLSI Design, Data Structures, Digital Signal Processing

Honors: Clara E. Mara merit scholarship, Ernest W. Reynolds Endowed Scholarship, Dean's List (all semesters)

SKILLS

Languages: C, C++, SystemVerilog, Python, Shell Scripting, Java, x86, ARM, RISC-V, Groovy

Tools: DC, Verdi, JasperGold, Virtuoso, HSpice, Innovus, Icarus Verilog, Yosys, GDB, Linux, Docker, Git, Makefile

EXPERIENCE

Systems Engineering Intern, *Stealth Startup* *May 2025 - Aug 2025*

- Created end-to-end system test framework to track performance metrics and verify changes
- Implemented embedded UDP broadcaster to efficiently stream data from a new sensor
- Optimized system boot process, reducing startup time by 60%

Instructional Aide, *University of Michigan CSE* *Aug 2024 - Present*

- Mentored 600+ students in digital logic and Verilog design/debugging
- Maintained website and autograder

AI Hardware Intern, *d-Matrix* *May 2024 - Aug 2024*

- Designed RTL to calibrate D2D interconnect of next-gen AI inference accelerator
- Developed toolkit for generating and optimizing custom TSMC SRAMs
- Reworked lint and CDC flow for static RTL verification

Research Assistant, *Quantum Engineering Lab, University of Michigan ECE* *Oct 2023 - May 2024*

- Architected a unified UI to automate and control optical test equipment (oscilloscope, DAQ, laser source)
- Eliminated ~4 hours of runtime from quantum IC data analysis program

Summer Intern, *Astera Labs* *Jun 2022 - Aug 2022*

- Benchmarked a tool to curb AWS costs for running Synopsys EDA tools
- DAC '23 research poster: "High Performance, Scalable and Cost Optimized AWS Cloud Infrastructure for Chip Development"

PROJECTS

Custom 16-Bit RISC Processor *Aug 2025 - Dec 2025*

- Developed custom 2-stage in-order pipeline processor
- Custom layout for RF, ALU, 2-way shifter, PC, decoder, and integration with memory

Advanced Out-of-Order RISC-V Processor *Feb 2025 - Apr 2025*

- Designed and tested an R10K-style RISC-V CPU with out-of-order & N-way superscalar execution, early branch resolution, load store queue, associative victim caches, G-share branch prediction, and instruction prefetching

Secure Embedded Satellite TV System *Jan 2025 - Apr 2025*

- Created U-M's first ever team for the MITRE embedded CTF. Led team of 30 students
- Developed a system to encrypt TV data for only authorized receivers, and attacked other university designs
- Won 3rd place out of 116 teams, beating seasoned teams including UIUC, MIT, UCLA, IIT Madras

Pipelined LC2K Microprocessor FPGA Design *Nov 2024 - Jan 2025*

- Designed RTL for a pipelined in-order processor using the LC2K educational ISA