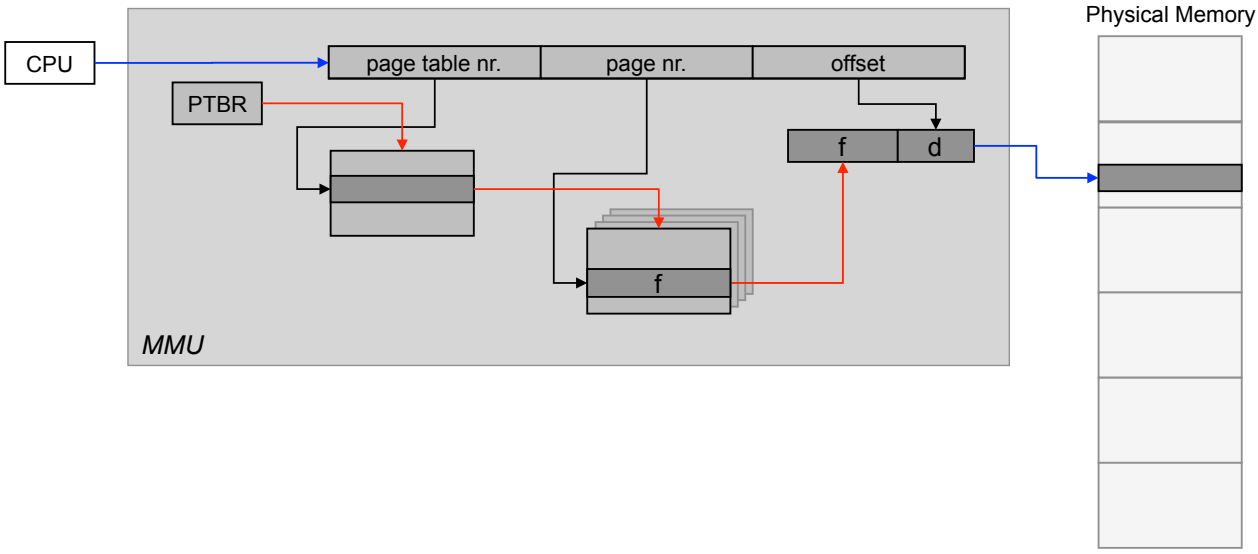
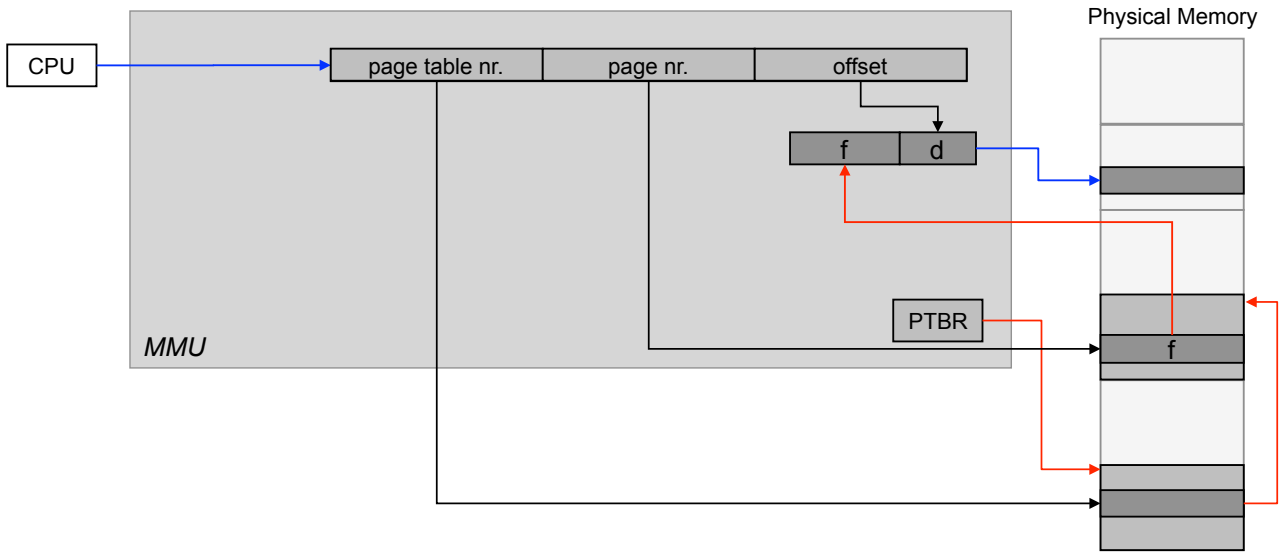
Translation Lookaside Buffers

- Page table lookups are expensive!
- Caching of page table entries
- Translation Lookaside Buffers (TLBs)
- Software-managed TLBs: MIPS

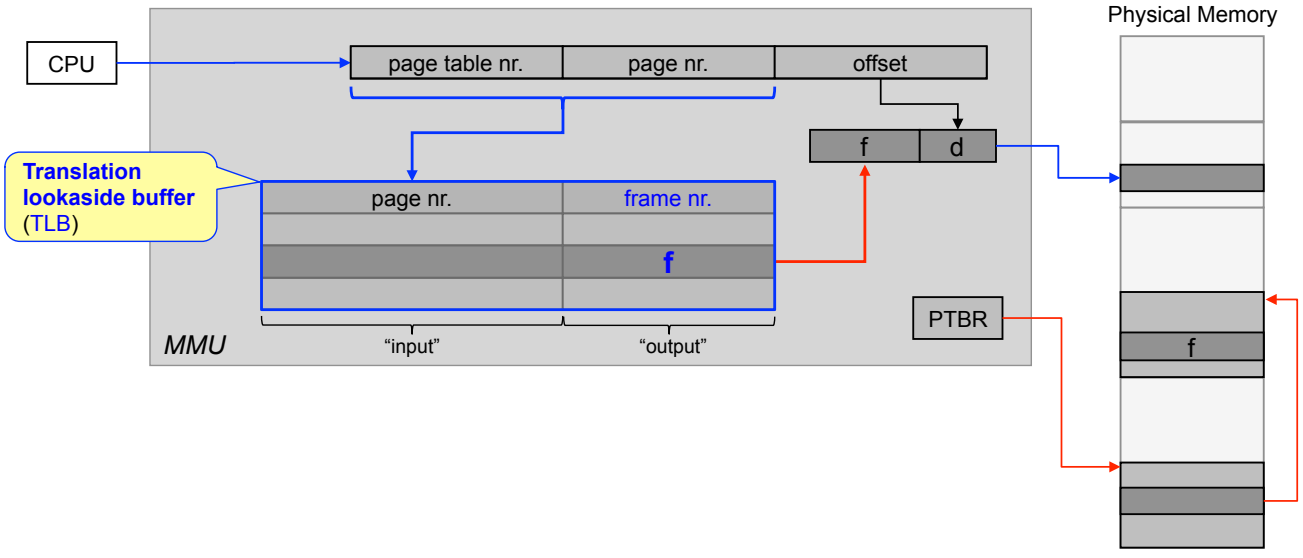
Recall: Address Translation for Two-Level Paging



Recall: Address Translation for Two-Level Paging



Solution: Translation Lookaside Buffers



Memory Translation with a TLB

page nr.	frame nr.
	f

1. Split virtual address, use page number.
2. Look in the TLB to see if we find translation entry for page.
   - If YES, use frame number.
   - If NO, system must locate page entry in main-memory-resident page table, load it into TLB, and start again.

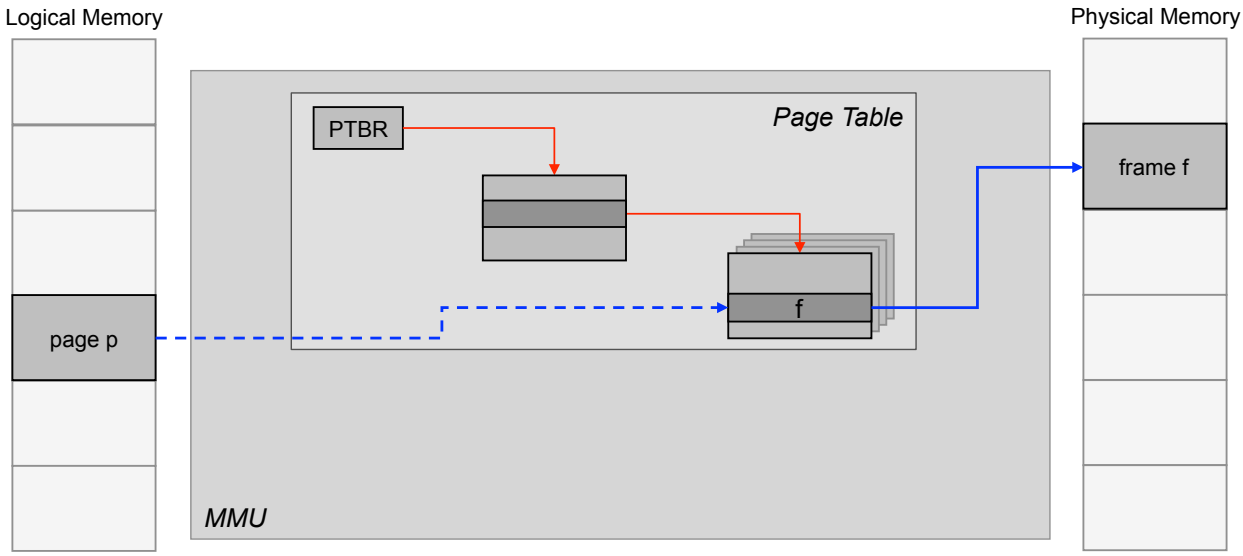
Parameters of the TLB

page nr.	frame nr.
	f

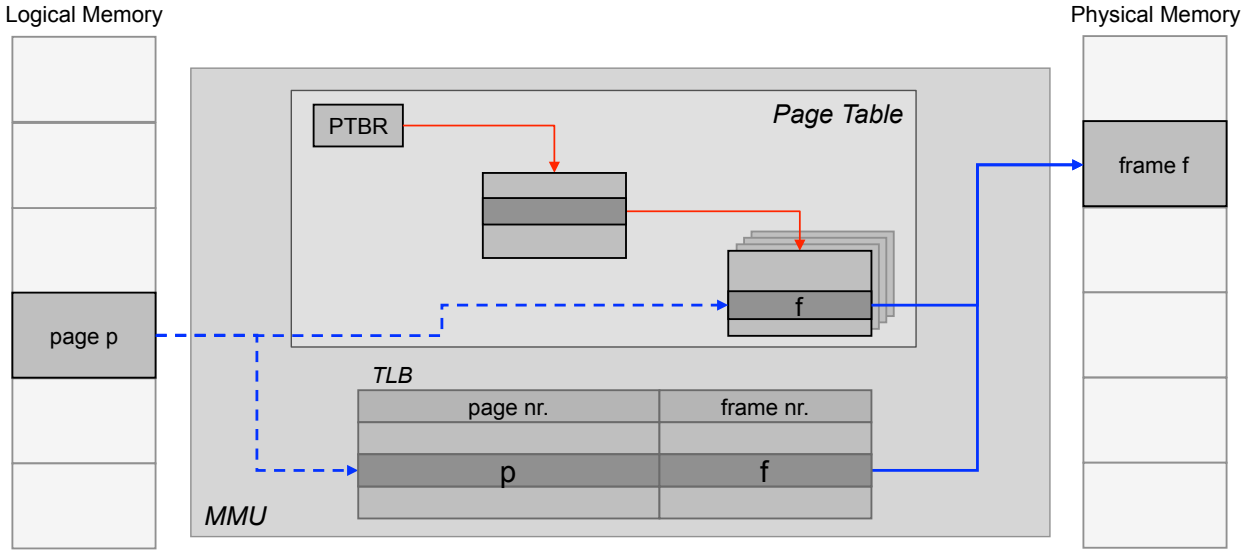
Parameters of TLBs

- Size: 12 – 4096 entries
- Lookup latency: 0.5 – 1 clock cycles
- Miss penalty: 10 – 100 clock cycles
- Target miss rate: 0.01% – 1%

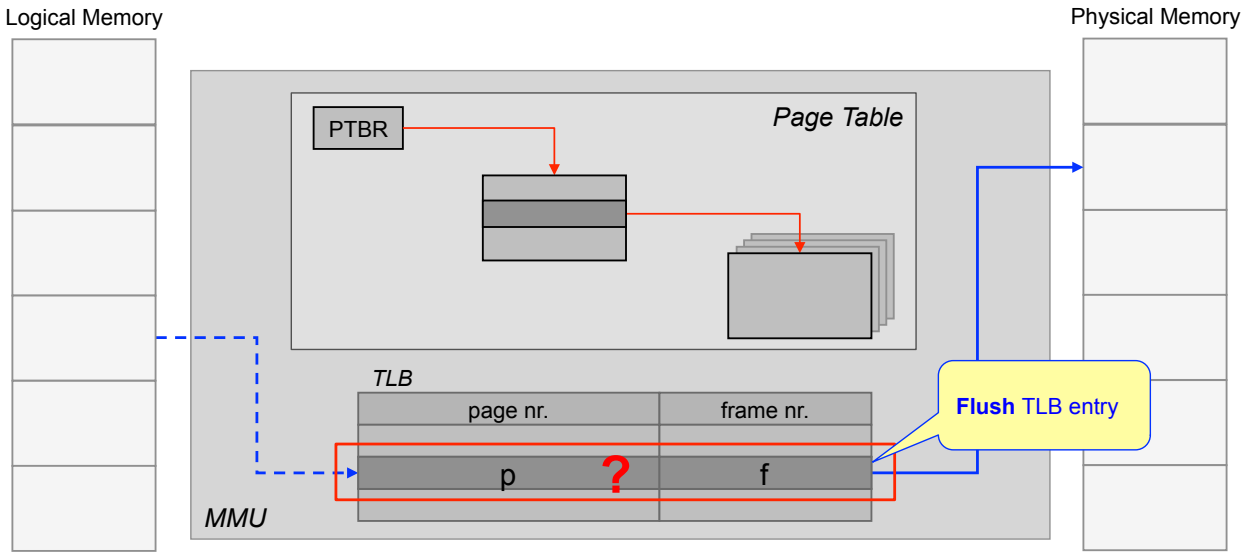
Freeing TLB Entries



Freeing TLB Entries



Freeing TLB Entries



How many TLBs?

One TLB per address space (process)

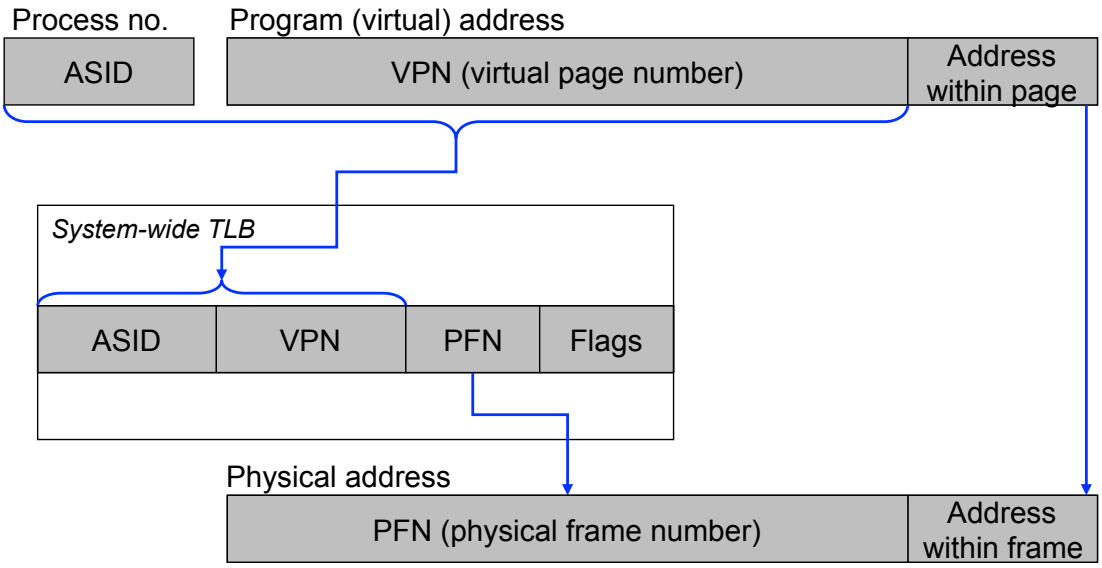
page nr.	frame nr.
	f

Need to flush TLB for every process switch.

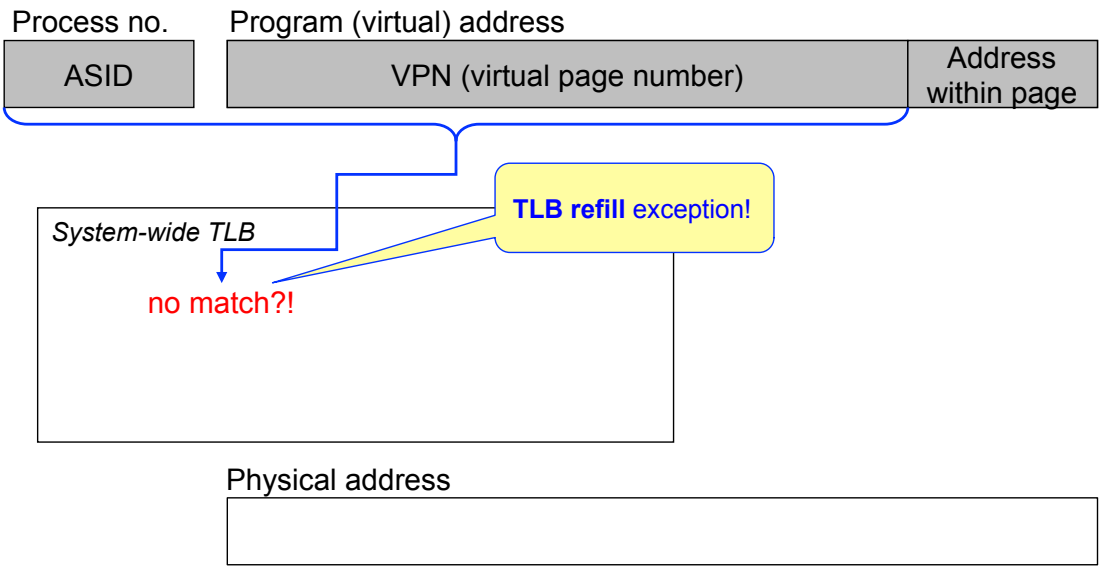
One TLB for entire system

address space id	page nr.	frame nr.
		f

Software-Managed TLBs: Paging - MIPS Style



Software-Managed TLBs: Paging - MIPS Style



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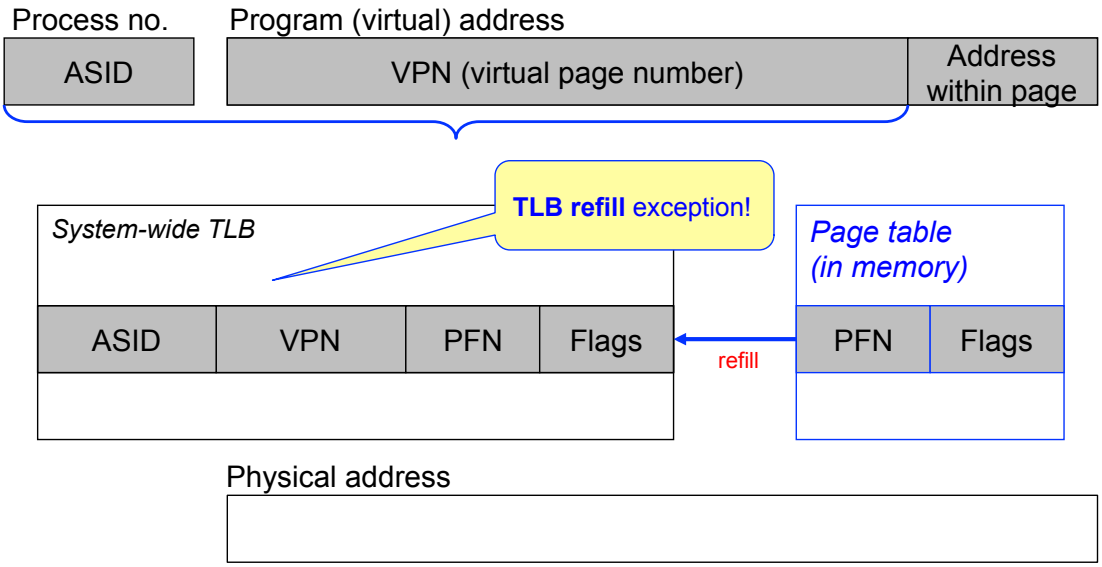
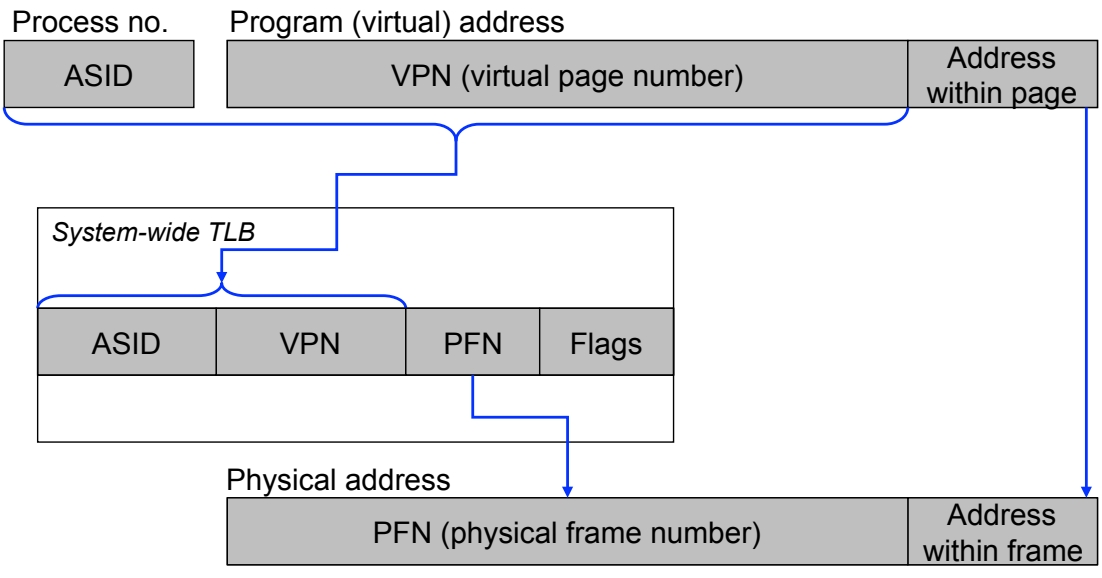
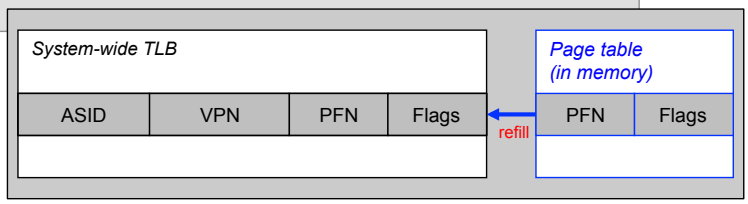


Software-Managed TLBs: Paging - MIPS Style



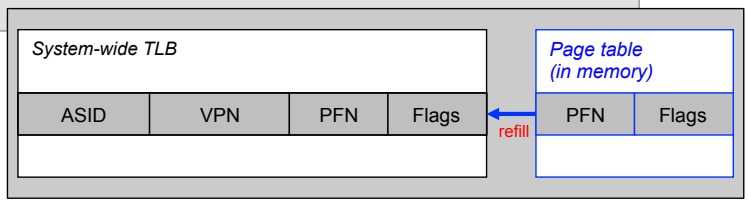
Memory Translation -- MIPS Style

- Principle: Make do with as little hardware as possible.
- Apart from a register with the ASID, the MMU is just the TLB.
  - The rest is all implemented in software!
- When TLB cannot translate an address, a special exception (TLB refill) is raised.
  - Software then takes over.



Software managed TLBs: TLB Refill Exception

1. Figure out if this virtual address is valid.
   - If not, trap to handling of address errors.
2. If address is valid, construct TLB entry.
3. If TLB already full, select an entry to discard.
4. Write the new entry into the TLB.



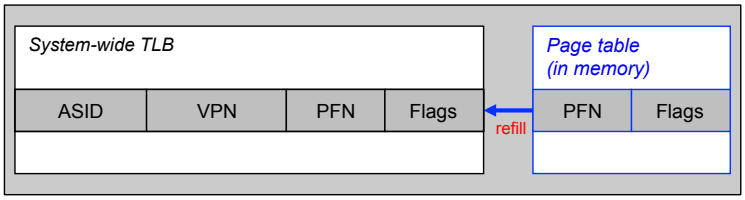
The MIPS TLB: TLB Entry Fields

input

- VPN: Virtual page number
- ASID: identifies the address space
- G: if set, disables the matching with the ASID

output

- PFN: Physical frame number
- N: cacheable / non-cacheable
- D: "write-control" bit (set to 1 if writeable)
- V: valid bit



TLBs: Summary

- Translation Lookaside Buffers (TLBs)
- Page table lookups are expensive!
- Caching of page table entries
- Hardware-managed vs. Software-managed TLBs
- TLBs on the MIPS