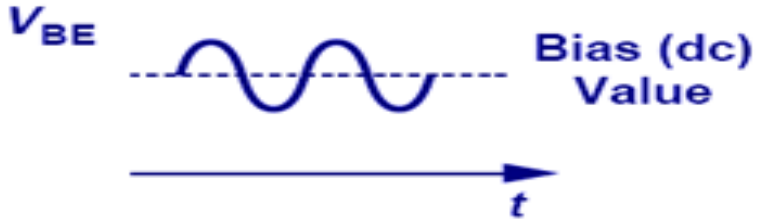
Small Signal Analysis of BJTs Amplifiers

BJT Amplifier Design

- *A BJT amplifier circuit should be designed to*
  1. Ensure that the BJT operates in the active mode,
  2. Allow the desired level of DC current to flow, and
  3. Couple to a small-signal input source and to an output "load".

→ **Proper "DC biasing" is required!**
(DC analysis using large-signal BJT model)

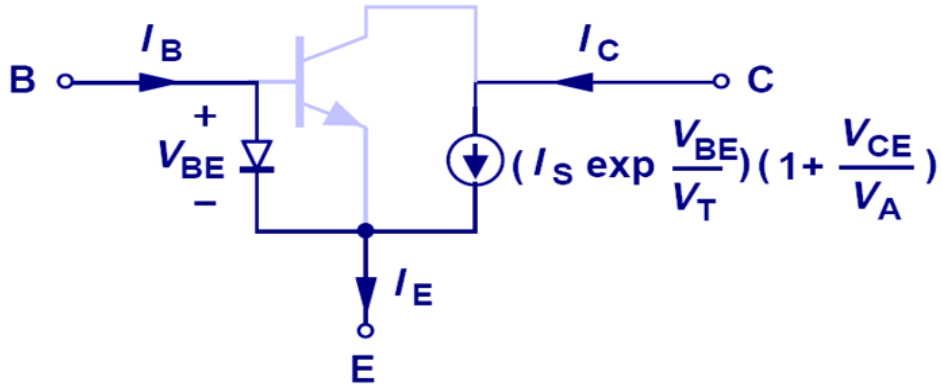


- **Key amplifier parameters:**
(AC analysis using small-signal BJT model)

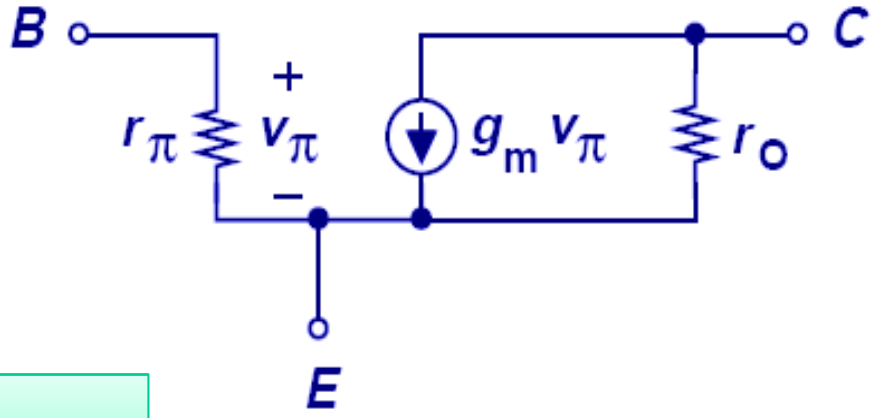
  - **Voltage gain $A_v \equiv v_{out}/v_{in}$**
  - **Input resistance R_{in}** ≡ resistance seen between the input node and ground (with output terminal floating)
  - **Output resistance R_{out}** ≡ resistance seen between the output node and ground (with input terminal grounded)

Large-Signal *vs.* Small-Signal Models

- The large-signal model is used to determine the DC operating point (V_{BE}, V_{CE}, I_B, I_C) of the BJT.



- The small-signal model is used to determine how the output responds to an input signal.



Small Signal Analysis of BJT

For the amplifier circuit analysis:-

a) Ac current gain

b) Voltage gain

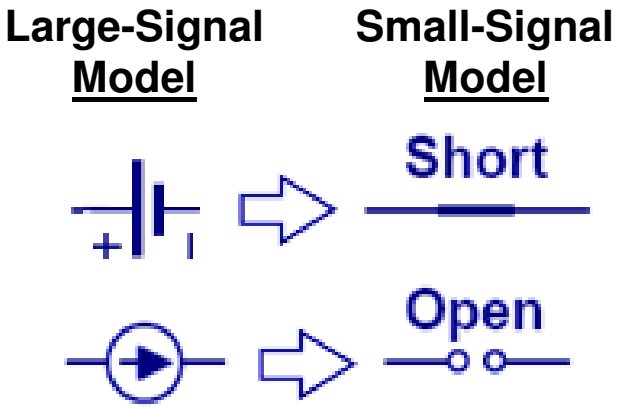
c) Input Impedance

d) Output Impedance

Small-Signal Models for Independent Sources

- The voltage across an independent voltage source does not vary with time. (Its small-signal voltage is always zero.)

  It is regarded as a short circuit for small-signal analysis.



- The current through an independent current source does not vary with time. (Its small-signal current is always zero.)

  It is regarded as an open circuit for small-signal analysis.

Comparison of Amplifier Topologies

Common Emitter

- **Large $A_v < 0$**
  - Degraded by R_E
  - Degraded by $R_B/(\beta+1)$
- **Moderate R_{in}**
  - Increased by R_B
  - Increased by $R_E(\beta+1)$
- **$R_{out} \cong R_C$**
- **r_o degrades A_v, R_{out}** but impedance seen looking into the collector can be "boosted" by emitter degeneration

Common Base

- **Large $A_v > 0$**
  - -Degraded by R_E and R_S
  - Degraded by $R_B/(\beta+1)$
- **Small R_{in}**
  - Increased by $R_B/(\beta+1)$
  - Decreased by R_E
- **$R_{out} \cong R_C$**
- **r_o degrades A_v, R_{out}** but impedance seen looking into the collector can be "boosted" by emitter degeneration

Emitter Follower

- **$0 < A_v \leq 1$**
  - Degraded by $R_B/(\beta+1)$
- **Large R_{in}** (due to $R_E(\beta+1)$)
- **Small R_{out}**
  - Effect of source impedance is reduced by $\beta+1$
  - Decreased by R_E
- **r_o decreases A_v, R_{in}, and R_{out}**

BJT Small Signal Analysis

In transistor r_e model:

(Common Emitter Configuration)

a) **Fixed Bias**
b) **Voltage divider**
c) **Emitter Follower Configuration**
d) **Common-Base Configuration**

BJT Small Signal Analysis

- $\mathbf{r_e}$ transistor model – employs a diode and controlled current source to duplicate the behavior of a transistor in the region of interest.

- The $\mathbf{r_e}$ and hybrid models will be used to analyze small-signal AC analysis of standard transistor network configurations.

Ex: Common-base, common-emitter and common-collector configurations.

- *The network analyzed represent the majority of those appearing in practice today.*

Circuit for Small Signal Analysis

AC equivalent of a network is obtained by:

1. **Setting all DC sources to zero**
2. **Replacing all capacitors by s/c equiv.**
3. **Redraw the network in more convenient and logical form**

In realistic and useful electronic circuit, the input can be decomposed into two separate components:

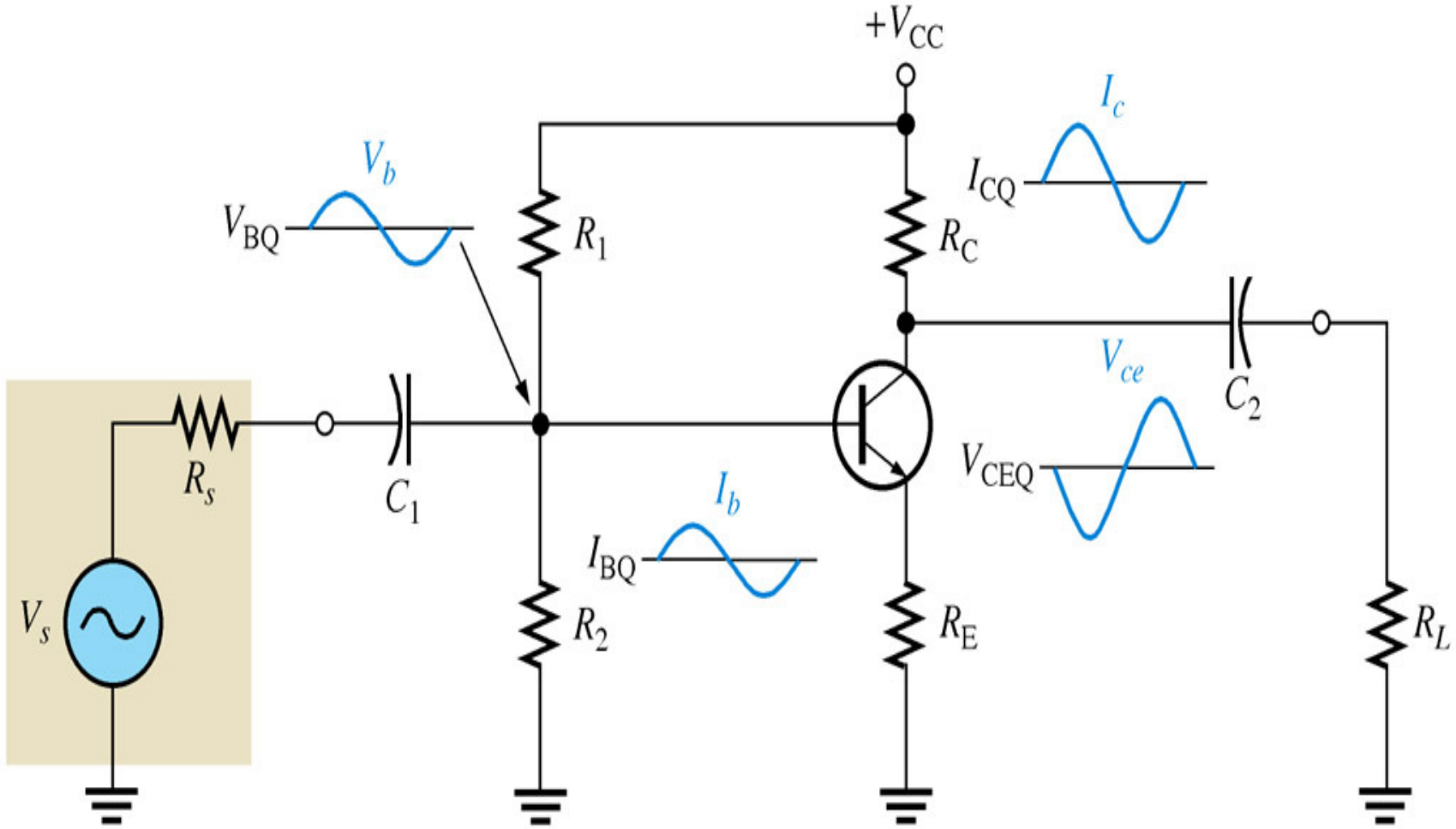
- ***The DC component, V_I***
- ***The small signal component, $v_i(t)$***

The DC component signal is not a function of time (as a constant e.g. V_I=12V)

The small-signal component $v_i(t)$ is a function of time. This signal is an AC signal

This signal $v_i(t)$ is referred as the small-signal component because its magnitude is generally small for all time *t*

DC and Small-Signal Components



DC and Small-Signal Components

- The purpose of DC analysis is to establish a Q-point (quiescent point) or DC operating point. The goal is to set the Q-point such that it does not go into saturation or cutoff when an ac signal is applied

- If the Q-point is in active region, the transistor can operate as an amplifier.

- The purpose of AC analysis is to obtain the gain (ratio of output voltage and input voltage)

To obtain

Current and Voltage Gain, A_i and V_i

Input Impedance, Z_i

Output Impedance, Z_o

by adopting simple circuit model or transistor equivalent model.

AC Analysis for BJT Circuit

- AC analysis;
  - Short all capacitors
  - Open circuit all DC Supplies and ground them

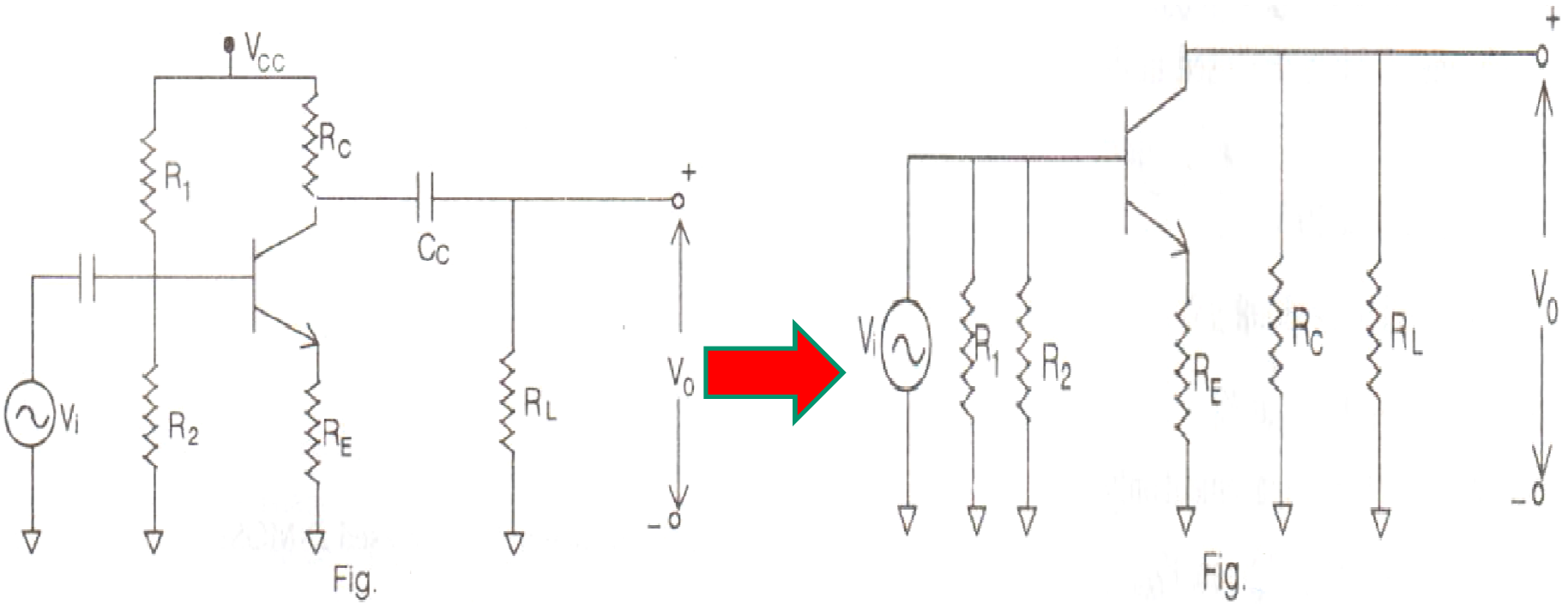
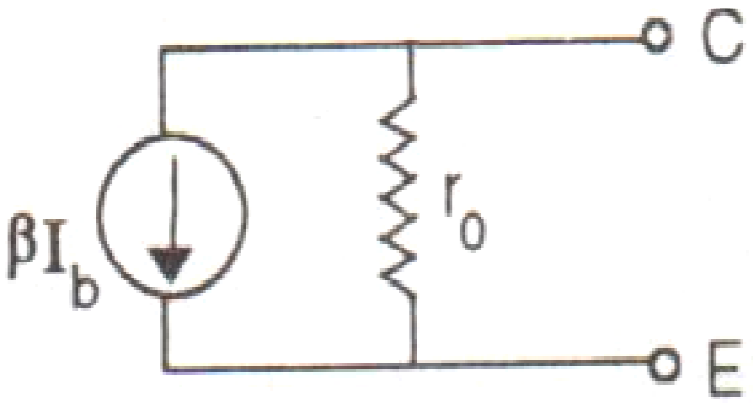


Fig.

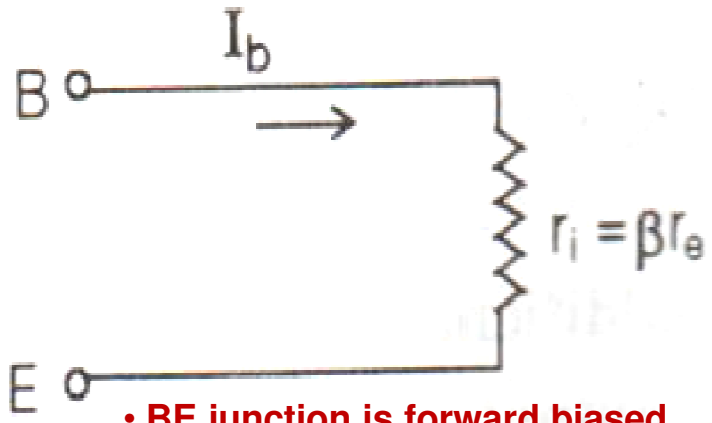
Fig.

Transistor r_e model

- High dynamic output resistance
- Transistor can replaced by a current source

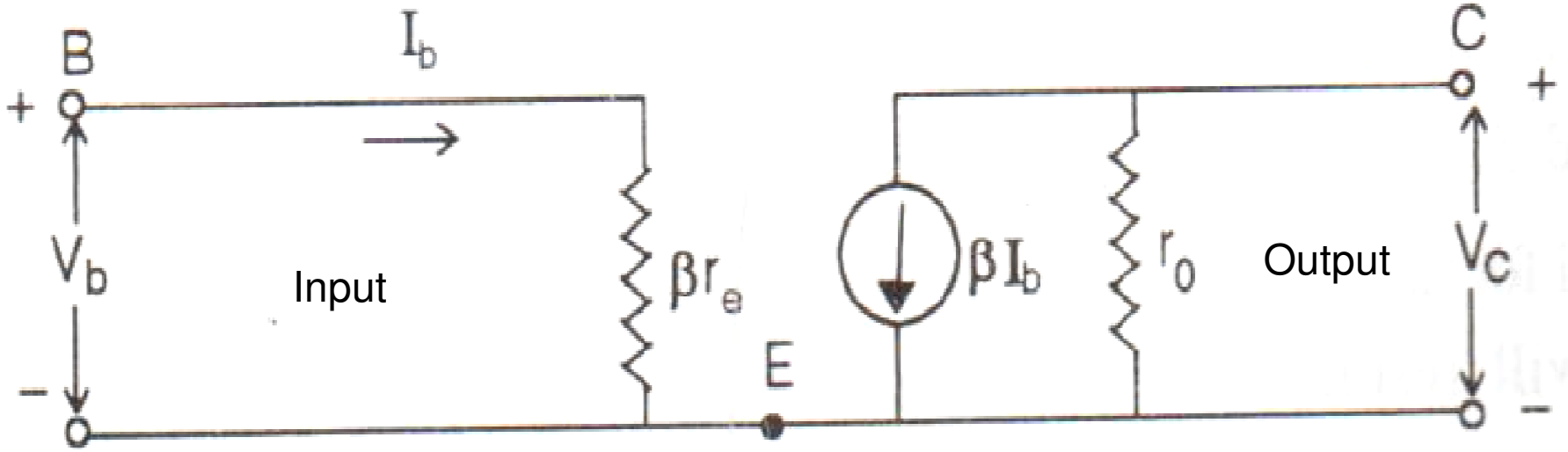


Equivalent circuit between C&E



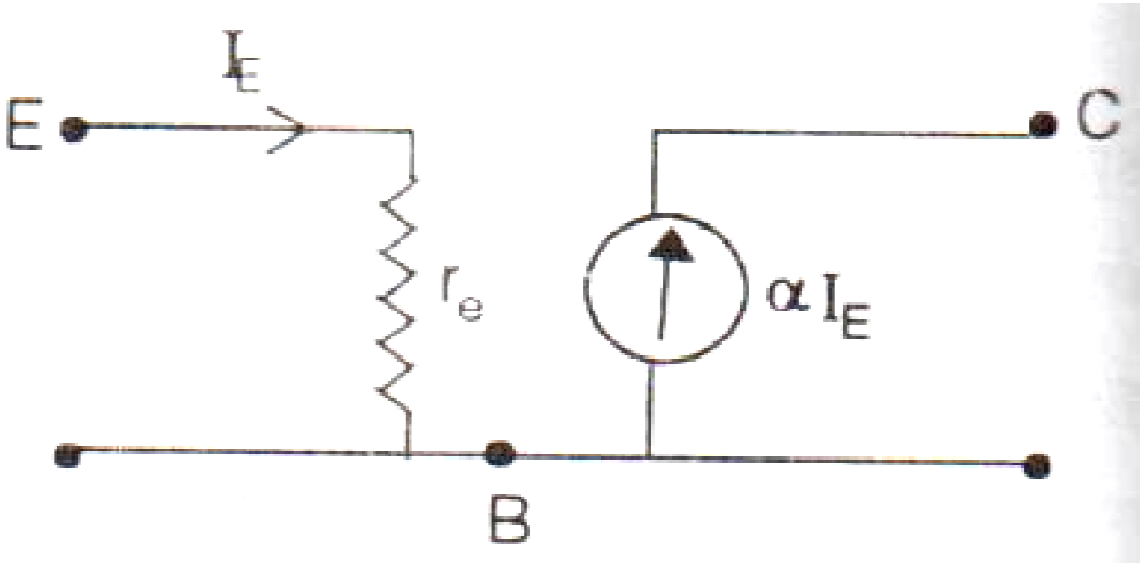
- BE junction is forward biased
- Junction is replaced by r_i

Equivalent circuit between Base&E



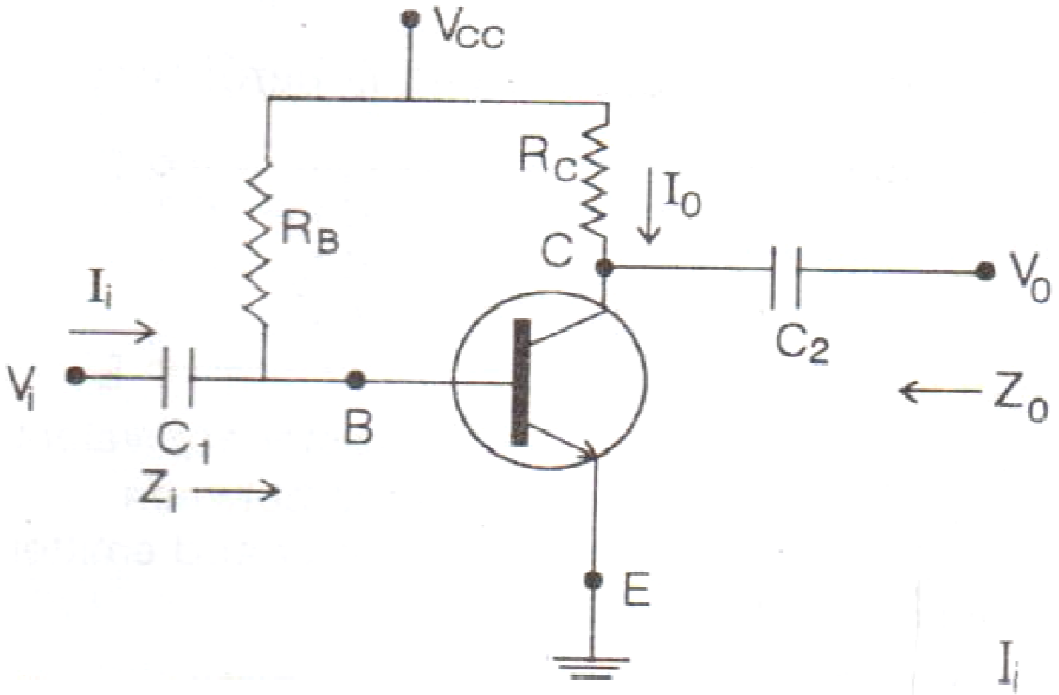
R_e Model for Common Emitter (CE) Transistor Configuration

R_e Model for Common Base (CB) Configuration



R_e Model for Common Base (CB)Transistor Configuration

Common Emitter Fixed-Bias Configuration

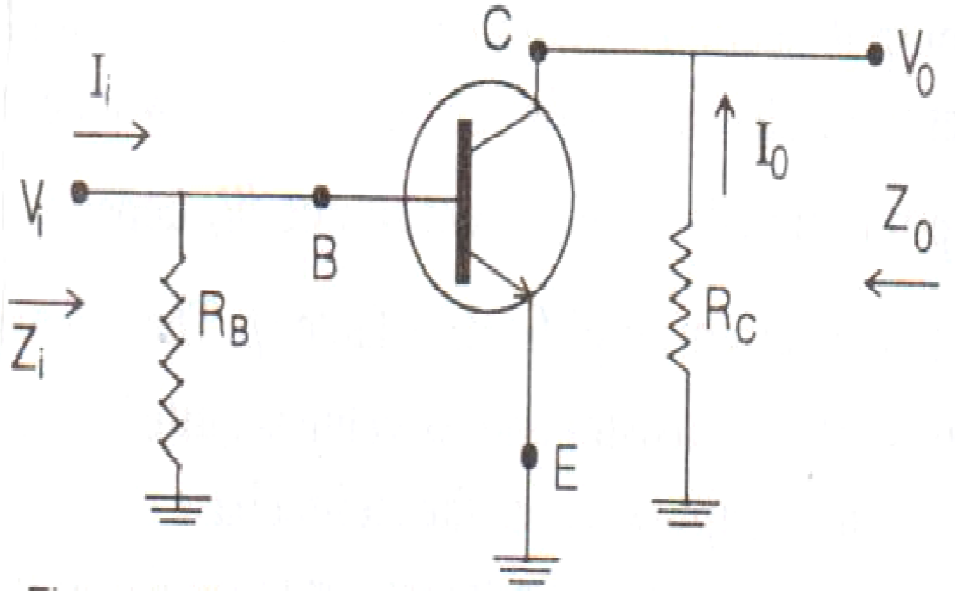


Fixed Bias Configuration

•The input (Vi) is applied to the base and the output (Vo) is from the collector.

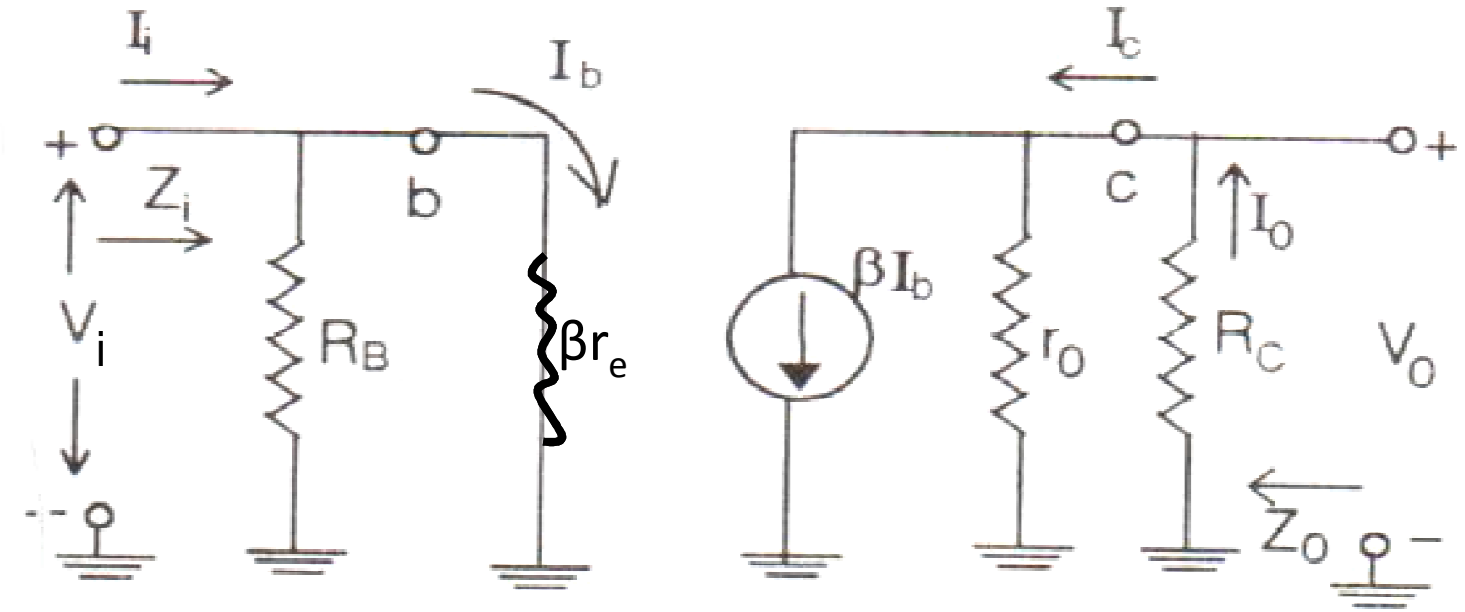
•The Common-Emitter is characterized as **having high input impedance** and **low output impedance** with a **high voltage and current gain.**

Removing DC effects of V_{CC} and Capacitors



Removal of effect V_{cc}, C_1 and C_2

Impedance Calculations



Redrawn Network for CE Configuration

Input Impedance (Zi):-

Z_i :

$$Z_i = R_B \| \beta r_e \quad \text{ohms} \qquad (1)$$

Determine β, r_e, and r_o:

β and r_o: look in the specification sheet for the transistor or test the transistor using a curve tracer.

r_e: calculate r_e using dc analysis:

$$r_e = \frac{26\text{mV}}{I_E}$$

$$Z_i \cong \beta r_e \quad \text{ohms} \qquad (2)$$

$$R_B \geqslant 10\, Br_e$$

Output Impedance (Zo)

The output impedance Zo determined V_i=0, for Fig. when V_i=0, I_i=I_b=0, resulting in an open circuit equivalence for the current source. The result for the Fig shown configuration :

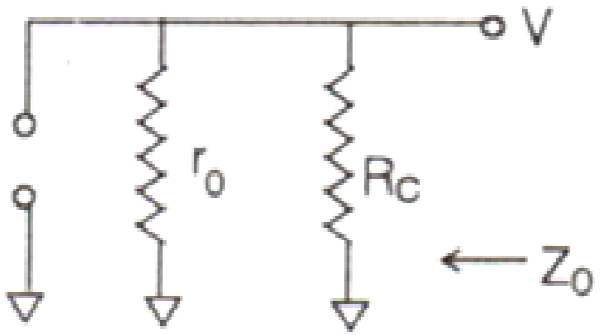


Fig.

$$\boxed{Z_o = R_C \| r_o} \text{ ohms} \qquad (3)$$

If $r_o \geq 10\,R_C$ the approximation $R_C \| r_o \cong R_C$ is frequently applied and

$$\boxed{Z_o \cong R_C} \quad r_o \geq 10R_C \qquad (4)$$

Voltage Gain (Av)

A_v : The resistors r_o and R_C are in parallel,

and
$$V_o = -\beta I_b (R_C \| r_o) \qquad (5)$$

$$\begin{cases} \because \quad v_0 = -I_o R_C \\ \text{where } I_o \approx I_C \approx BI_b \end{cases}$$

but
$$I_b = \frac{V_i}{\beta_{r_e}} \qquad (6)$$

so that
$$V_o = -\beta \left(\frac{V_i}{\beta_{r_e}} \right) (R_C \| r_o) \qquad (7)$$

From Eq. 5 and 6

and
$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e} \qquad (8)$$

If $r_o \geq 10R_C$
$$A_v = -\frac{R_C}{r_e} \quad r_o \geq 10R_C \qquad (9)$$

Current gain (A_i):-

Apply the current divider rule to input and output of circuit

$$I_o = \frac{(r_o)(\beta I_b)}{r_o + R_C} \tag{10}$$

and

$$\frac{I_0}{I_b} = \frac{r_o \beta}{r_o + R_C} \tag{11}$$

with

$$I_b = \frac{(R_B)(I_i)}{R_\beta + \beta_{r_e}}$$

or

$$\frac{I_b}{I_i} = \frac{R_\beta}{R_\beta + \beta r_e} \tag{12}$$

The result is

$$A_i = \frac{I_o}{I_i} = \left(\frac{I_o}{I_b}\right)\left(\frac{I_b}{I_i}\right) = \left(\frac{r_o \beta}{r_o + R_C}\right)\left(\frac{R_B}{R_B + \beta r_e}\right) \tag{13}$$

and

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}} \tag{14}$$

which is certainly an unwieldy complex expression.

However, if $r_o \geq 10R_C$ and $R_B \geq \beta r_e$, which is often the case,

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R_B r_o}{(r_o)(R_B)} \tag{15}$$

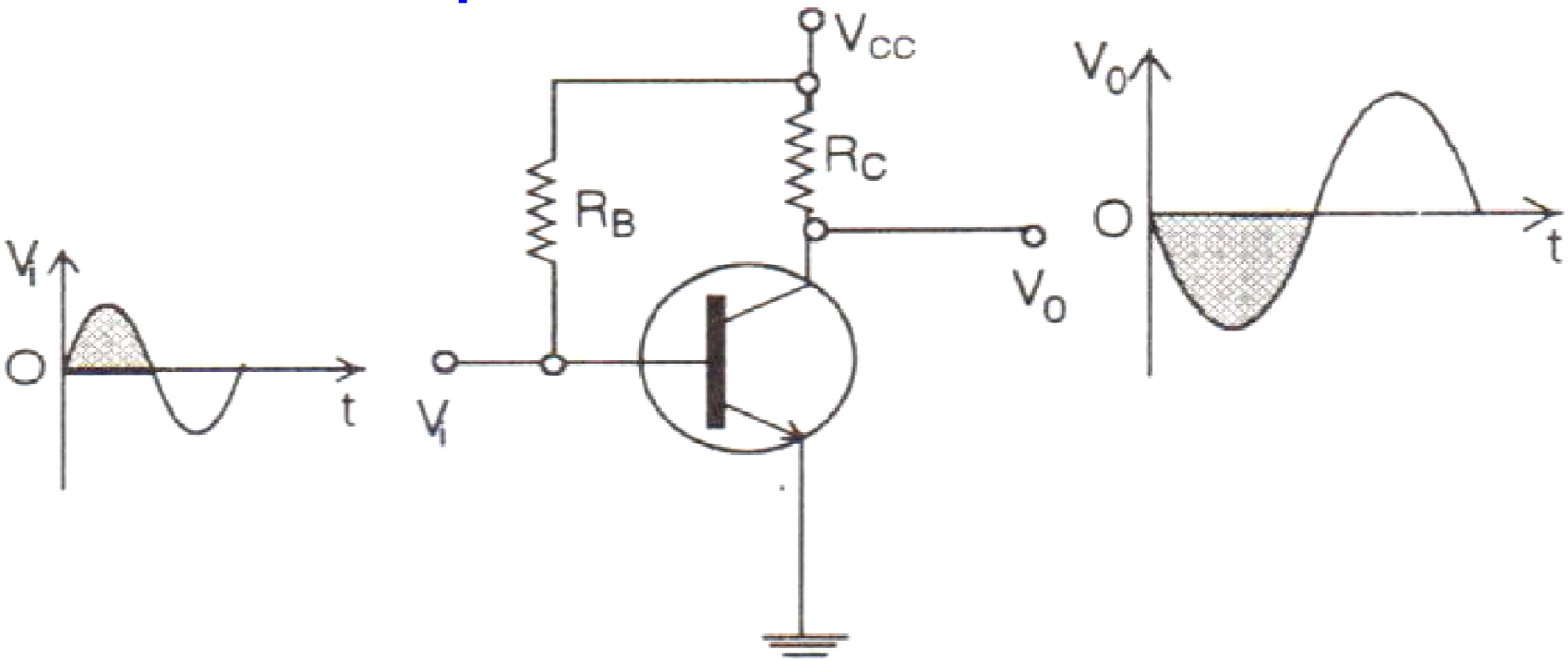
and

$$\boxed{A_i \cong \beta} \quad r_0 \geq 10R_C,\ R_B \geq 10\beta r_e \tag{16}$$

Current Gain from Voltage Gain:

$$A_i = -A_v \frac{Z_i}{R_C}$$

Phase Relationship



The negative sign in Av equation indicate that a 180 degree phase shift occurs between input and output.

The phase relationship between input and output is 180 degrees. The negative sign used in the voltage gain formulas indicates the inversion.