Assignment for Applied Electronics

(Due Date 30/5/2014 at 5 P.M)

(Part A- Digital Electronics)

1) Note difference between CPLD and FPGA.
2) Convert
   a) Decimal to Binary- 77, 96, 0.63
   b) Binary to Decimal – 1010, 001000010
   c) Hex to Binary- 9124,F44H
   d) Decimal to Hex- 99,1100,123

3) Find 2's Complement
   a) 1001010 b) 111001

4) Perform –

   a) 23D9 + 94BE b) 59F - 2B8 c) 11010011 + 01101111

5) Explain and write down Purpose of Using Gray Code, Excess3 Code, ASCII Code.

6. Convert the decimal number 345 to binary in two ways: (a) convert directly to binary; (b) convert first to hexadecimal, then from hexadecimal to binary, Which method is faster?

7) Suppose 8 bit word in memory is 11000010. Using hamming algorithm what check bits would be stored in memory.

8) Implement x'y'z + x'yz + xy' using OR, AND & NOT Gate.

9) Make AND & OR Gates using Diodes.

10) What are essential and non essential prime implicant in k map. Explain with examples

11) Simplify using k map

F= x'y'z + xy'z + xyz' + xyz

12) Implement using 8:1 MUX and 4:1 MUX

F= x'y'z + xy'z+xyz'+xyz

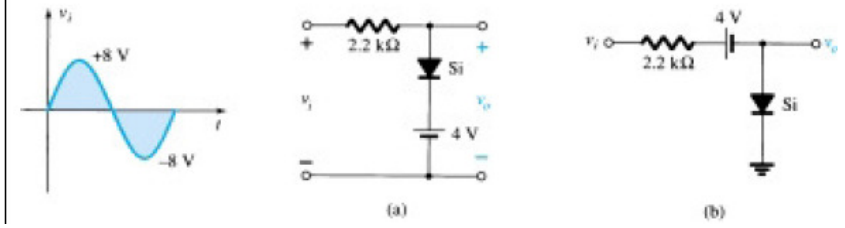
13) What is racing in sequential circuits and how it can be avoided.

14) Convert JK Flip Flop into D and T Flip flop.

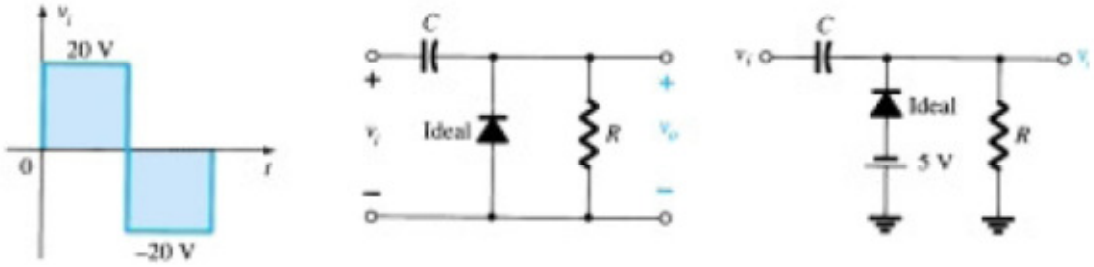
(Part B- Analog Electronics)

1) Explain in detail the working of full wave rectifier and derive the expression for maximum rectifying efficiency.

2) Determine *Vo* for each network of as given below with the input shown



3) Determine *Vo* for each network of as given below with the input shown



4) Explain in detail (with circuit diagram) BJT circuit configurations and compare them.

5) In the circuit shown below in Fig., R1=12KΩ, R2 = 5KΩ, R3 = 8KΩ, RF = 12KΩ. The inputs are: V1 = 9V, V2 = -3V and V3 = -1V. Compute the output voltage

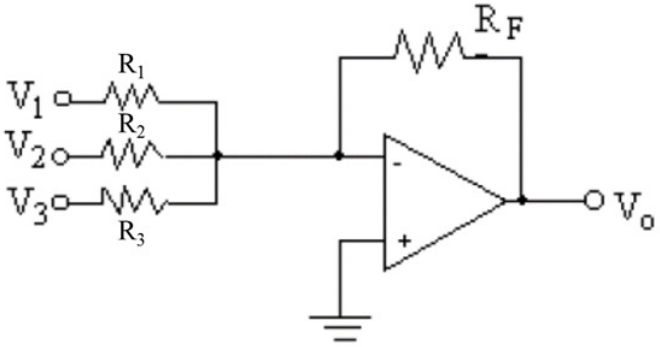


Fig.

6) What is a load line and how is it used in the calculation of current and voltage gains for a single stage amplifier?

7) Explain how an opamp can be used as

a) Integrator b) Differentiator

8) Calculate the dc bias, voltage gain, input impedance, output impedance and resulting output voltage for the cascade amplifier shown in Fig. Calculate the load voltage if a 10 kΩ load is connected across the output. Given V_{GSQ}=-1.9V, I_{DQ} =2.8mA.

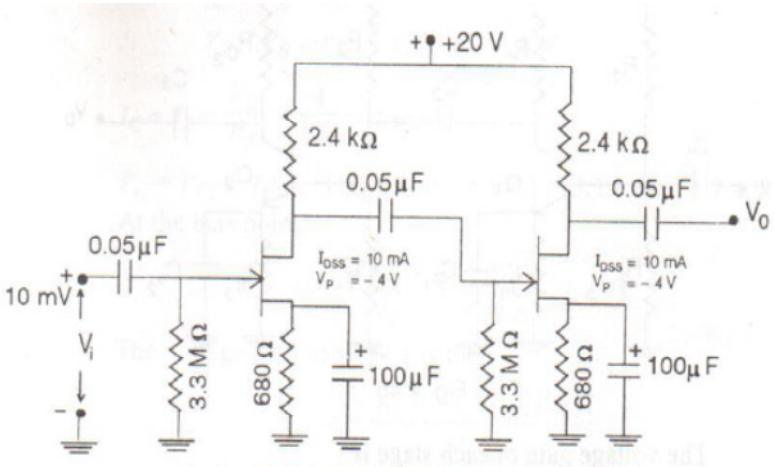
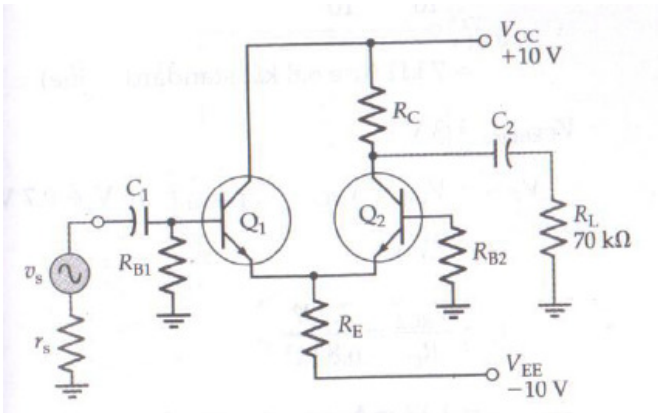


Fig.

9) Determine the suitable resistor values for the differential amplifier circuit in Fig.. The transistor parameters are h_{fe}=60 and h_{ie}=1.4kΩ.



10.) Calculate the closed-loop gain for the negative feedback amplifier shown in Fig. Also calculate the closed loop gain when the open loop gain is changed by ± 50%. Note that Av = 100 000 and B= 1/100.