Sequential Circuits (Circuits as Memory)

Sequential Circuits

•Most digital systems like digital watches, digital phones, digital computers, digital traffic light controllers and so on require memory elements

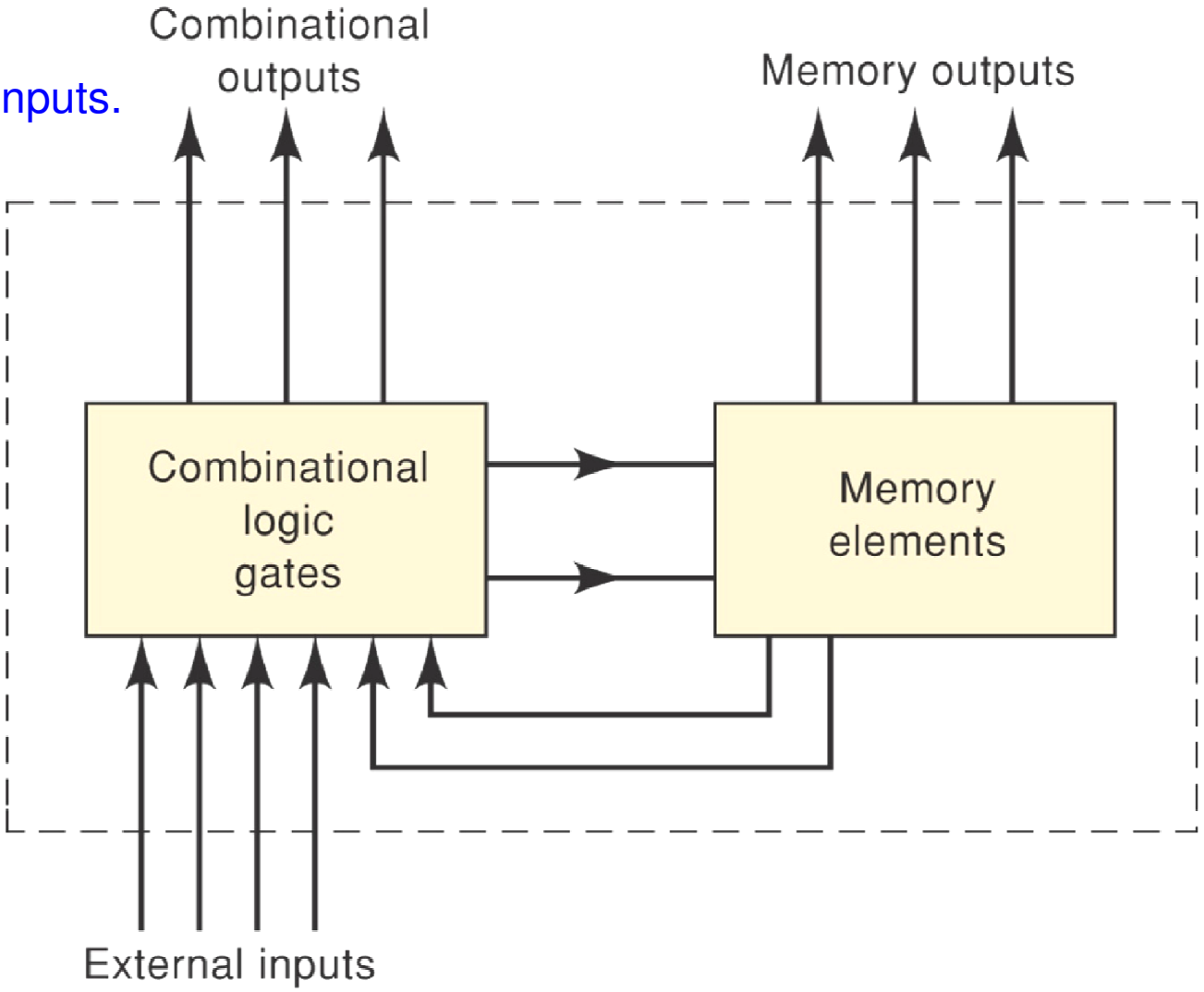
• Memory elements are digital circuits that can store and retrieve data in the form of 1's and 0's.

• The output of the systems with memory depends not only on present inputs but also on what has happened in the past.

•SR latch is an example of memory circuits that can store one bit of information

General Digital System

Outputs depend on:
current inputs, previous inputs.



Cont……Sequential circuit

•**These circuits form a sequential circuit, because the output of the circuit is also used as input to the circuit.**

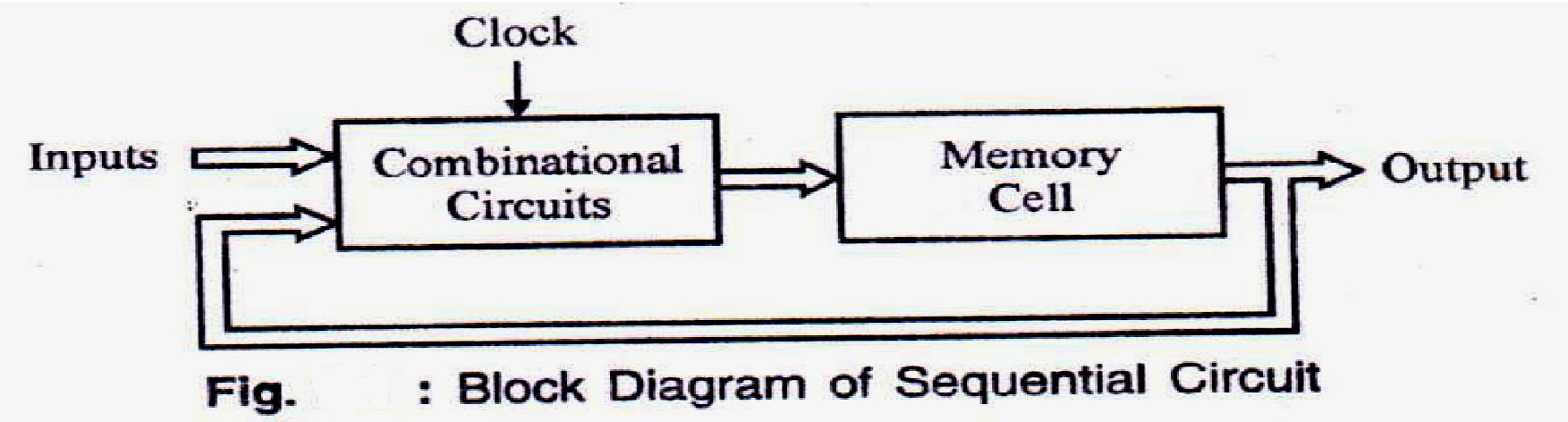


Fig. : Block Diagram of Sequential Circuit

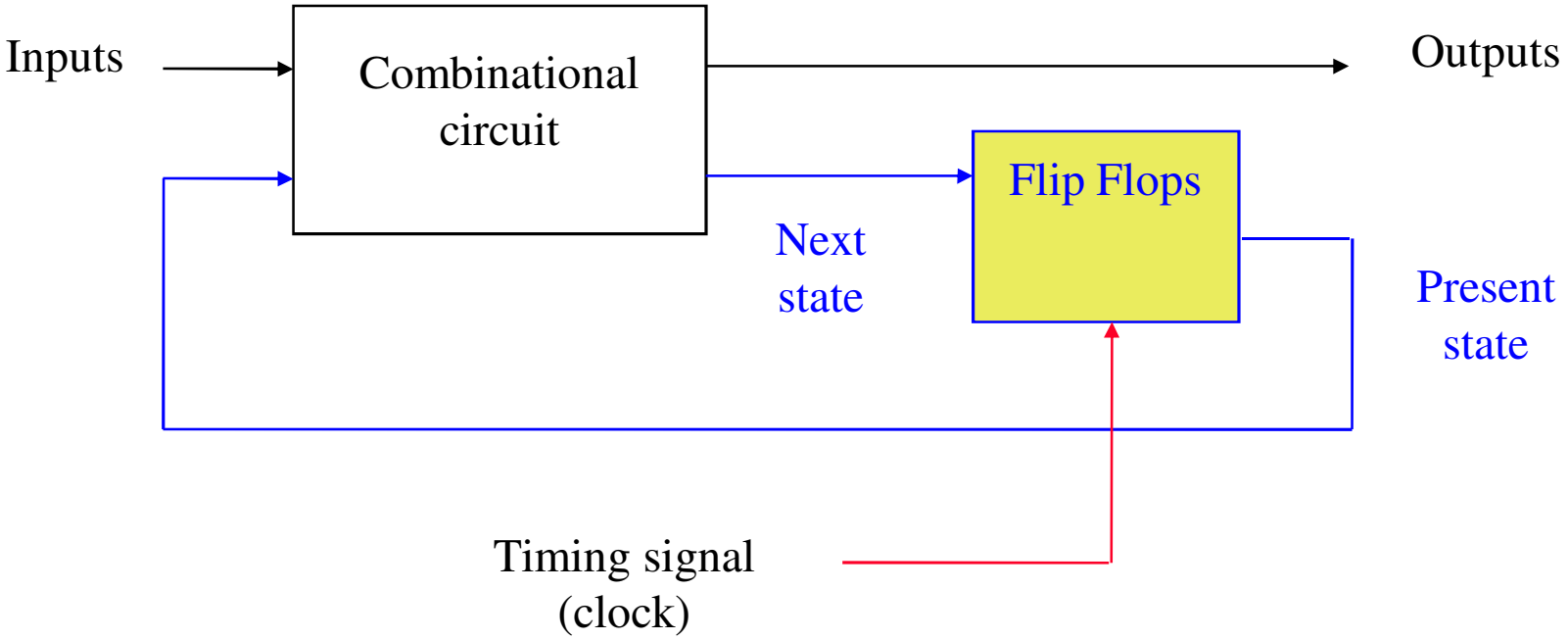
Sequential circuit

The output is a function of the input values and the existing state of the circuit.

We describe the circuit operations using

- Boolean expressions
- Logic diagrams
- Truth tables

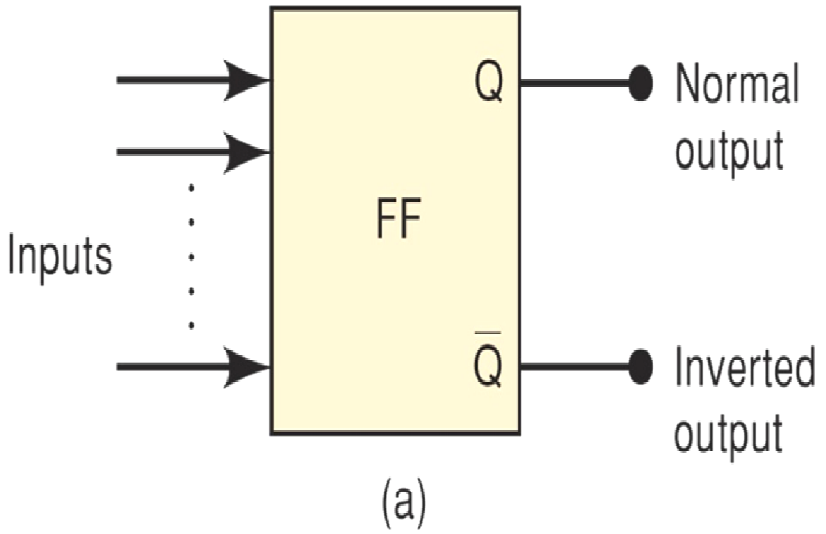
Sequential Circuits



Clock
a periodic external event (input)

synchronizes when current state changes happen
keeps system well-behaved
makes it easier to design and build large systems

General flip-flop symbol and definition of its two possible output states



(a)

Output states	
$Q = 1, \overline{Q} = 0$:	called HIGH or 1 state; also called SET state
$Q = 0, \overline{Q} = 1$:	called LOW or 0 state; also called CLEAR or RESET state

(b)

NAND Gate Latch

- The NAND gate latch or simply latch is a basic FF.
- The inputs are set and clear (reset)
- The inputs are active low, that is, the output will change when the input is pulsed low.
- When the latch is set

$$Q = 1 \text{ and } \overline{Q} = 0$$

- When the latch is clear or reset

$$Q = 0 \text{ and } \overline{Q} = 1$$

A NAND latch is an example of a bistable device

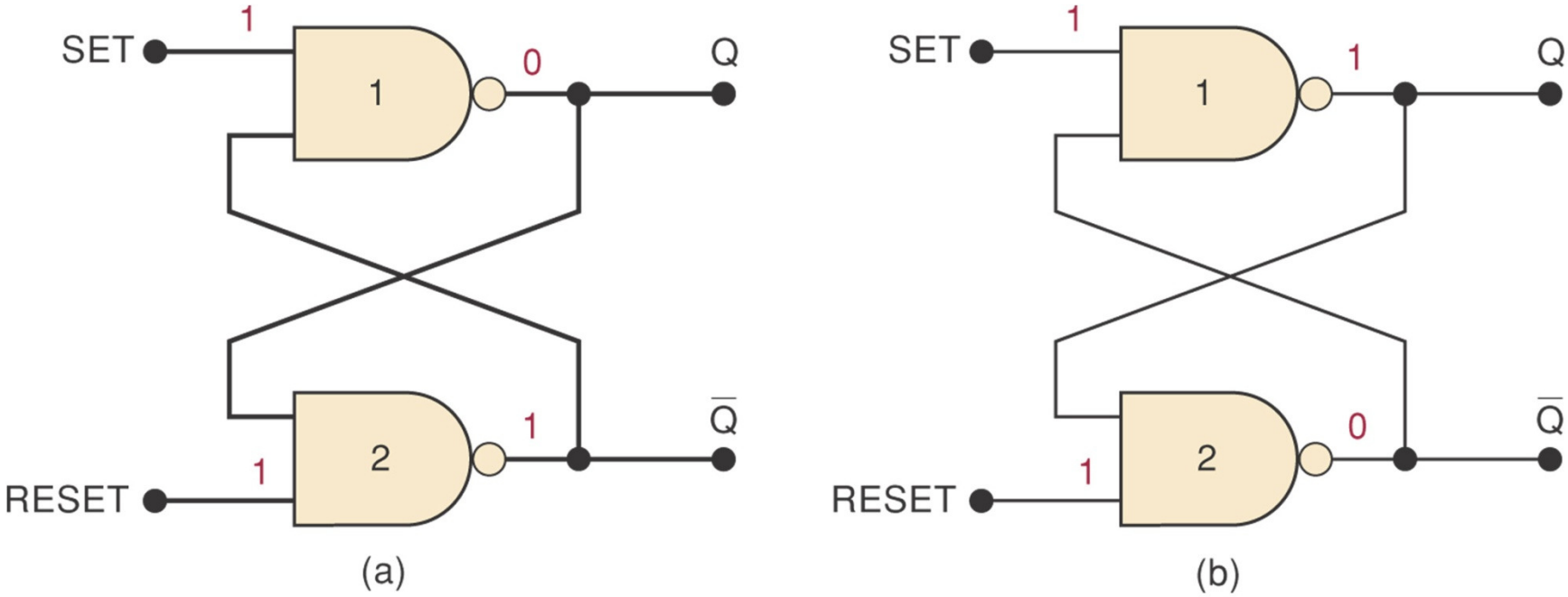
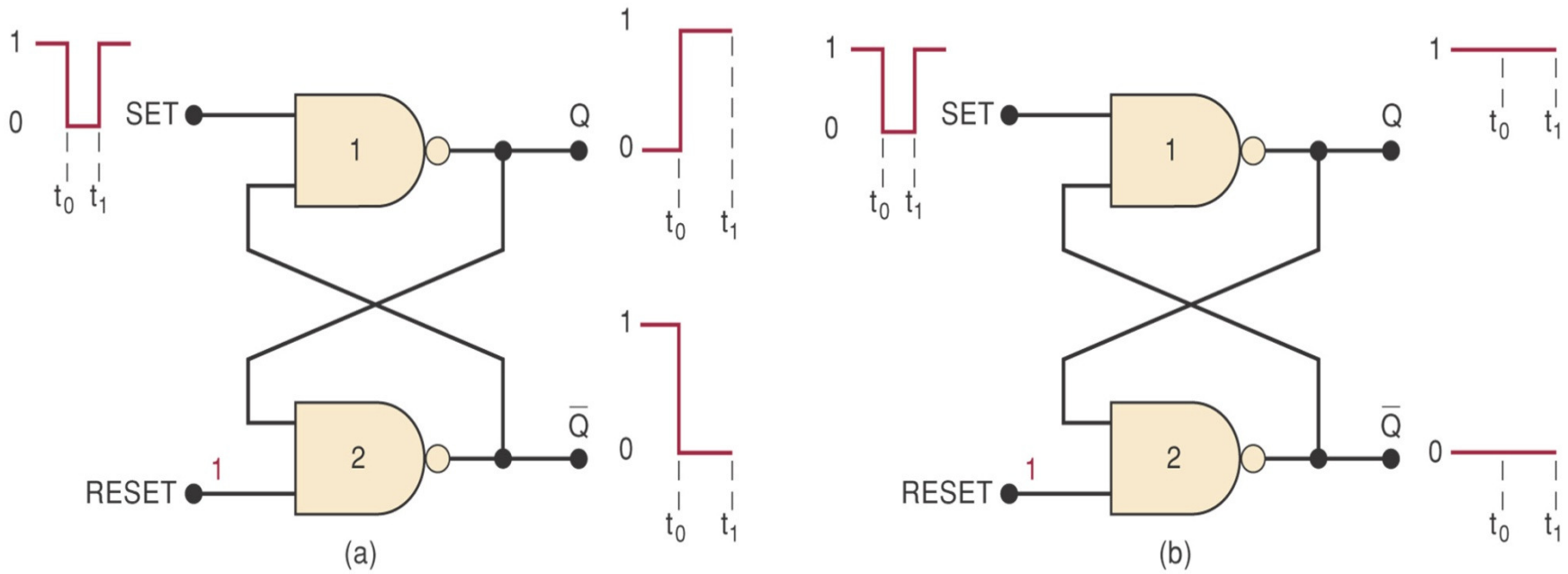


Figure A NAND latch has two possible resting states when SET = RESET = 1.

NAND		
0	0	1
0	1	1
1	0	1
1	1	0

Setting the NAND Flip-Flop



NAND		
0	0	1
0	1	1
1	0	1
1	1	0

Figure Pulsing the SET input to the 0 state when (a) *Q* = 0 prior to SET pulse; (b) *Q* = 1 prior to SET pulse. Note that, in both cases, *Q* ends up HIGH.

Resetting the NAND Flip-Flop

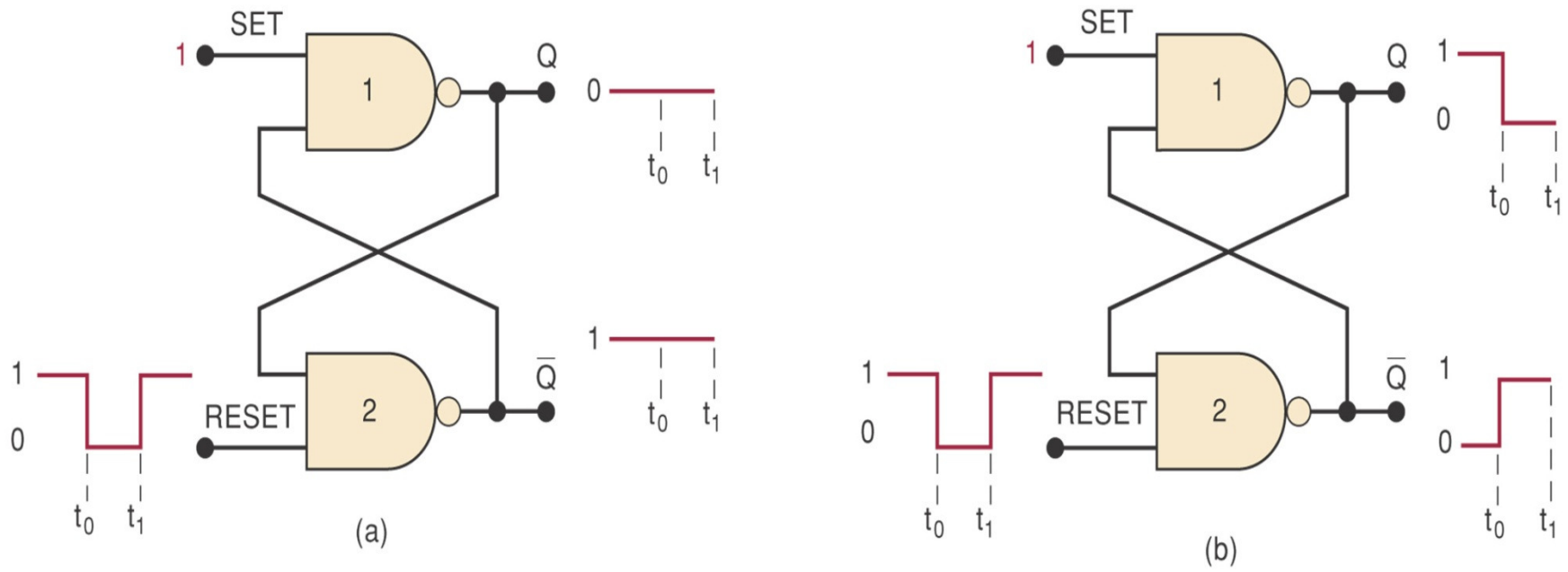
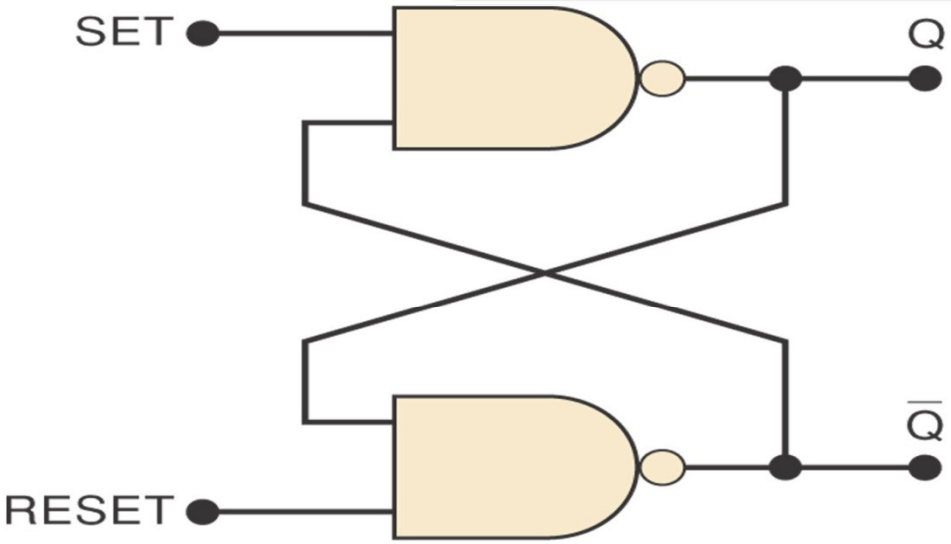


Figure Pulsing the RESET input to the LOW state when (a) *Q* = 0 prior to RESET pulse; (b) *Q* = 1 prior to RESET pulse. In each case, *Q* ends up LOW.

Function table of a NAND latch

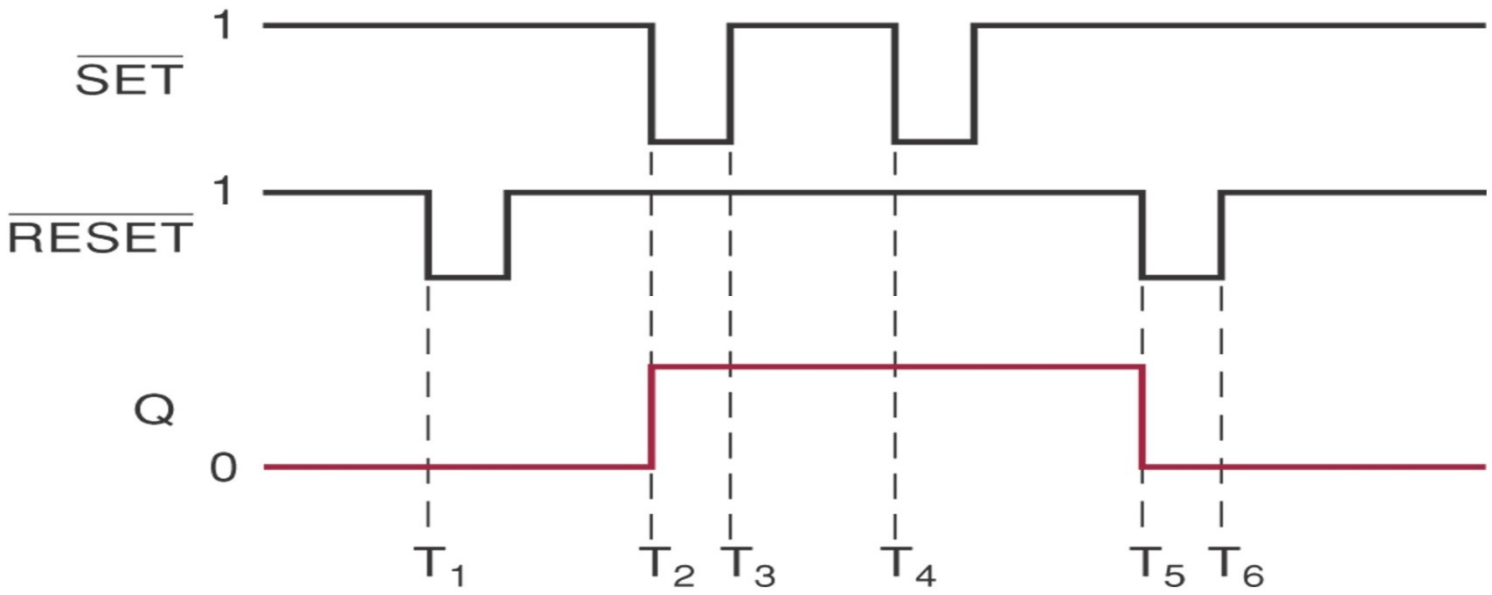


(a)

Set	Reset	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid*

*Produces $Q = \overline{Q} = 1$.

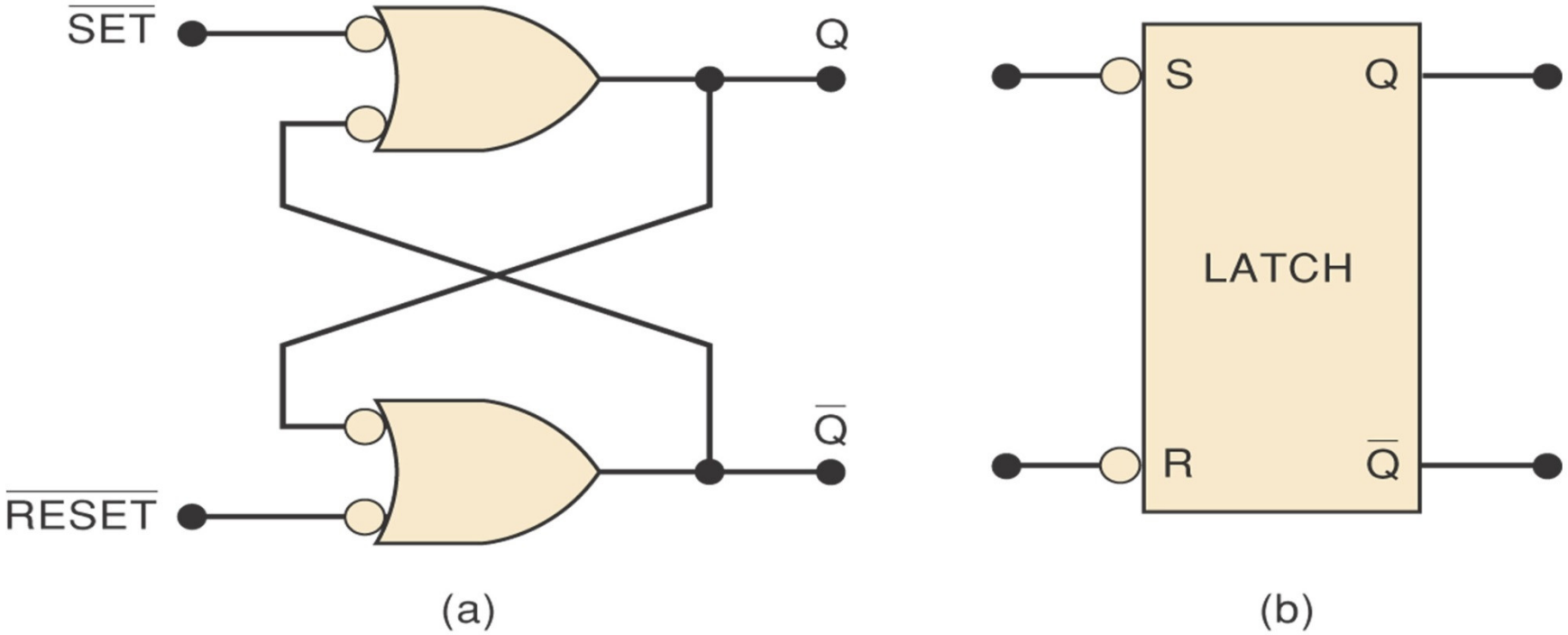
(b)



NAND Gate Latch Summary

- **Summary of the NAND latch:**
- **SET = RESET = 1. Normal resting state, outputs remain in state prior to input.**
- **SET = 0, RESET = 1. Q will go high and remain high even if the SET input goes high.**
- **SET = 1, RESET = 0. Q will go low and remain low even if the RESET input goes high.**
- **SET = RESET = 0. Output is unpredictable because the latch is being set and reset at the same time.**

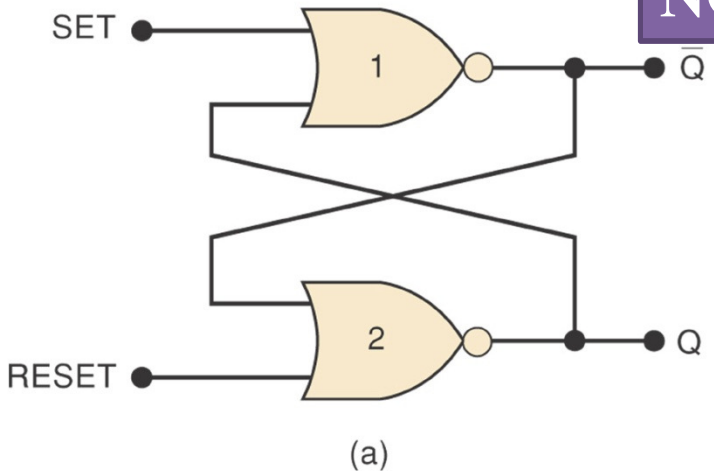
Other Representations of a NAND latch



NOR Gate Latch

- The NOR latch is similar to the NAND latch except that the outputs are reversed.
- The SET and RESET inputs are active high, that is, the output will change when the input is pulsed high.
- In order to ensure that a FF begins operation at a known level, a pulse may be applied to the SET or RESET inputs when a device is powered up.

NOR gate latch

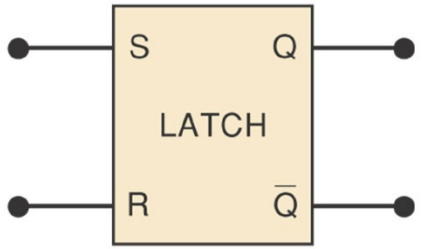


(a)

Set	Reset	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid*

*Produces Q = $\overline{Q}$ = 0.

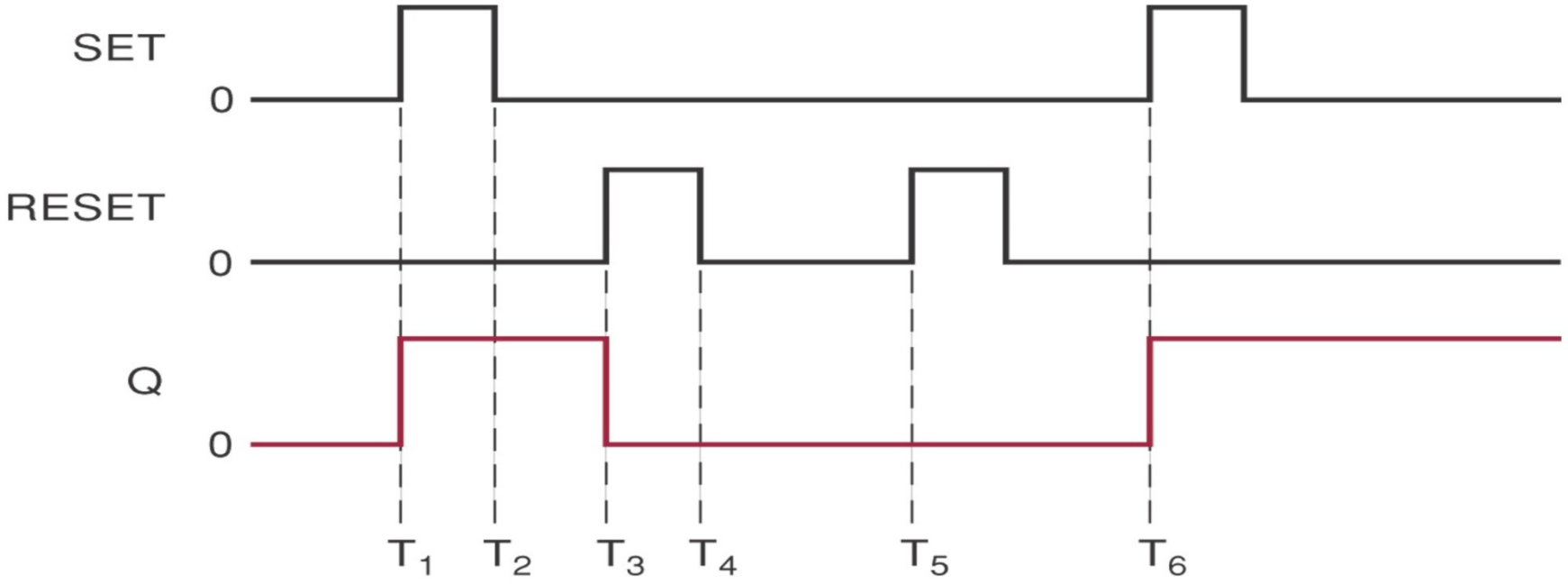
(b)



(c)

Figure (a) NOR gate latch; (b) function table; (c) simplified block symbol.

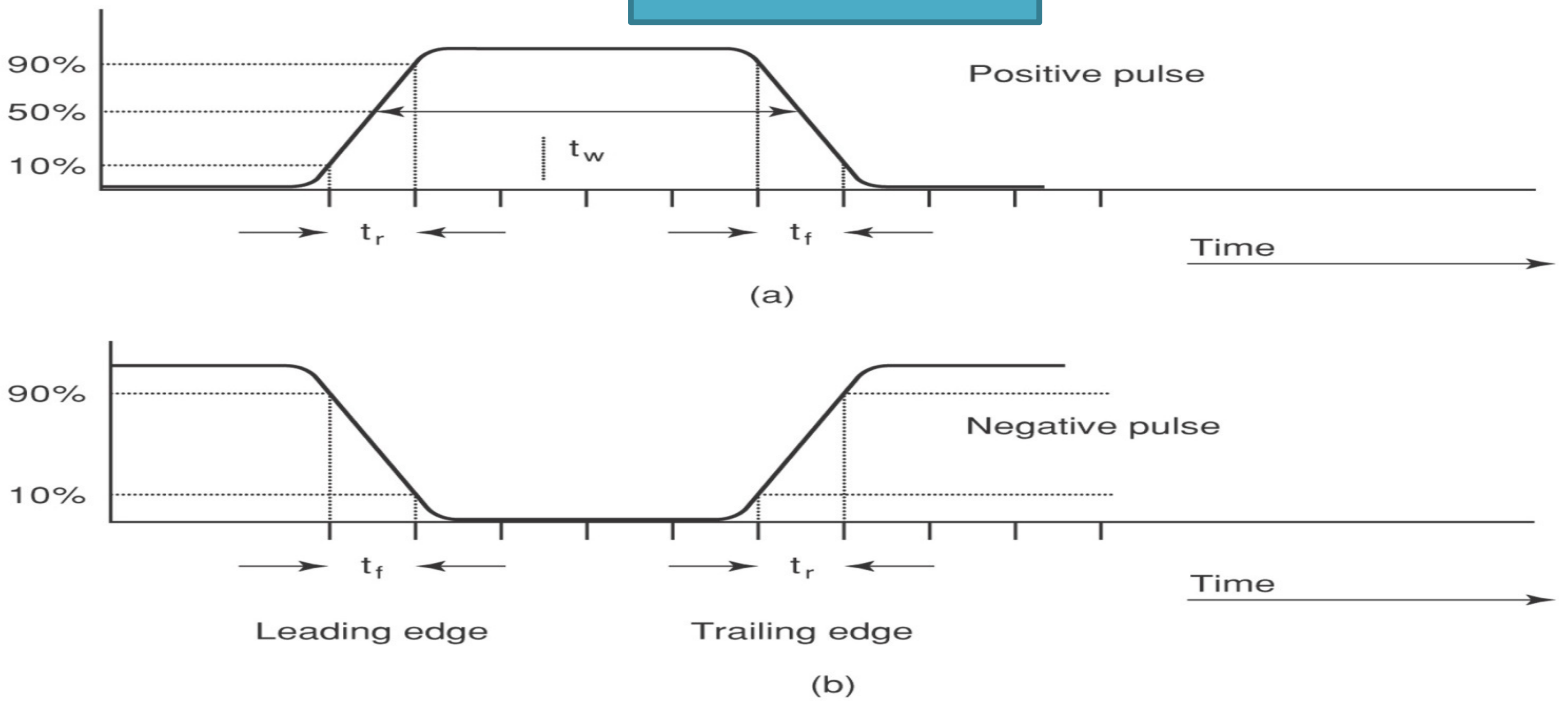
Determine Q for a NOR latch given the inputs below



Digital Pulses

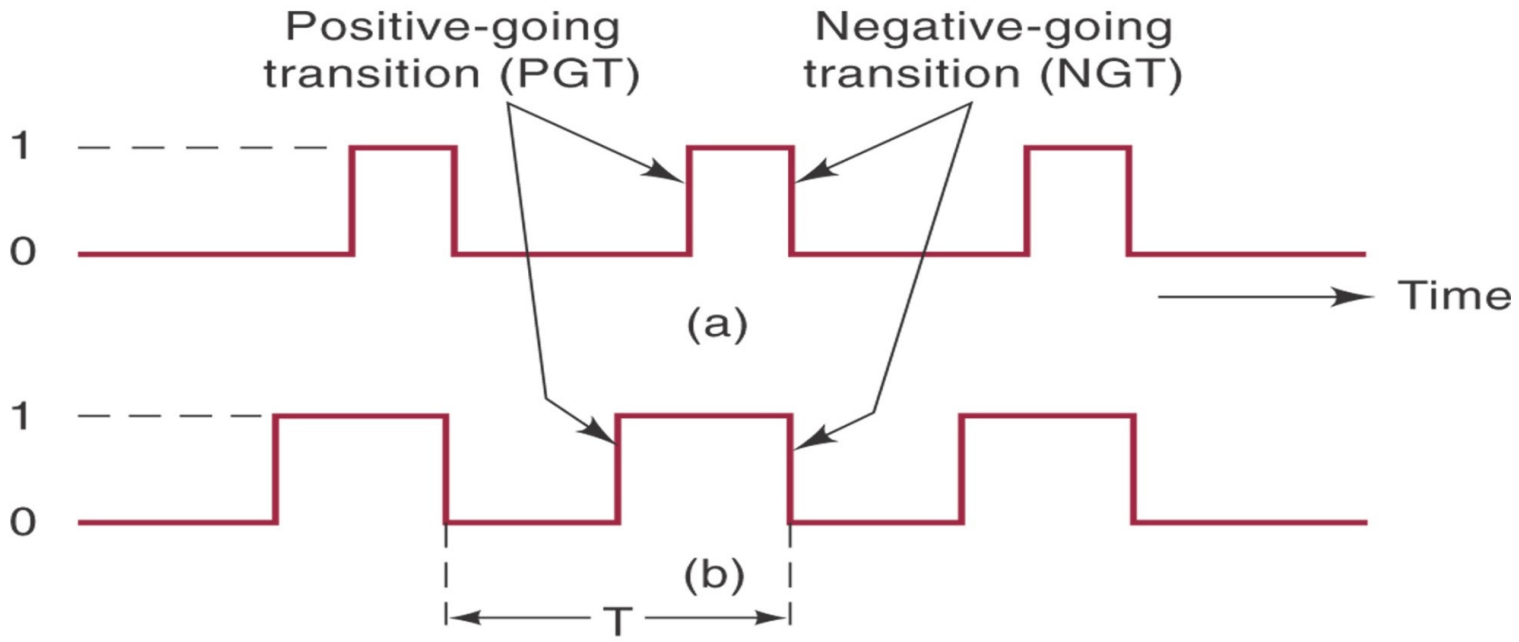
- The transition from low to high on a positive pulse is called rise time (t_r).
  - Rise time is measured between the 10% and 90% points on the leading edge of the voltage waveform.
- The transition from high to low on a positive pulse is called fall time (t_f).
  - Fall time is measured between the 90% and 10% points on the trailing edge of the voltage waveform.

Rise and Fall times



Clock Signals and Clocked Flip-Flops

- Asynchronous system – outputs can change state at any time the input(s) change.
- Synchronous system – output can change state only at a specific time in the clock cycle.
  - The clock signal is a rectangular pulse train or square wave.
  - Positive going transition (PGT) – when clock pulse goes from 0 to 1.
  - Negative going transition (NGT) – when clock pulse goes from 1 to 0.
  - Transitions are also called edges.

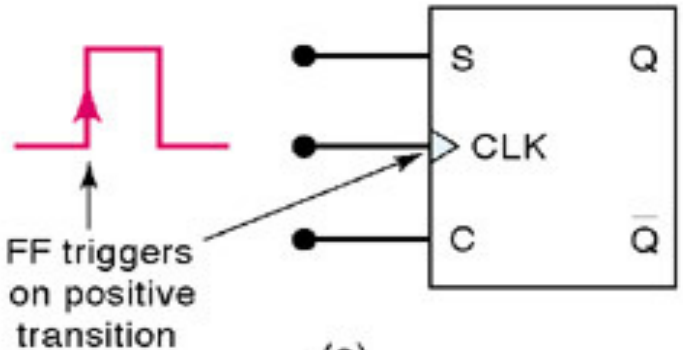


Clock Signals and Clocked Flip-Flops

- **Clocked FFs change state on one or the other clock transitions.**
- Some common characteristics:
  - Clock inputs are labeled CLK, CK, or CP.
  - A small triangle at the CLK input indicates that the input is activated with a PGT.
  - A bubble and a triangle indicates that the CLK input is activated with a NGT.
  - Control inputs have an effect on the output only at the active clock transition (NGT or PGT). These are also called synchronous control inputs.
  - The control inputs get the FF outputs ready to change, but the change is not triggered until the CLK edge.

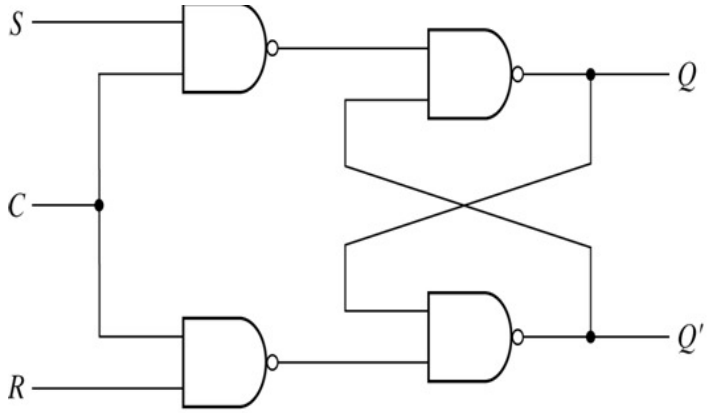
Clocked S-R Flip-Flop

- **The SET-RESET (or SET-CLEAR) FF will change states at the positive going or negative going clock edge.**



Inputs			Output
S	C	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.



(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; set state
1	1	1	Indeterminate

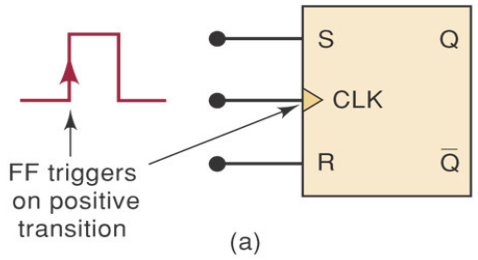
(b) Function table

Fig. SR Latch with Control Input

- **Occasionally, desirable to avoid latch changes**
- **C = 0 disables all latch state changes**
- **Control signal enables data change when C = 1**
- **Right side of circuit same as ordinary S-R latch.**

Clocked SR Flip-Flop

Figure (a) Clocked S-R flip-flop that responds only to the positive-going edge of a clock pulse; (b) function table; (c) typical waveforms.

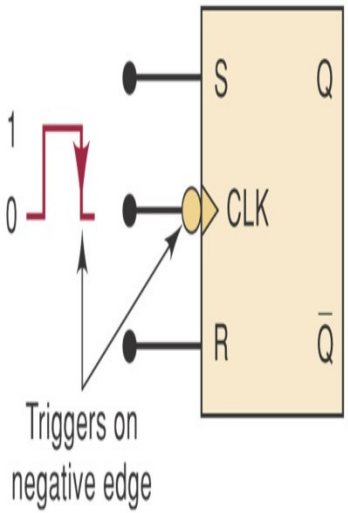


(a)

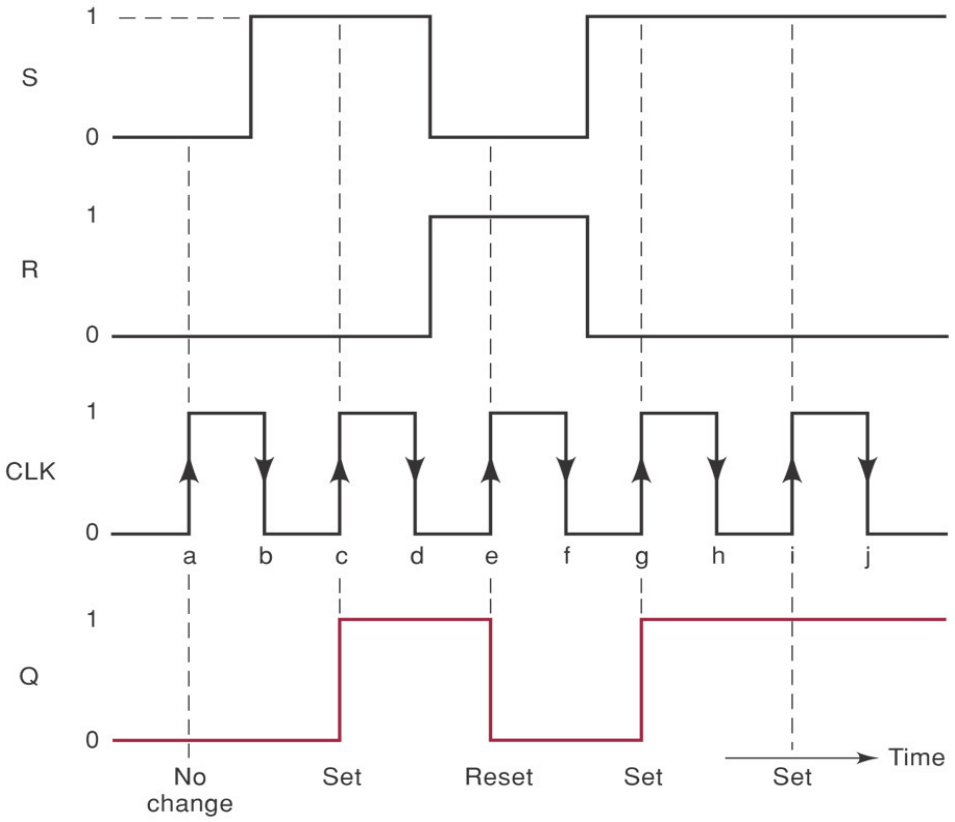
Inputs			Output
S	R	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

(b)



Inputs			Output
S	R	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	Ambiguous



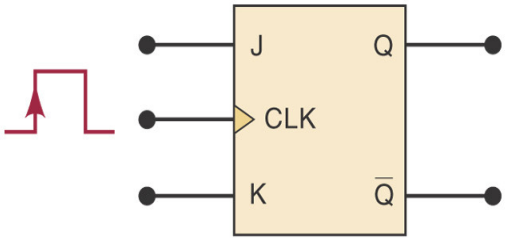
(c)

Figure Clocked S-R flip-flop that triggers only on negative-going transitions.

Clocked J-K Flip-Flop

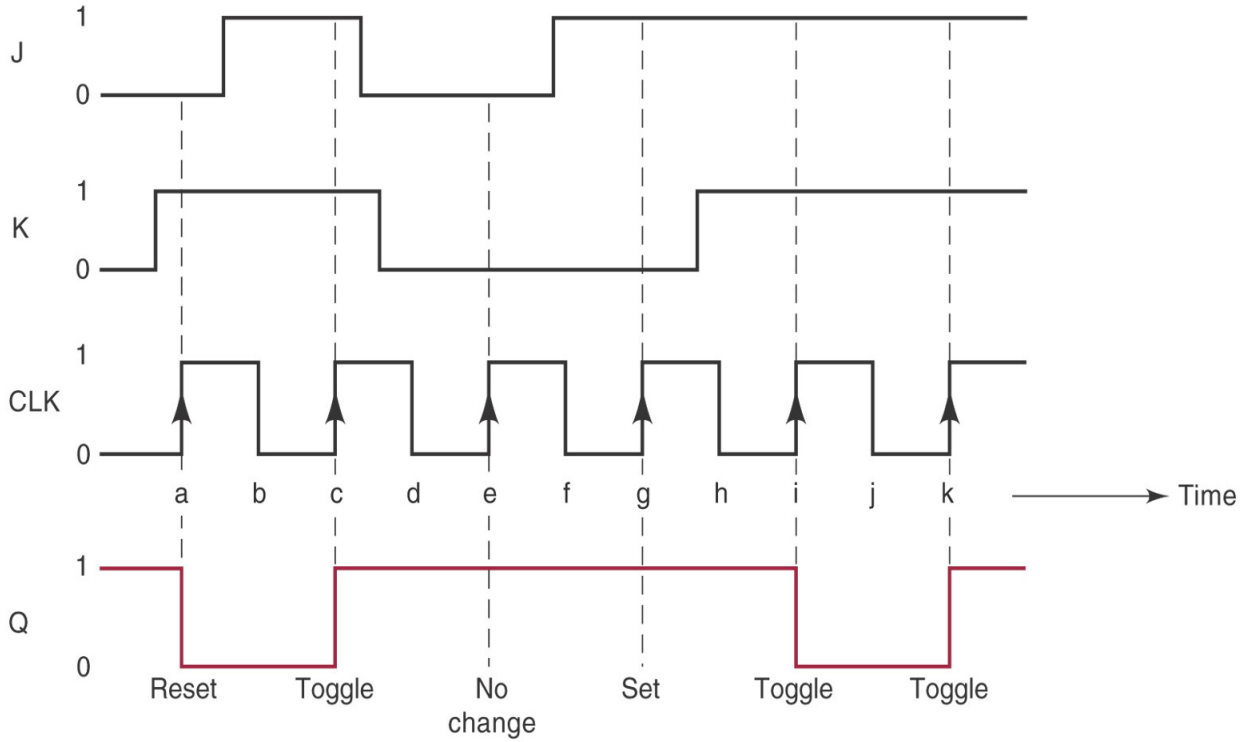
- Operates like the S-R FF. J is set, K is clear.
- When J and K are both high the output is toggled from whatever state it is in to the opposite state.
- May be positive going or negative going clock trigger.
- Has the ability to do everything the S-R FF does, plus operate in toggle mode.

Clocked JK Flip-Flop



J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

(a)



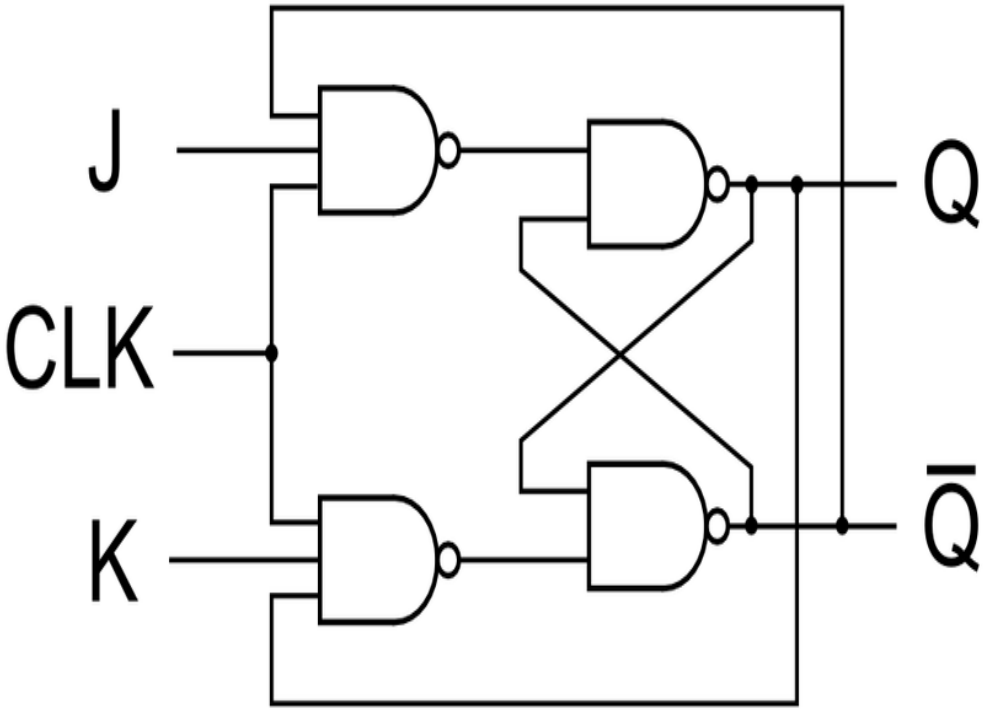
(b)

Figure (a) Clocked J-K flip-flop that responds only to the positive edge of the clock; (b) waveforms.

J-K Flip-flop

The 4 modes of operation are:
hold, set, reset, toggle

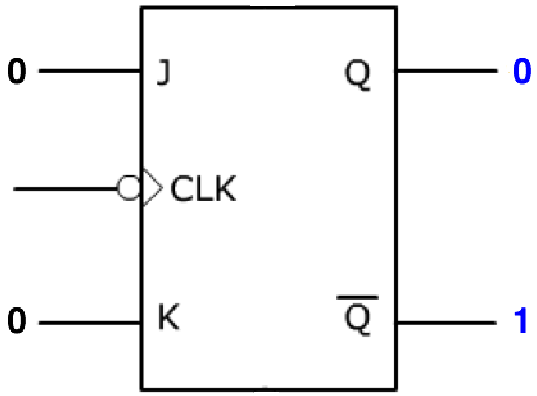
J	K	Q	Q’	Mode
0	0	Q	Q’	Hold
1	0	1	0	Sets
0	1	0	1	Resets
1	1	Q’	Q	Toggle

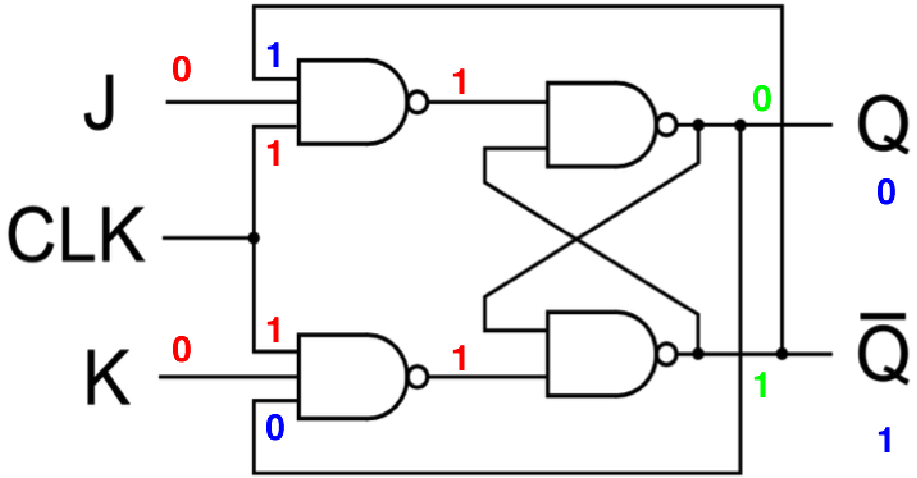


JK contains an internal
Active Low SR latch.

Mode of Operation: Hold

Hold: no change in Q.

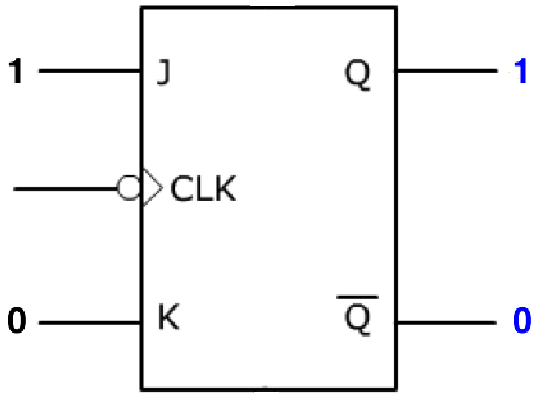


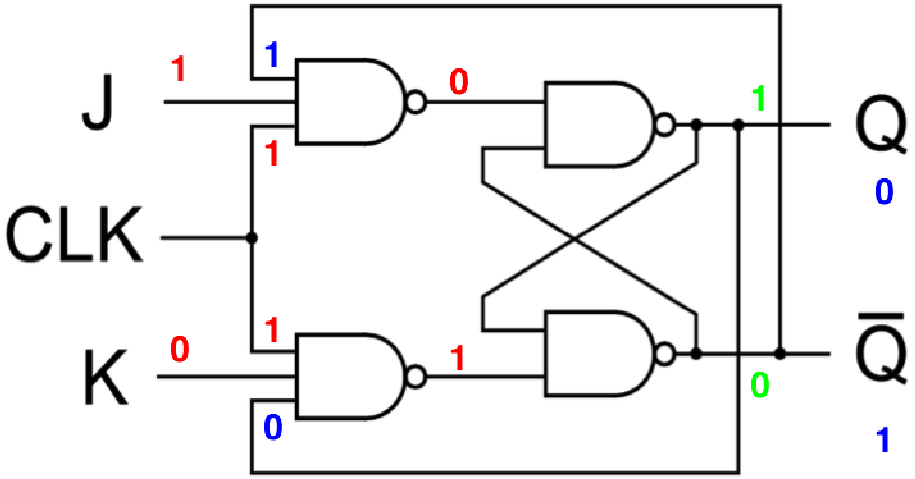


J	K	Q	Q'	Orig. Q	Orig. Q'
0	0	0	1	0	1

Mode of Operation: Set

Set: Q = 1.

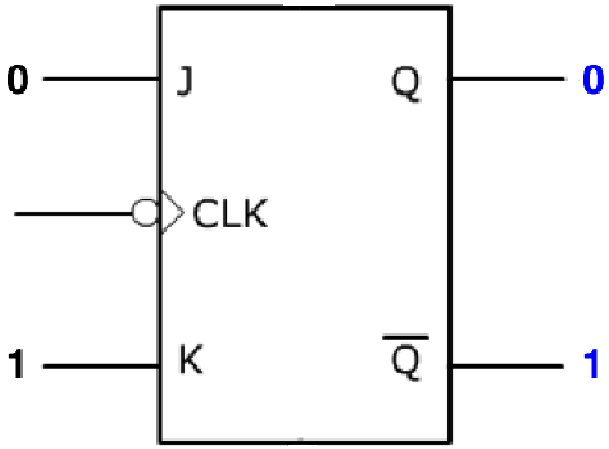


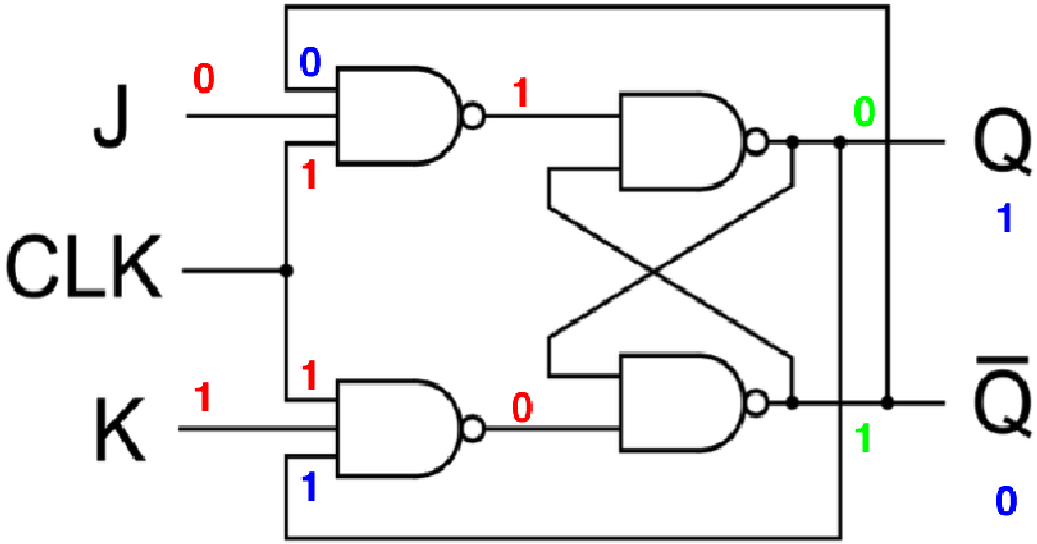


J	K	Q	Q'	Orig. Q	Orig. Q'
1	0	1	0	0	1

Mode of Operation: Reset

Reset: Q = 0.

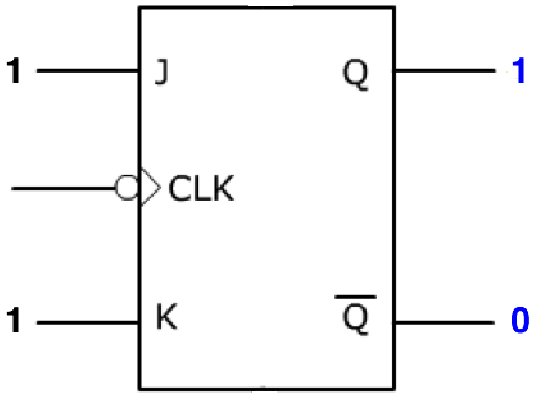


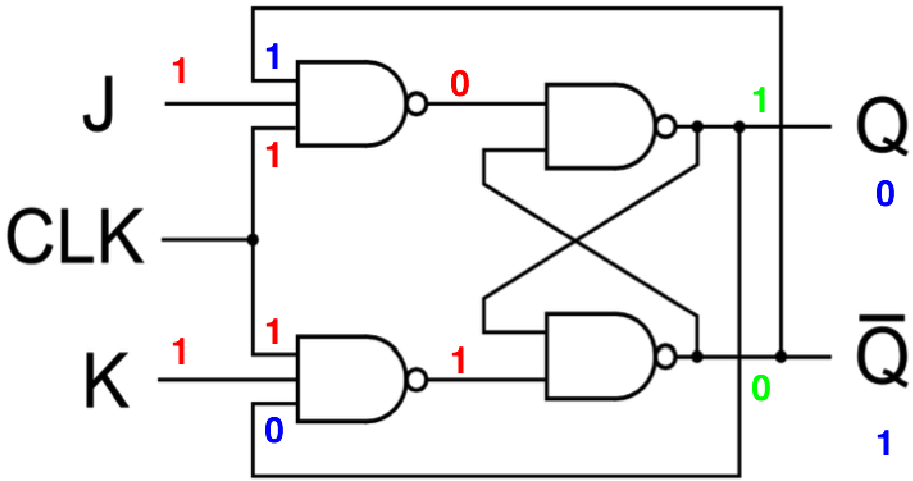


J	K	Q	Q'	Orig. Q	Orig. Q'
0	1	0	1	1	0

Mode of Operation: Toggle

Toggle: Q = Q'.

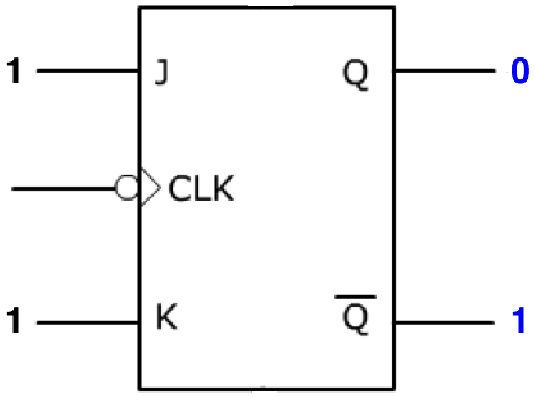


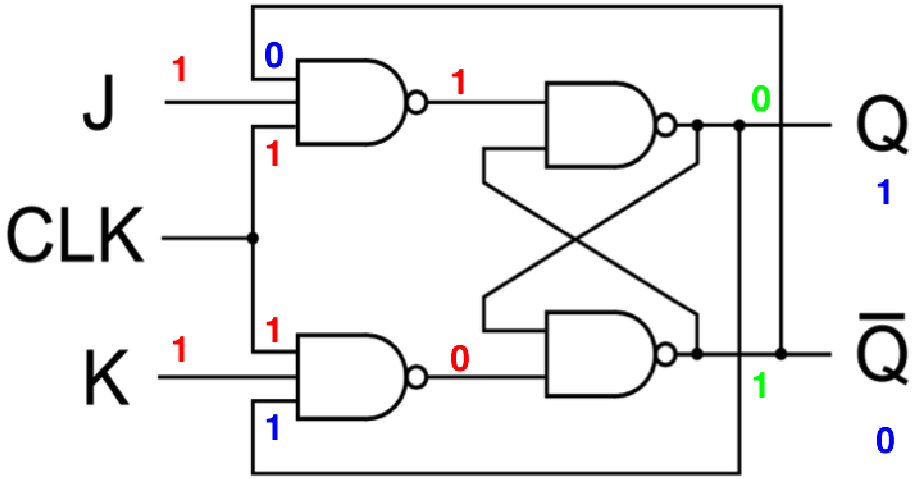


J	K	Q	Q'	Orig. Q	Orig. Q'
1	1	1	0	0	1

Mode of Operation: Toggle again

Toggle: Q = Q'.

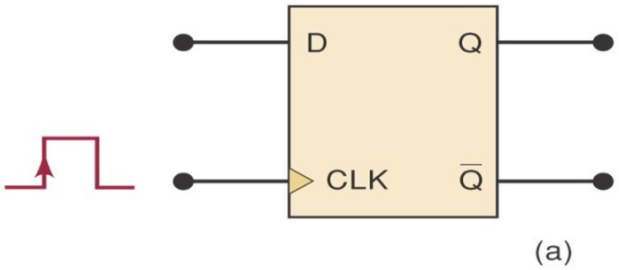




J	K	Q	Q'	Orig. Q	Orig. Q'
1	1	0	1	1	0

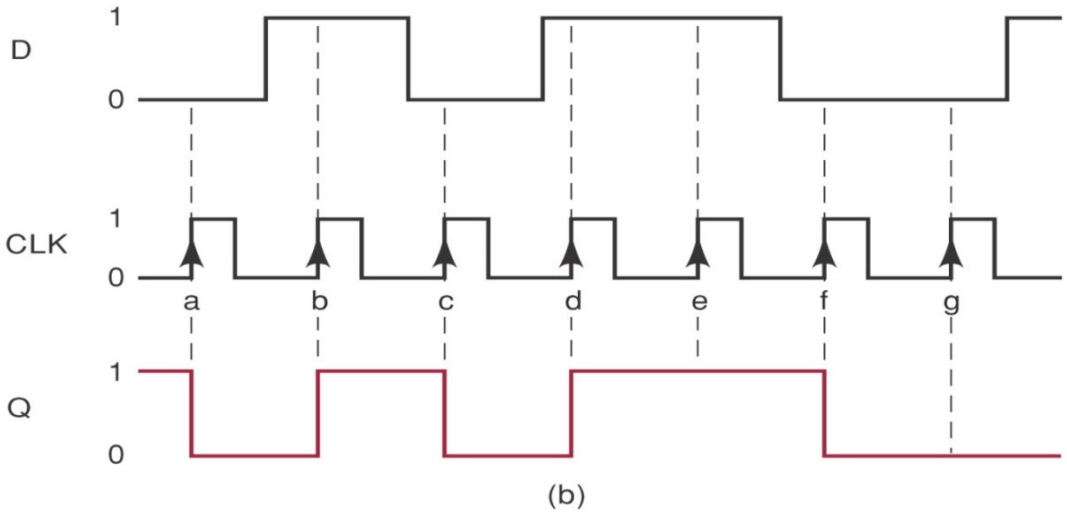
Clocked D Flip-Flop

- One data input.
- The output changes to the value of the input at either the positive going or negative going clock trigger.
- May be implemented with a J-K FF by tying the J input to the K input through an inverter.
- Useful for parallel data transfer.



(a)

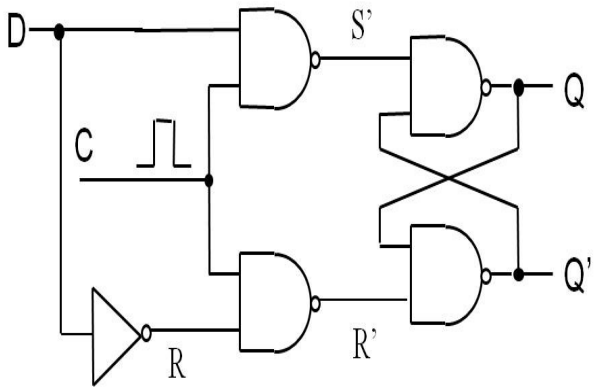
D	CLK	Q
0	↑	0
1	↑	1



(b)

Edge-triggered D flip-flop

D (Delay) Flip Flop



D	C	Q	Q'
0	1	0	1
1	1	1	0
X	0	Q_0	Q_0'

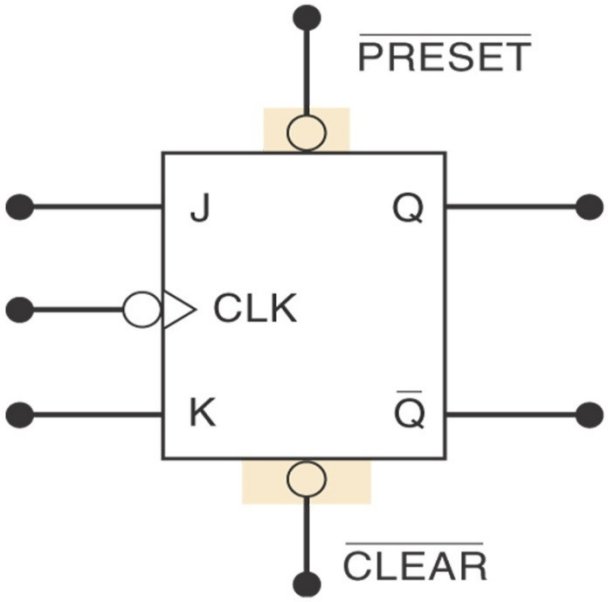
S	R	C	Q	Q'	
0	0	1	Q_0	Q_0'	Store
0	1	1	0	1	Reset
1	0	1	1	0	Set
1	1	1	1	1	Disallowed
X	X	0	Q_0	Q_0'	Store

When C is high, D passes from input to output (Q)

Asynchronous Inputs

- Inputs that depend on the clock are synchronous.
- Most clocked FFs have asynchronous inputs that do not depend on the clock.
- The labels PRE and CLR are used for asynchronous inputs.
- Active low asynchronous inputs will have a bar over the labels and inversion bubbles.
- If the asynchronous inputs are not used they will be tied to their inactive state.

Clocked J-K flip-flop with asynchronous inputs

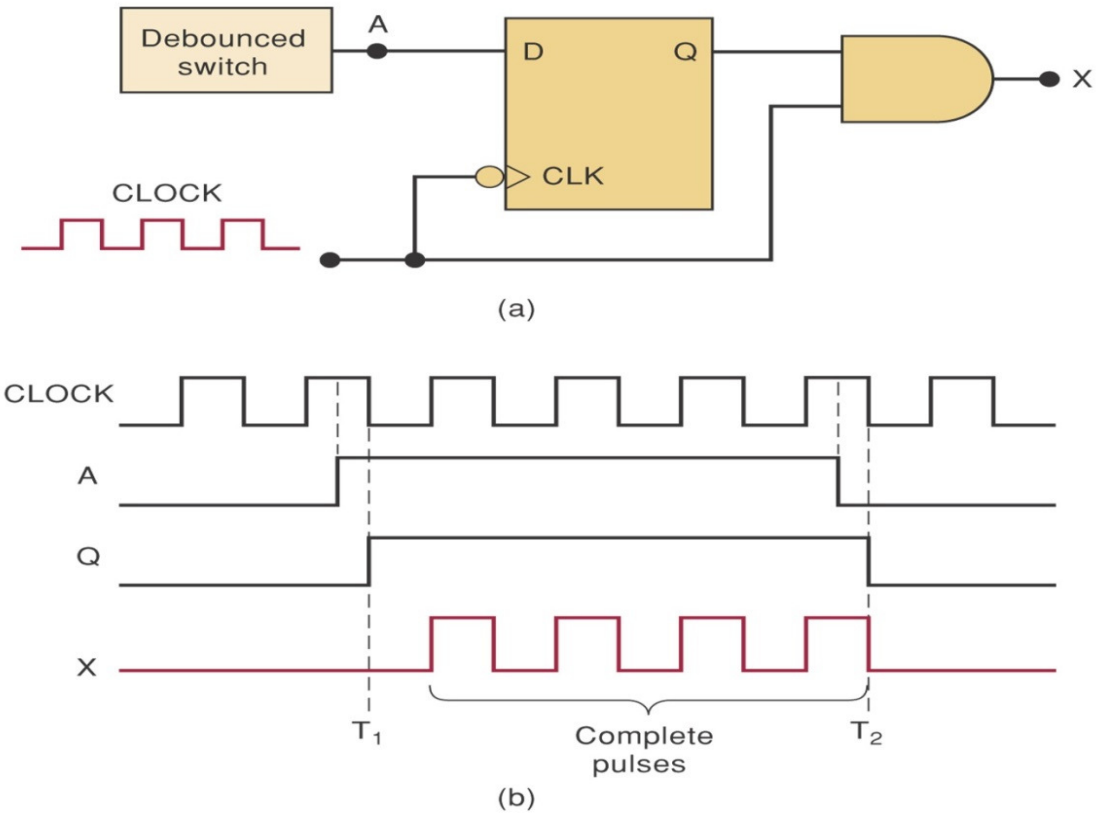


J	K	Clk	$\overline{PRE}$	$\overline{CLR}$	Q
0	0	↓	1	1	Q (no change)
0	1	↓	1	1	0 (Synch reset)
1	0	↓	1	1	1 (Synch set)
1	1	↓	1	1	$\overline{Q}$ (Synch toggle)
x	x	x	1	1	Q (no change)
x	x	x	1	0	0 (asynch clear)
x	x	x	0	1	1 (asynch preset)
x	x	x	0	0	(Invalid)

Flip-Flop Synchronization

- Most systems are primarily synchronous in operation, in that changes depend on the clock.
- Asynchronous and synchronous operations are often combined.
- The random nature of asynchronous inputs can result in unpredictable results.

The signal *A* has no effect until negative edge of clock.



Edge-triggered flip-flop can Synchronize Circuit

Master-Slave D Flip Flop

- **Consider two latches combined together**
- **Only one *C* value active at a time**
- **Output changes on falling edge of the clock**

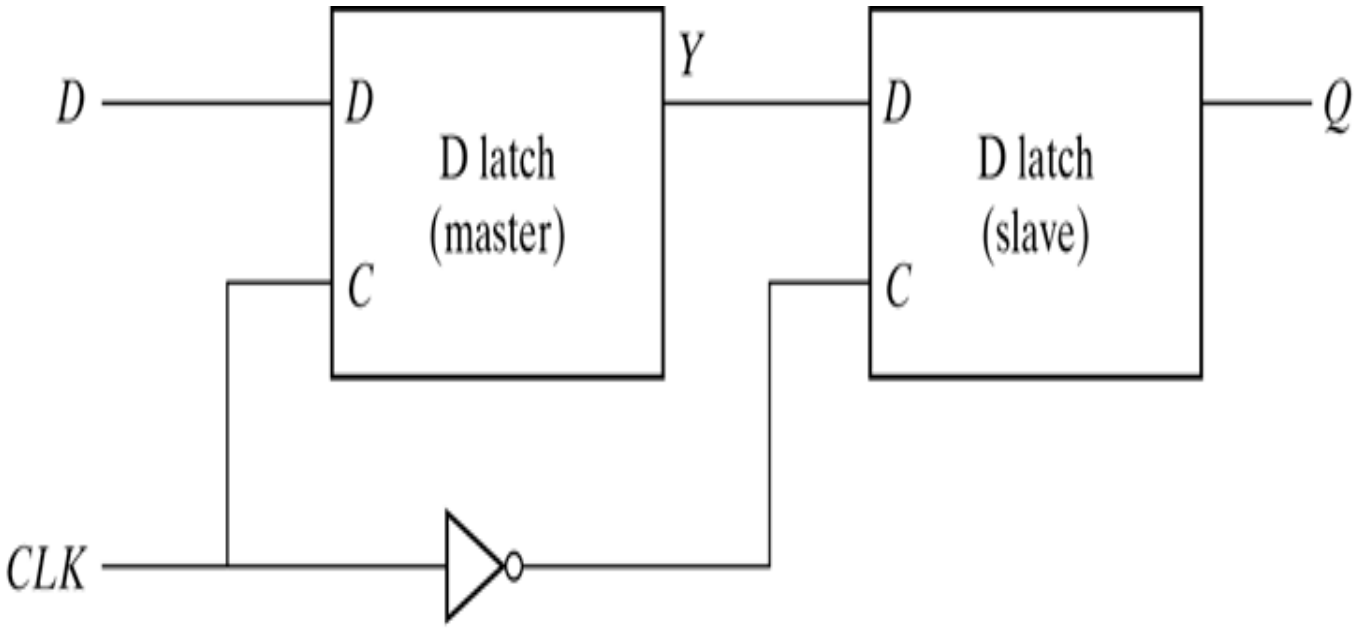
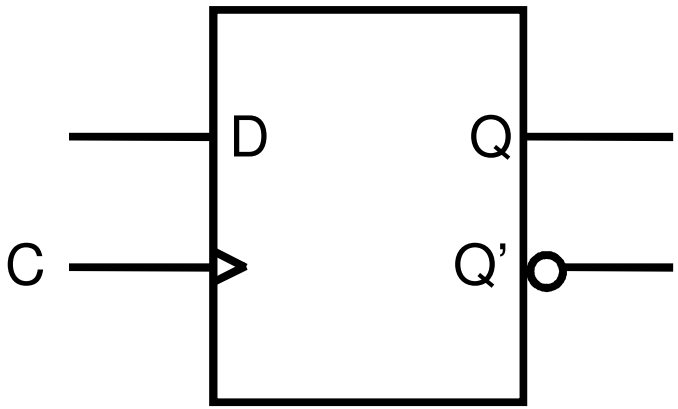


Fig. Master-Slave *D* Flip-Flop

- **Stores a value on the positive edge of *C***
- **Input changes at other times have no effect on output**

Positive edge triggered



D	C	Q	Q'
0	↑	0	1
1	↑	1	0
X	0	Q_0	Q_0'

D gets latched to Q on the rising edge of the clock.