1.

a) RegDst信号控制的多路选择器，输入2对应常数31，这里的31代表寄存器$ra的寄存器号，因为调用jal指令时需要进行$ra = PC+4 的操作，因此执行jal指令时需要RegDst信号为2；

b) 从指令表中可以看出只有sll、srl、sra三个指令用到了[10:6]的指令字段，为shamt，只有在执行这三条指令时才会用到[10:6]字段的参数；

c) MemtoReg信号控制的多路选择器输入2对应的输出为PC+4，所以在执行jal和jalr指令时需要MemtoReg信号为2，因为这些指令需要将下一条指令地址（PC+4）存入$ra或其他寄存器中；

d) PCSrc信号控制的多路选择器输入2对应的输出为寄存器ReadData1，即相应的指令[25:21](rs)，在执行jr和jalr时需要该信号输入2，因为这两个指令都有跳转到寄存器所在地址的功能。

e) ExtOP信号控制符号扩展，有符号数进行扩展时需要输入1，无符号数扩展时需要输入0，ExtOp用于控制到底进行有符号还是无符号的扩展；

f) sll指令中，若rt=rd=shamt=0，也不会进行任何操作，即为nop，不需要更改处理器结构。



|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | PCSrc  [1:0] | Branch | RegWrite | RegDst  [1:0] | MemRead | Memwrite | MemtoReg[1:0] | ALUSrc1 | ALUSrc2 | ExtOp | LuOp |
| lw | 00 | 0 | 1 | 00 | 1 | 0 | 01 | 0 | 1 | 1 | 0 |
| sw | 00 | 0 | 0 | XX | 0 | 1 | XX | 0 | 1 | 1 | 0 |
| lui | 00 | 0 | 1 | 00 | 0 | 0 | 00 | 0 | 1 | X | 1 |
| add | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 0 | 0 | X | X |
| Addu | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 0 | 0 | X | X |
| Sub | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 0 | 0 | X | X |
| Subu | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 0 | 0 | X | X |
| Addi | 00 | 0 | 1 | 00 | 0 | 0 | 00 | 0 | 1 | 1 | 0 |
| Addiu | 00 | 0 | 1 | 00 | 0 | 0 | 00 | 0 | 1 | 1 | 0 |
| And | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 0 | 0 | X | X |
| Or | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 0 | 0 | X | X |
| Xor | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 0 | 0 | X | X |
| Nor | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 0 | 0 | X | X |
| Andi | 00 | 0 | 1 | 00 | 0 | 0 | 00 | 0 | 1 | 0 | 0 |
| Sll | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 1 | 0 | X | X |
| Srl | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 1 | 0 | X | X |
| Sra | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 1 | 0 | X | X |
| Slt | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 0 | 0 | X | X |
| Sltu | 00 | 0 | 1 | 01 | 0 | 0 | 00 | 0 | 0 | X | X |
| Slti | 00 | 0 | 1 | 00 | 0 | 0 | 00 | 0 | 1 | 1 | 0 |
| Sltiu | 00 | 0 | 1 | 00 | 0 | 0 | 00 | 0 | 1 | 0 | 0 |
| Beq | 00 | 1 | 0 | XX | 0 | 0 | XX | 0 | 0 | 1 | 0 |
| J | 01 | X | 0 | XX | 0 | 0 | XX | X | X | X | X |
| Jal | 01 | X | 1 | 10 | 0 | 0 | 10 | X | X | X | X |
| Jr | 10 | X | 0 | XX | 0 | 0 | XX | X | X | X | X |
| jalr | 10 | X | 1 | 01 | 0 | 0 | 10 | X | X | X | X |