Laboratory Exercise 3

The purpose of this exercise is to design a combinational circuit that can multiply two unsigned numbers. First, you will design an array multiplier that does not use the multiplier LPM module from the Quartus II system. Consult your textbook for a descritpion of the array multiplier. Then, you will use the LPM module to accomplish the same task, and compare the results achieved. To make the design task more managable, start with a simple case of 4-bit numbers.

Part I
Design an array multiplier that multiplies 4-bit numbers, as follows:

1. Create a new project which will be used to implement the desired circuit on the Altera DE2 board.
2. Use switches SW_{11-8} to represent the number A and switches SW_{3-0} to represent B. The hexadecimal values of A and B are to be displayed on the 7-segment displays $HEX6$ and $HEX4$, respectively. The result $C = A * B$ is to be displayed on $HEX1$ and $HEX0$.
3. Generate the required Verilog file, include it in your project, and compile the circuit.
4. Use functional simulation to verify that your code is correct.
5. Assign the pins on the FPGA to connect to the switches and 7-segment displays, as indicated in the User Manual for the DE2 board.
6. Recompile the circuit and download it into the FPGA chip.
7. Test the functionality of your design by toggling the switches and observing the 7-segment displays.

Part II

Extend your multiplier to multiply 8-bit numbers. Use switches SW_{15-8} to represent the number A and switches SW_{7-0} to represent B. The hexadecimal values of A and B are to be displayed on the 7-segment displays $HEX7-6$ and $HEX5-4$, respectively. The result $C = A * B$ is to be displayed on $HEX3-0$.

Part III

Change your Verilog code to implement the 8 x 8 multiplier by using the *lpm_mult* module from the library of parameterized modules in the Quartus II system. Complete the design steps above. Compare the results in terms of the number of logic elements (LEs) needed.