ANALOG DEVICES

Advantiv
Advanced Television Solutions
by Analog Devices

PROGRAMMING GUIDE **AD9889B**

AD9889B/AD9389B

HDMI Transmitter

Rev. B December 2011

Analog Devices, Inc. (ADI) One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, USA Tel: 781.329.4700 Fax: 781.461.3113
www.analog.com

REVISION HISTORY

Rev. A:

Initial Release	**Extensive editing**

Rev. B:

12/2011	**Minor default register values.**
	R0x00 – Chip Revision changed from 0x10 to 0x00
	R0x3B – changed from 0x00 to 0x80 – sampling frequency from I2C register
	R0x94 – interrupt enable changed from 0x00 to 0xC0 – enabling HPD and Monitor sense automatically
	R0xCF – Packet Memory I2C address changed from 0xE0 to 0x70
Section 4.1	**Map address for EDID memory and Packet Memory were corrected to R0x43 and R0xCF respectively**
Section 4.3.2.1	**Corrected Clock Divide register bit – from R0x9D[3:2] to R0x9D[2]. Added explanation of use of clock delay with 2x clock.**
Section 4.4.1.1	**Clarified that AD9889B supports only 64-bit mode I2S audio.**
Section 4.9	**Clarified that hardware INT is a low active signal.**

TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

SECTION 1: INTRODUCTION

1.1 Scope and Organization

1.1.1 Organization

This document is intended to help a programmer understand the details of the operation of the AD9889B. It is divided into sections:

- ► Section 2: References is a list of other references, which will be helpful when designing with the HDMI Transmitter.
- ► Section 3: Quick Start Guide provides a reference to commonly used registers divided by function.
- ► Section 4: Programming Tasks is divided into common programming tasks. This section includes references to registers and detailed descriptions of the method to accomplish the task. For some tasks, the registers will be spread throughout the map, so this section helps the user locate the registers.
- ► Section 5: Register Map contains the complete register maps. The main register map contains cross-reference links to sections within the document that contain the relevant details on using each bit described.

1.1.2 Use of Register Bits

Different bits on a single byte may have various functions. ► Section 4: *Programming Tasks* may refer to an isolated bit. Using a "read, modify, write" method when changing the value of these bits is recommended to guarantee that other bits in the register will not be affected. To find the functions of other bits in the byte, refer to ► Section 5: *Register Map*, where the Reference column points to the section with more detailed information about the register.

1.1.3 Register Types

Registers that do not have a defined functionality will be one of three types:

Fixed	Value may need to be set one time, but should never be changed.
Reserved	Register exists, but has no function.
Not Used	Register does not exist and will always be read back as 0. Any register not defined in the complete register map fits this description.

1.1.4 Format Standards

In this document, ADI has chosen to represent data in the following ways:

0xNN	Hexadecimal (base-16) numbers are represented using the "C" language notation, preceded by 0x.
0bNN	Binary (base-2) numbers are represented using "C" language notation, preceded by 0b.
NN	Decimal (base-10) numbers are represented using no additional prefixes or suffixes.
Bit	Bits are numbered in little-endian format; i.e., the least-significant bit of a byte or word is referred to as bit 0.

Bit descriptions in the register maps are assumed to be binary.

1.1.5 Links

There are many links in this document to help with navigation. Use a mouse click to follow a link, and use the Alt key + left arrow key to return.

1.1.6 Symbols

Symbols are used to indicate internal and external document references as follows:

- ► Indicates a reference to another section of this document.
- ▹ Indicates a reference to another document, either an ADI document or an external specification.

SECTION 2: REFERENCES

2.1 ADI Documents and Other Resources

- AD9889B Data Sheet
- AD9889B Hardware User's Guide
- AD9889B Software Driver User's Guide

Additional product choices for Advanced TV applications are available on the Advantiv® site. Information about obtaining licenses required for using HDMI and HDCP technologies is available from www.hdmi.org and www.digital-cp.com, respectively.

2.2 Specifications

- EIA/CEA-861
- HDMI Specification 1.3
- HDCP 1.3
- IEC 60958
- IEC 61937
- The I2C-Bus Specification

SECTION 3: QUICK START GUIDE

The Quick Start guide brings attention to registers that need to be configured when initially bringing up the HDMI transmitter. For detailed information, refer to the section number link on the right side of the page. Complete registers and their descriptions are listed in ► Section 5*: Register Map*

Power-up the Tx (HPD must be high)	
0x41[6] = 0b0 for power-up – 0b1 for power-down	► 4.7
Fixed registers that must be set on power up	
0x0A[6:5] = 0b00	
0x98 = 0x07	► 4.2.7
0x9C = 0x38	► 4.2.7
0x9D[1:0] = 0b01	► 4.2.7
0xA2 = (0x87 for high speed 0x84 for low power)	► 4.2.7
0xA3 = (0x87 for high speed 0x84 for low power)	► 4.2.7
0xBB = 0xFF	► 4.2.7
Set up the video input mode	
0x15[3:0] – Video Format ID (default = 4:4:4)	► 4.3.1
0x16[5:4] – Input Color Depth for 4:2:2 (default = 12 bit)	► 4.3.1
0x16[3:2] – Video Input Style (default style = 1)	►4.3.1
0x17[1] – Aspect ratio of input video (4x3 = 0b0, 16x9 = 0b1)	► 4.3.1
Set up the video output mode	
0x16[7:6] = 0b0 for 4:4:4 – Output Format (4:4:4 vs 4:2:2)	► 4.3.5
0x18[7] = 0b1 for YCbCr to RGB – CSC Enable	► 4.3.7
0x18[6:5] = 0b00 for YCbCr to RGB – CSC Scaling Factor	► 4.3.7
0xAF[1] = 0b1 for HDMI – Manual HDMI or DVI mode select	► 4.2.2
HDCP	
0xBA[4] = 0b0 for AD9889B – 0b1 for AD9389B	
0xAF[7] = 0b1 for enable HDCP	► 4.6
0x97[6] – BKSV Interrupt Flag (Wait for value to be 0b1 then write 0b1)	► 4.6
Audio setup	
0x01 – 0x03 = 0x001800 for 48kHz - N Value	► 4.4.2
0x0A[4] – Audio Select (I2S = 0, SPDIF = 1)	► 4.4.2
Audio Mode	
0x44[7] = 0b1 – SPDIF Enable	► 4.4.1.2
0x0C[5:2] = 0b1111 – I2S Enable	► 4.4.1.1
0x15[7:4] – I2S Sampling Frequency	► 4.4.1.1
0x0A[3:2] – Audio Mode	► 4.4.1

SECTION 4: PROGRAMMING TASKS

4.1 I2C Bus

The AD9889B uses three I2C register maps. The SDA/SCL programming address for the Main Register Map is 0x72 or 0x7A, based on whether PD/AD is pulled high (10KΩ resistor to power supply = 0x7A) or pulled low (10KΩ resistor to GND = 0x72) when power is applied to the supplies. The user should wait 200ms for the address to be decided, after the power supplies are high, before attempting to communicate with the AD9889B using I2C. A complete listing of the Main Register Map is provided in ► Section 5: *Register Map*. Refer to the "I2C Interface (access to the AD9889B registers)" section in the ▹ *AD9889B Hardware User's Guide* for information about I2C hardware.

The device address for the Spare Packet Memory is programmable and is controlled by register 0xCF of the Main Register Map. The default setting is 0x70. The details of the Packet Memory Map can be found in ►Figure 8.

The EDID Memory address is programmable and controlled by register 0x43 of the Main Register Map. The default setting is 0x7E.

Table 1 I2C Addresses

I2C Address	Default	Control
Main Register Map	0x72/0x7A	State of PD/AD pin when power applied
Packet Memory Map	0x70	0xCF in Main Register Map
EDID Memory Map	0x7E	0x43 in Main Register Map

4.2 General Control

4.2.1 Hot Plug Detect (HPD) and Rx Sense

To operate the AD9889B, it is necessary to monitor the Hot Plug Detect (HPD) signal and power up the part after HPD becomes high. To power up the part, the Power Down register bit (0x41[6]) must be written to 0 when the HPD pin is high. The status of the HPD pin can be read in register bit 0x42[6].

When the signal on the HPD pin is low, some registers cannot be written to. When HPD goes from high to low, some registers will be reset to their defaults. For additional details see ► Table 57. Refer to ► 4.9 for details on the use of interrupts.

The best method to determine when the HPD is high is to use the interrupt system. The bit representing an HPD interrupt is 0x96[7]. Refer to ► 4.9 for details on the use of interrupts.

Rx Sense refers to the detection of TMDS clock line pull-ups in the HDMI sink. If greater than 1.8V is detected, the Rx Sense interrupt will be triggered and the Rx Sense State bit (0x42[5]) will be 1.

One reason to detect the Rx Sense is to delay powering up the chip until the Rx is actually ready to receive signals. A typical implementation for a sink is to tie the HDMI 5V to HPD through a series resistor. In this case, the HPD signal will be detected regardless of whether the sink is powered on and ready to receive audio and video. For this reason it is best to wait for both the Rx Sense and HPD before powering up the chip when trying to achieve minimum power consumption.

Table 2 HPD and Rx Sense related registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x41	R/W	[6]	*1******	Power Down	Main Power Down 0 = all circuits powered up 1 = power down the whole chip, except I2C, HPD interrupt and Rx Sense interrupt
► 0x42	RO	[7]	1*******	PD/AD Polarity Detection	Polarity Detected for the PD/AD Pin 0 = I2C address is 0x7A and power down pin is active low 1 = I2C address is 0x72 and power down pin is active high
		[6]	*0******	HPD State	State of the hot plug detection 0 = Hot Plug Detect not detected (low) 1 = Hot Plug detected (high)
		[5]	**0*****	Rx Sense State	State of the Rx Sense. 0 = HDMI clock termination not detected 1 = HDMI clock termination detected
► 0x94	R/W	[7]	0*******	HPD Interrupt Enable	HPD Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled
		[6]	*0******	Rx Sense Interrupt	Rx Sense Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled
► 0x96	R/W	[7]	0*******	HPD Interrupt	Interrupt for Hot Plug Detect (HPD) 1 = interrupt active 0 = interrupt not active
		[6]	*0******	Rx Sense Interrupt	Interrupt for Rx Sense 1 = interrupt active 0 = interrupt not active
► 0xA1	R/W	[6]	*0******	Rx Sense Power Down	Rx Sense Monitoring and Level II Power Down 0 = Rx Sense monitoring enabled 1 = Rx Sense monitoring disabled

4.2.2 HDMI DVI Selection

The HDMI Transmitter supports both HDMI and DVI modes. HDMI or DVI mode is selected by 0xAF[1]. In DVI mode no packets will be sent, and all registers relating to packets and InfoFrames will be disregarded. DVI only supports the RGB color space, so, if the input is not RGB, it is important to remember to set the color space conversion to output RGB when DVI is enabled. See ► 4.3.7 for details about the Color Space Converter.

Table 3 HDMI DVI Selection Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0xAF	R/W	[1]	******0*	HDMI DVI Select	HDMI Mode 0 = DVI 1 = HDMI

4.2.3 AV Mute

The AV Mute bits are sent to the Rx through the General Control Packet (GCP). One purpose of the AV Mute is to alert the Rx of a change in the TMDS clock so the Rx can mute audio and video. AV Mute also pauses HDCP encryption, so the HDCP link is maintained while the TMDS clock is not stable. It can also be used in general to tell

the sink to mute audio and video. AV Mute is not sufficient as a means to hide protected content, because the content is still sent even when AV Mute is enabled.

To use AV Mute, enable the GCP by setting the GC Packet Enable register bit (0x40[7]) to 1. To set AV mute, clear the Clear AV Mute bit (0x45[7] = 0) and set the Set AV Mute bit (0x45[6] = 1) to 1. To clear AV mute, clear Set AV Mute (0x45[6] = 0) and set Clear AV Mute (0x45[7] = 1). Note that it is invalid to set both bits to 1.

Table 4 AV Mute Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x40	R/W	[7]	0*******	GC Packet Enable	General Control Packet Enable 0 = disable 1 = enable
► 0x45	R/W	[7]	0*******	Clear AV Mute	Clear Audio Video Mute 0 = clear 1 = set clear av mute.
		[6]	*0******	Set AV Mute	Set Audio Video Mute 0 = clear 1 = set av mute.

4.2.4 TMDS Power-Down

The differential outputs of the AD9889B can be powered down. This can be useful for ensuring that no invalid data will be put on the HDMI link until the register settings have been confirmed.

Table 5 TMDS Power-Down Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0xA1	R/W	[5]	**0*****	Channel 0 Power Down	Channel 0 Power Down 0 = power up 1 = power down
		[4]	***0****	Channel 1 Power Down	Channel 1 Power Down 0 = power up 1 = power down
		[3]	****0***	Channel 2 Power Down	Channel 2 Power Down 0 = power up 1 = power down
		[2]	*****0**	Clock Driver Power Down	Clock Driver Power Down 0 = power up 1 = power down

4.2.5 Source Product Description (SPD) Packet

The Source Product Description (SPD) packet contains the vendor name and product description. One application of this packet is to allow the Rx to display the source information on an OSD. This information is in 7-bit ASCII format. Refer to the ▹ *HDMI 1.3a* specification for more detail.

Table 6 SPD Packet Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x40	R/W	[6]	*0******	SPD Packet Enable	Source Product Descriptor Packet Enable 0 = disable 1 = enable

Table 7 SPD Packet Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x52	R/W	[7:0]	00000000	SPD_PB1	User-defined
…	…	…	…	…	…
► 0x6A	R/W	[7:0]	00000000	SPD_PB25	User-defined

4.2.6 System Monitoring

The AD9889B utilizes both interrupts and registers to report errors and the status of internal operations. See ► 4.9 for details about using interrupts.

4.2.6.1 *HDCP Controller Status*

The current state of the HDCP controller can be read from the HDCP Controller State I2C register (0xC8 [3:0]). The codes for this register are shown in ► Table 8.

Table 8 HCDP Controller Status

0xC8 [3:0]	HDCP Controller State
0000	In Reset (No Hot Plug Detected)
0001	Reading EDID
0010	IDLE (Waiting for HDCP Requested)
0011	Initializing HDCP
0100	HDCP Enabled
0101	Initializing HDCP Repeater

4.2.6.2 *HDCP/EDID Controller Error Codes*

If an error occurs, the AD9889B can send and interrupt. See ► 4.9 for details about using interrupts. An error code is then reported in the HDCP Controller Error register (0xC8 [7:4]). ► Table 9 lists the possible error conditions and the corresponding 4-bit error code. The error code is only valid when the error interrupt is 1. The last error code will remain in the HDCP Controller Error register even when the interrupt is cleared.

Table 9 Error Code Definitions

Error Code	Error Condition
0000	No Error
0001	Bad Receiver BKSV
0010	Ri Mismatch
0011	Pj Mismatch
0100	I2C Error (usually a no-ack)
0101	Timed Out Waiting for Downstream Repeater DONE
0110	Max Cascade of Repeaters Exceeded
0111	SHA-1 Hash Check of KSV List Failed
1000	Too Many Devices Connected to Repeater Tree

Table 10 System Monitoring Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x94	R/W	[5]	**0*****	Vsync Interrupt Enable	Vsync Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled
		[4]	***0****	Audio FIFO Full Interrupt Enable	Audio FIFO Full Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled
		[3]	****0***	Embedded Sync Parity Error Interrupt Enable	Embedded Sync Parity Error Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled
► 0x95	R/W	[7]	0*******	HDCP Controller Error Interrupt Enable	HDCP Controller Error Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled
► 0x96	R/W	[5]	**0*****	Vsync Interrupt	Interrupt for active VS edge 1 = interrupt enabled 0 = interrupt disabled
		[4]	***0****	Audio FIFO Full Interrupt	Interrupt for audio FIFO overflow 1 = interrupt enabled 0 = interrupt disabled
		[3]	****0***	Embedded Sync Parity Error Interrupt	Interrupt for Embedded Sync Parity Error (1st error corrected 2nd error flagged) 1 = interrupt enabled 0 = interrupt disabled
► 0x97	R/W	[7]	0*******	HDCP Controller Error Interrupt	HDCP Controller Error Interrupt (See HDCP Controller Error bits 0xC8[7:4]) 1 = interrupt enabled 0 = interrupt disabled
► 0x9E	RO	[4]	***0****	PLL Lock Status	PLL Lock Status 0 = PLL not locked 1 = PLL locked
► 0xB8	RO	[4]	***0****	Key Reading Error	HDCP Key Reading Error 0 = Successful 1 = Error Reading Keys
► 0xC8	RO	[7:4]	0000****	HDCP Controller Error	Error code from latest HDCP/EDID Controller Error Interrupt (See ► Table 9)
		[3:0]	****0000	HDCP Controller State	Current state of the HDCP/EDID controller (See ► Table 8)

4.2.7 Fixed Registers That Must Be Set

After HPD becomes low the AD9889B will be powered down and many registers reset. When HPD becomes high, it must be powered up by using the Power Down register bit (0x41[6]). The following fixed registers should be set after power up:

Table 11 Fixed Registers That Must Be Set(Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x0A	R/W	[6:5]	*10*****	Fixed	Must be set to 0b00 for proper operation
► 0x98	R/W	[7:0]	00001011	Fixed	Must be written to 0x07 for proper operation
► 0x9C	R/W	[7:0]	01011010	Fixed	Must be written to 0x38 for proper operation
► 0x9D	R/W	[1:0]	******00	Fixed	Must be written to 0b01 for proper operation
► 0xA2	R/W	[7:0]	10000000	Fixed	Must be written as 0x87 for high speed operation (pixel clock > 80 MHz) Can be 0x84 for lower power operation (up to 80 MHz)
► 0xA3	R/W	[7:0]	10000000	Fixed	Must be written as 0x87 for high speed operation (pixel clock > 80 MHz) Can be 0x84 for lower power operation (up to 80 MHz)
► 0xBB	R/W	[7:0]	00000000	Fixed	Must be written to 0xFF for proper operation

4.3 Video Setup

4.3.1 Input Formatting

To use the AD9889B with a video input, the data clock, video data, and control signals must be clearly defined and the connection of these signals to the HDMI Tx must be understood. The AD9889B can accept video data from as few as eight pins (either YCbCr 4:2:2 double data rate [DDR] or YCbCr 4:2:2 with 2x pixel clock) or as many as 24 pins (RGB or YCbCr 4:4:4). Either separate control signals (Hsync, Vsync, and DE (Data Enable)), or control signals embedded in the video data in the style of the ITU BT.656, SMPTE 274M, and SMPTE 296M specifications are accepted. The clock can be either DDR or SDR (single data rate) depending on the format selected.

The AD9889B can detect all of the 59 video formats defined in the ▹ EIA/CEA-861D specification. The format is detected based on the frequency and polarity of the Hsyncs and Vsyncs.

▹ For timing details for video capture, refer to the "Functional Description" section of the *Hardware User Guide*.

The tables in section ► 4.3.2 define how the many different formats are accepted on the input video data lines.

Table 12 Input ID Selection

Input ID	Bits per Color	Pin Assignment Table	Maximum Input Clock	Format Name	Sync Type
0	8	► Table 13	165.0 MHz	RGB 4:4:4, YCbCr 4:4:4	Separate syncs
1	8, 10, 12	► Table 14	165.0 MHz	YCbCr 4:2:2	Separate syncs
2	8, 10, 12	► Table 15	165.0 MHz	YCbCr 4:2:2	Embedded syncs
3	8, 10, 12	► Table 16	82.5 MHz	YCbCr 4:2:2 2X clock	Separate syncs
4	8, 10, 12	► Table 17	82.5 MHz	YCbCr 4:2:2 2X clock	Embedded syncs
5	8, 10, 12	► Table 18	82.5 MHz	RGB 4:4:4, YCbCr 4:4:4 DDR	Separate syncs
6	8, 10, 12	► Table 19	82.5 MHz	YCbCr 4:2:2 DDR	Separate syncs

4.3.2 Video Input Tables

Table 13 RGB or YCbCr 444 (24 bits) with Separate Syncs. Input ID = 0.

Input Format	Data<23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RGB 444	R[7:0]								G[7:0]								B[7:0]							
YCbCr 444	Cr[7:0]								Y[7:0]								Cb[7:0]							
An input format of RGB 444 or YCbCr 444 can be selected by setting the input ID (R0x15 [3:1]) to 0x0. There is no need to set the Input Style (R0x16[3:2]).																								

Table 14 YCbCr 422 Formats (24, 20, or 16 bits) with Separate Syncs. Input ID = 1.

Input Format	Data<23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Style 1																								
YCbCr422 Sep. Sync (24 bit)	Cb[11:4]								Y[11:4]								Cb[3:0]				Y[3:0]			
	Cr[11:4]								Y[11:4]								Cr[3:0]				Y[3:0]			
YCbCr422 Sep. Sync (20 bit)	Cb[9:2]								Y[9:2]								Cb[1:0]				Y[1:0]			
	Cr[9:2]								Y[9:2]								Cr[1:0]				Y[1:0]			
YCbCr422 Sep. Sync (16 bit)	Cb[7:0]								Y[7:0]															
	Cr[7:0]								Y[7:0]															
Style 2																								
24 bit	Cb[11:0]												Y[11:0]											
	Cr[11:0]												Y[11:0]											
20 bit	Cb[9:0]										Y[9:0]													
	Cr[9:0]										Y[9:0]													
16 bit	Cb[7:0]								Y[7:0]															
	Cr[7:0]								Y[7:0]															
Style 3																								
24 bit	Y[11:0]												Cb[11:0]											
	Y[11:0]												Cr[11:0]											
20 bit	Y[9:0]										Cb[9:0]													
	Y[9:0]										Cr[9:0]													
16 bit	Y[7:0]								Cb[7:0]															
	Y[7:0]								Cr[7:0]															
An input with YCbCr 422 with separate syncs can be selected by setting the Input ID (R0x15[3:1]) to 0x1. The data bit width (24, 20, or 16 bits) must be set with R0x16 [5:4]. The 3 input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2].																								

Table 15 YCbCr 422 Formats (24, 20 or 16 bits) with Embedded Syncs. Input ID = 2

Input Format	Data<23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Style 1																								
YCbCr422 Sep. Sync (24 bit)	Cb[11:4]								Y[11:4]								Cb[3:0]				Y[3:0]			
	Cr[11:4]								Y[11:4]								Cr[3:0]				Y[3:0]			
YCbCr422 Sep. Sync (20 bit)	Cb[9:2]								Y[9:2]								Cb[1:0]				Y[1:0]			
	Cr[9:2]								Y[9:2]								Cr[1:0]				Y[1:0]			
YCbCr422 Sep. Sync (16 bit)	Cb[7:0]								Y[7:0]															
	Cr[7:0]								Y[7:0]															
Style 2																								
24 bit	Cb[11:0]												Y[11:0]											
	Cr[11:0]												Y[11:0]											
20 bit	Cb[9:0]										Y[9:0]													
	Cr[9:0]										Y[9:0]													
16 bit	Cb[7:0]								Y[7:0]															
	Cr[7:0]								Y[7:0]															
Style 3																								
24 bit	Y[11:0]												Cb[11:0]											
	Y[11:0]												Cr[11:0]											
20 bit	Y[9:0]										Cb[9:0]													
	Y[9:0]										Cr[9:0]													
16 bit	Y[7:0]								Cb[7:0]															
	Y[7:0]								Cr[7:0]															

An input with YCbCr 422 with embedded syncs (SAV [Start of Active Video] and EAV [End of Active Video]) can be selected by setting the Input ID (R0x15[3:1]) to 0x2. The data bit width (24 = 12bit, 20 = 10 bit, or 16 = 8 bits) must be set with R0x16 [5:4]. The 3 input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The only difference between Input ID 1 and Input ID 2 is that the syncs on ID 2 are embedded in the data much like an ITU 656 style bus running at 1X clock and double width.

Table 16 YCbCr 422 Formats (12, 10, or 8 bits) with Separate Syncs. Input ID = 3.

Input Format	Data <23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Style 1																								
12 bit									Cb/Y/Cr/Y[11:4]												[3:0]			
10 bit									Cb/Y/Cr/Y[9:2]												[1:0]			
8 bit									Cb/Y/Cr/Y[7:0]															
Style 2																								
12 bit													Cb/Y/Cr/Y[11:0]											
10 bit															Cb/Y/Cr/Y[9:0]									
8 bit																	Cb/Y/Cr/Y[7:0]							

An input with YCbCr 422 data and separate syncs can be selected by setting the Input ID (R0x15[3:1]) to 0x3. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The 2 input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. This mode requires an input clock 2X the pixel rate.

Table 17 YCbCr 422 Formats (12, 10, or 8 bits) with Embedded Syncs. Input ID = 4.

Input Format	Data <23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Style 1																								
12 bit									Cb/Y/Cr/Y[11:4]												[3:0]			
10 bit									Cb/Y/Cr/Y[9:2]												[1:0]			
8 bit									Cb/Y/Cr/Y[7:0]															
Style 2																								
12 bit													Cb/Y/Cr/Y[11:0]											
10 bit															Cb/Y/Cr/Y[9:0]									
8 bit																	Cb/Y/Cr/Y[7:0]							

An input with YCbCr 422 and embedded syncs (ITU 656 based) can be selected by setting the Input ID (R0x15[3:1]) to 0x4. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The 2 input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The order of data input is the order in the table. For example, data is accepted as: Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3… This mode requires an input clock 2X the pixel rate.

Table 18 RGB or YCbCr 444 (12 bits) DDR with Separate Syncs. Input ID = 5.

Input Format	Data <23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Style 1																								
RGB 444 (DDR)	1st edge												G[3:0]				B[7:0]							
	2nd edge												R[7:0]								G[7:4]			
YCbCr444(DDR)	1st edge												Y[3:0]				Cb[7:0]							
	2nd edge												Cr[7:0]								Y[7:4]			
Style 2																								
RGB 444 (DDR)	1st edge												R[7:0]								G[7:4]			
	2nd edge												G[3:0]				B[7:0]							
YCbCr444 (DDR)	1st edge												Cr[7:0]								Y[7:4]			
	2nd edge												Y[3:0]				Cb[7:0]							
Style 3																								
YCbCr444 (DDR)	1st edge												Y[7:0]								Cb[7:4]			
	2nd edge												Cb[3:0]				Cr[7:0]							

An input format of RGB 444 DDR or YCbCr 444 DDR can be selected by setting the input ID (R0x15 [3:1]) to 0b101. The 3 input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 422 word and should be where DE starts.

Table 19 **YCbCr 422 (12, 10, or 8 bits) DDR with Separate Syncs. Input ID = 6.**

Input Format	Data<23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Style 1																								
YCbCr422 Sep Syncs (DDR) 12 bit	1st pixel	1st edge											Y[7:4]				Cb[3:0]				Y[3:0]			
		2nd edge											Cb[11:4]								Y[11:8]			
	2nd pixel	1st edge											Y[7:4]				Cr[3:0]				Y[3:0]			
		2nd edge											Cr[11:4]								Y[11:8]			
YCbCr422 Sep Syncs (DDR) 10 bit	1st pixel	1st edge											Y[5:4]		Cb[3:0]				Y[3:0]					
		2nd edge											Cb[9:4]						Y[9:6]					
	2nd pixel	1st edge											Y[5:4]		Cr[3:0]				Y[3:0]					
		2nd edge											Cr[9:4]						Y[9:6]					
YCbCr 422 Sep. Syncs (DDR) 8 bit	1st pixel	1st edge											Cb[3:0]				Y[3:0]							
		2nd edge											Cb[7:4]				Y[7:4]							
	2nd pixel	1st edge											Cr[3:0]				Y[3:0]							
		2nd edge											Cr[7:4]				Y[7:4]							
Style 2																								
12 bit	1st pixel	1st edge											Y[11:0]											
		2nd edge											Cb[11:0]											
	2nd pixel	1st edge											Y[11:0]											
		2nd edge											Cr[11:0]											
10 bit	1st pixel	1st edge											Y[9:0]											
		2nd edge											Cb[9:0]											
	2nd pixel	1st edge											Y[9:0]											
		2nd edge											Cr[9:0]											
8 bit	1st pixel	1st edge											Y[7:0]											
		2nd edge											Cb[7:0]											
	2nd pixel	1st edge											Y[7:0]											
		2nd edge											Cr[7:0]											
Style 3																								
12 bit	1st pixel	1st edge											Cb[11:0]											
		2nd edge											Y[11:0]											
	2nd pixel	1st edge											Cr[11:0]											

		2nd edge											Y[11:0]									
10 bit	1st pixel	1st edge											Cb[9:0]									
		2nd edge											Y[9:0]									
	2nd pixel	1st edge											Cr[9:0]									
		2nd edge											Y[9:0]									
8 bit	1st pixel	1st edge											Cb[7:0]									
		2nd edge											Y[7:0]									
	2nd pixel	1st edge											Cr[7:0]									
		2nd edge											Y[7:0]									

An input format of YCbCr 422 DDR can be selected by setting the input ID (R0x15 [3:1]) to 0b110. The 3 different input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The Data Input Edge is defined in R0x16 [1]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 422 word and should be where DE starts.

Figure 1 **DDR DE Timing - Register 0x16[1] = 1**

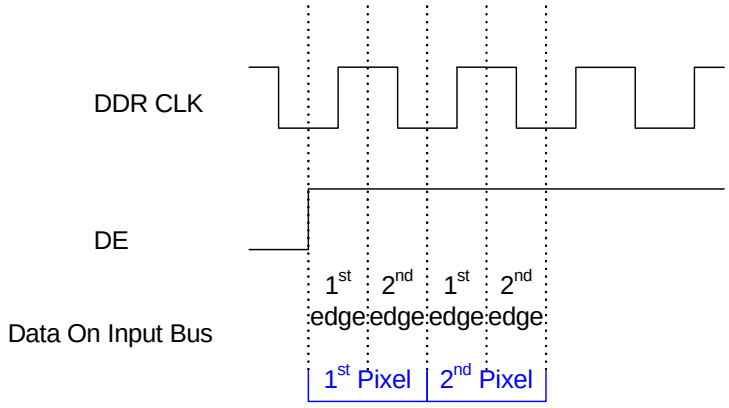
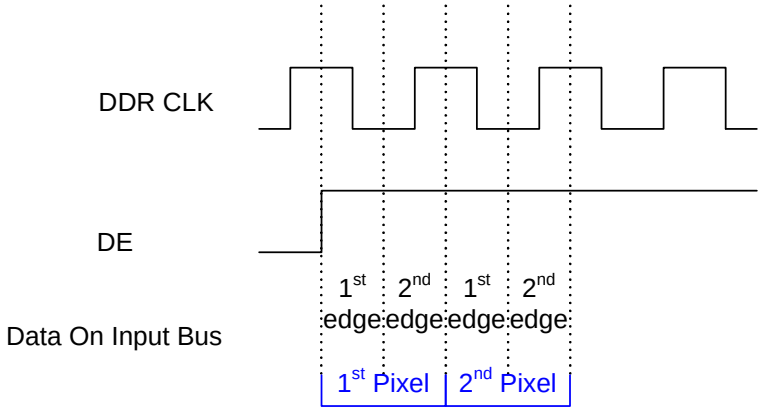


Figure 2 **DDR DE Timing - Register 0x16[1] = 0**



4.3.2.1 *Input Data Clock*

When using an input format where the clock is 2 times the frequency of the data, such as 480i at 27MHz, the CLK Divide register (0x9D[2]) needs to be set to 1 and the CLK Divide enable register (0xA4[6]) needs to be set to 1. Register 0xBA[7:5] controls the clock delay for the video data capture and must be set to 0b000 when using the 2x clock input format.

Table 20 Input formatting Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
►0x15	R/W	[3:1]	****000*	Input ID	Input Video Format See tables in section ► 4.3.2 000 = 24 bit RGB or YCbCr 4:4:4 001 = 16 bit YCbCr 4:2:2 (separate syncs) 010 = 16 bit YCbCr 4:2:2 (embedded syncs) 011 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, separate syncs) 100 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, embedded syncs) 101 = 12 bit RGB 4:4:4 or YCbCr (DDR with separate syncs) 110 = 8,10,12 bit YCbCr 4:2:2 (DDR with separate syncs) 111 = undefined
►0x16	R/W	[5:4]	**00****	4:2:2 Width	4:2:2 Width for Input Video Data. See tables in section ► 4.3.2 00 = invalid 10 = 12 bit 01 = 10 bit 11 = 8 bit
		[3:2]	****00**	Input Style	Styles refer to the input pin assignments. See tables in section ► 4.3.2 00 = style 1 01 = style 2 10 = style 1 11 = style 3
		[1]	******0*	DDR Input Edge	Video data input edge selection. Defines the first half of pixel data clocking edge. Used for DDR Input ID 5 and 6 only. 0 = falling edge 1 = rising edge
►0x9D	R/W	[2]	*****0**	CLK Divide	Input Video CLK Divide 0 = input clock not divided 1 = input clock divided by 2
►0xA4	R/W	[6]	*0******	CLK Divide Enable	Input Video CLK Divide Enable 0 = clock divider disabled, 0x9D[2] must be set to 0b0 1 = clock divider set by 0x9D[2]
►0xBA	R/W	[7:5]	000*****	Clock Delay	Delay Adjust for the Input Video CLK Capture Should be set to 0b011 if no delay is desired 000 = -1200ps 001 = -800ps 010 = -400ps 011 = no delay 100 = 400ps 101 = 800ps 110 = 1200ps 111 = invert

4.3.3 Video Mode Detection

The video mode detection feature can inform the user of the CEA 861D defined Video Identification (VIC) of the video being input to the AD9889B, as well as some additional formats. If an 861D format is detected, the VIC code is contained in register 0x3E[7:2]. Some additional non-861D formats are contained in 0x3F[7:5]. Some information from

the user is required to make the VIC determination for formats which can't be distinguished by the automatic detection system. The aspect ratio (0x17[1]) is used to distinguish between 861D video timing codes where aspect ratio is the only difference. The Low Refresh Rate bit (0x48[7]) informs the detection logic that a low-frequency Vsync format is being used. These include 1080p formats 32 and 33. For 240p and 288p modes the number of total lines can be selected in 0x3F[4:3]. The VIC detected is also affected by pixel repeat; see ► 4.3.4.

The detected VIC will be sent in the AVI InfoFrame unless pixel repetition is applied, causing the sent VIC to be different. To override the VIC detection, the pixel repeat mode must be set to manual by setting register 0x3B[6:5] to 0b11. The desired VIC is input into 0x3C[5:0]. The transmitter can support non-CEA 861D modes, but these will not be automatically detected. In this case the VIC should be 0. Also, when using 3D formats the VIC detection will not be valid.

Table 21 Mode Detection Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x15	R/W	[0]	*******0	Low Refresh Rate Video	Low Refresh Rate Video 0 = Normal Mode 1 = Allow detection of CEA 861 VIC codes 32,33, or 34
► 0x17	R/W	[1]	******0*	Aspect Ratio	Aspect ratio of input video. 0 = 4:3 1 = 16:9
► 0x3C	R/W	[5:0]	**000000	VIC Manual	User programmed VIC to send to Rx. (Value Defined in CEA861D)
► 0x3D	RO	[7:6]	00******	Pixel Repeat to Rx	Pixel Repetition Sent to Rx Status 00 = 1x 01 = 2x 10 = 4x 11 = 4x
		[5:0]	**000000	VIC to Rx	VIC sent to HDMI Rx and Used in the AVI InfoFrame Status (Value Defined in CEA861D)
► 0x3E	RO	[7:2]	000000**	VIC Detected	VIC detected by video front-end (Value Defined in CEA861D)
► 0x3F	RO	[7:5]	000*****	Auxiliary VIC Detected	This register is for video input formats that are not inside the 861D table. 000 = see 0x3E for video input information 001 = 240p Not Active 010 = 576i Not Active 011 = 288p Not Active 100 = 480i Active 101 = 240p Active 110 = 576i Active 111 = 288p Active
		[4:3]	***00***	Progressive Mode Information	Information about 240p and 288p modes. Case 1: 240p 01 = 262 lines 10 = 263 lines Case 2: 288p 01 = 312 lines 10 = 313 lines 11 = 314 lines

4.3.4 Pixel Repetition

Pixel repetition is used in HDMI to increase the amount of blanking period available to send packets or to increase the pixel clock to meet the minimum specified clock frequency. The AD9889B offers three choices for the user to implement this function: auto mode, manual mode, and max mode (R0x3B[6:5]). If using SPDIF or I2S the AD9889B can automatically select the necessary pixel repetition multiple for combinations of video format and audio sample rate. The video is converted to the appropriate format within the AD9889B, and the resulting VIC is sent in the AVI InfoFrame.

In automatic mode, the AD9889B takes the audio sampling rate and detected VIC information as parameters to decide if pixel repeat is needed to obtain sufficient blanking periods to send the audio. For I2S, the sample rate is determined by register 0x15. The audio sampling rate is either determined by the channel status information of the incoming SPDIF data, or by setting register 0x15. In the case of SPDIF, the source of the sampling rate information is set in register 0x3B[7]. With I2S, the sampling rate is always set by the user. If the pixel repetition factor is adjusted to meet bandwidth requirements, then the detected input VIC may be different from the VIC sent to the Rx. The VIC of the actual video sent, which is included in the AVI InfoFrame, can be seen in register 0x3D[5:0].

In the manual pixel repeat selection case, the VIC sent in the AVI info frame will need to be set in register 0x3C. The multiplication of the input clock must be programmed in 0x3B[6:5], and the pixel repeat value sent to the Rx must be programmed in 0x3B[4:3]. Refer to the ▹ *HDMI 1.3a* specification for more details on valid pixel repeat formats.

Max mode works in the same way as the automatic mode, except that it will always select the highest pixel repeat multiple the HDMI Tx is capable of. This makes the video timing independent of the audio sampling rate. This mode is not typically used.

Table 22 Pixel Repetition Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x15	R/W	[7:4]	0000****	Sampling Frequency	Sampling frequency for I2S audio. This information is used for both Channel Status and determining the pixel repetition. 0011 = 32kHz 0000 = 44.1kHz 0010 = 48kHz 1000 = 88.2kHz 1010 = 96kHz 1100 = 176.4kHz 1110 = 192kHz
► 0x3B	R/W	[7]	1*******	Audio Sampling Frequency Select	Select source of audio sampling frequency for pixel repeat and I2S mode 4 0 = use sampling frequency from stream 1 = use sampling frequency from I2C register
		[6:5]	*00*****	PR Mode	Pixel Repetition Mode Selection. Set to b00 unless non-standard video is supported. 00 = auto mode 01 = max mode 10 = manual mode. See 0x3B bits [4:3][1] 11 = manual mode[1]
		[4:3]	***00***	PR PLL Manual	The clock multiplication of the input clock used in manual pixel repetition. 00 = x1 01 = x2 10 = x4 11 = x4
		[2:1]	*****00*	PR Value Manual	User programmed pixel repetition number to send to Rx used in manual pixel repetition. 00 = x1 01 = x2 10 = x4 11 = x4
► 0x3C	R/W	[5:0]	**000000	VIC Manual	User programmed VIC to send to Rx. (Value Defined in CEA861D)
► 0x3D	RO	[7:6]	00******	Pixel Repeat to Rx	The actual pixel repetition sent to Rx
		[5:0]	**000000	VIC to Rx	VIC sent to HDMI Rx and Used in the AVI InfoFrame Status (Value Defined in CEA861D)

4.3.5 4:2:2 4:4:4 Conversion

The AD9889B can up-convert from 4:2:2 format to 4:4:4 format as well as down-convert from 4:4:4 to 4:2:2. To convert from 4:4:4 to 4:2:2, the video data always goes through a filter first to remove any artificial down-sampling noise. To convert from 4:2:2 to 4:4:4, the AD9889B utilizes either the zero-order up-conversion (repetition) or first-order up-conversion (linear interpolation). The type of conversion, zero or first order, can be selected in register 0x17[2], and first order will give the best results.

The up-conversion and down-conversions are automatically applied when the video output format does not match the video input format. The input format is selected as described in ► 4.3.1, and the output format is selected in bits 0x16[7:6].

[1] 0b10 and 0b11 are the same

Table 23 4:4:4 4:2:2 Conversion Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x16	R/W	[7:6]	00******	Output Format	Video Output Format In HDMI mode, this should be written along with AVI InfoFrame Y1Y0 (0x55[6:5]). 00 = RGB 4:4:4 01 = YCbCr 4:4:4 11 = YCbCr 4:2:2
► 0x17	R/W	[2]	*****0**	4:2:2 to 4:4:4 Interpolation Style	4:2:2 to 4:4:4 Up Conversion Method 1 = use first order interpolation 0 = use zero order repetition

4.3.6 DE, Hsync and Vsync Generation

When transmitting video data across the TMDS interface, it is necessary to have an Hsync, Vsync, and Data Enable (DE) defined for the image. There are three methods for sync input to the AD9889B.

Separate Hsync, Vsync, and DE

For this method, all necessary signals are provided so neither Sync generation nor DE generation is required. If desired, the user can adjust the Hsync and Vsync timing relative to DE (refer to Hsync and Vsync adjustment section). Also, the DE timing can be adjusted relative to Hsync and Vsync.

Embedded Syncs (SAV and EAV)

This method requires that Hsync and Vsync be generated. Registers 0x30 through 0x34 and 0x17[6:5] contain the settings for Hsync and Vsync generation in the embedded sync decoder section. The AD9889B will use the signal generated by the EAV and SAV as the DE by default, but a new DE can also be generated

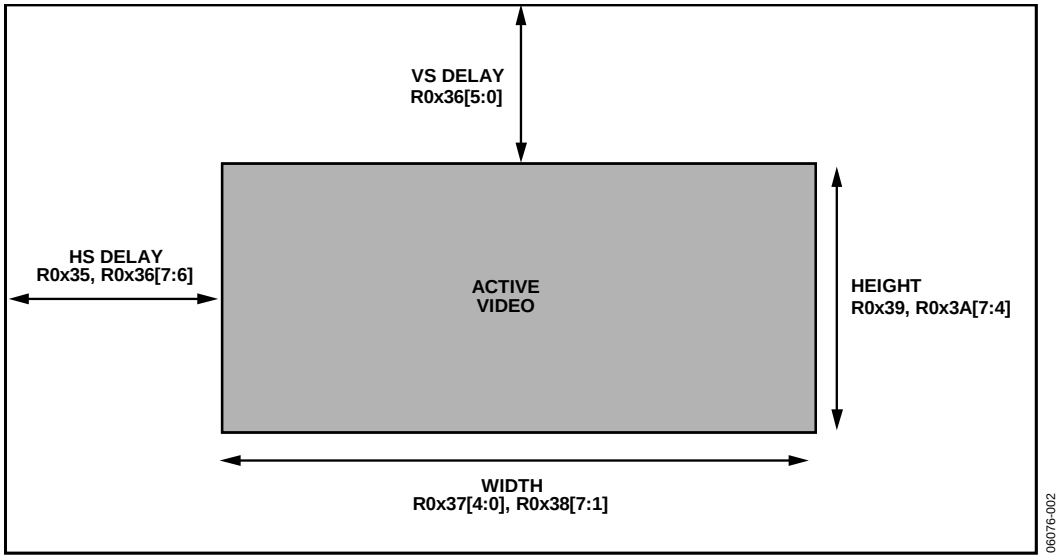
Separate Hsync and Vsync only

This method requires that a DE be generated. Registers 0x35 – 0x3A contain the settings for the DE generation. DE generation must be enabled using register bit 0x17[0] = 1.

4.3.6.1 *DE generation*

To properly frame the active video, the AD9889B can use an external DE (via an external pin) or can generate its own DE signal. To activate the internal DE generation, set register 0x17[0] to '1'. Registers 0x35 – 0x3A are used to define the DE. Registers 0x35 and 0x36[7:6] define the number of pixels from the Hsync leading edge to the DE leading edge minus 1. Register 0x36[5:0] is the number of Hsyncs between leading edge of VS and DE. Register 0x37[7:5] defines the difference of Hsync counts during Vsync blanking for the two fields in interlaced video. Registers 0x37[4:0] and 0x38[7:1] indicate the width of the DE. Registers 0x39 and 0x3A[7:4] are the number of lines of active video. These adjustments are illustrated in ► Figure 3.

Figure 3 **Active Video**



4.3.6.2 *Embedded Sync Input Mode*

The F, H, and V codes from the embedded syncs define the DE by default in the AD9889B. To achieve 861D formats at the output by default, the embedded sync V signal needs to be aligned with the data as specified in the 861D specification.

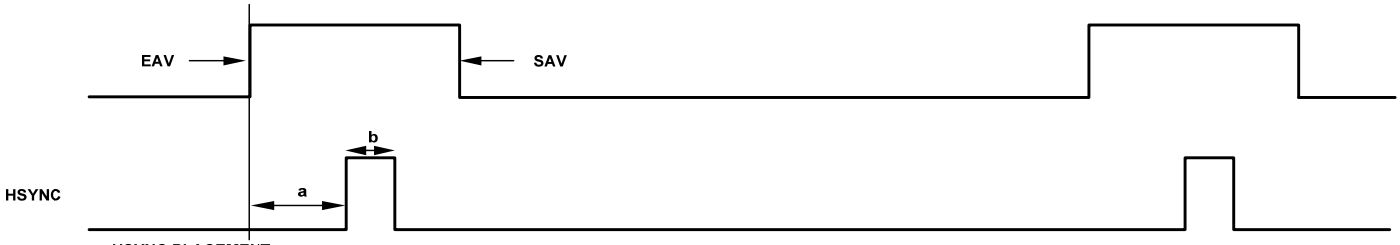
For video with embedded syncs, it is necessary to reconstruct the Hsync and Vsync. This is done with registers 0x30 – 0x34 and 0x17[6:5]. Registers 0x30 and 0x31[7:6] specify the number of pixels between the Hsync leading edge and the trailing edge of DE. Registers 0x31[5:0] and 0x32[7:4] are the duration of the Hsync in pixel clocks. Registers 0x32[3:0] and 0x33[7:2] are the number of Hsync pulses between the trailing edge of the last DE and the leading edge of the Vsync pulse. Registers 0x33[1:0] and 0x34[7:0] are the duration of Vsync in units of Hsyncs. Hsync and Vsync polarity can be specified by setting registers 0x17[5] and 0x17[6]. ► Figure 4 - Figure 5 show the sync generation parameters.

The internal DE generator can also be enabled when using embedded syncs by setting register 0x17[0] to '1'. The default reference points for the DE parameters are the Hsync and Vsync from the embedded sync decoder block. These are defined by registers 0x30 – 0x34.

4.3.6.3 *Hsync and Vsync Adjustment*

Hsync and Vsync can also be adjusted based on a DE input. Setting 0x41[1] to '1' enables this function (when using embedded syncs 0x41[1] should be set to 0). Registers 0x30-0x34, and 0x17[6:5] are shared with the embedded sync decoder and the sync adjustment block for setting the Hsync and Vsync parameters, so only one can be used at a time. The parameters work the same way as in embedded sync decoding except the DE input is used instead of the F, H, and V codes.

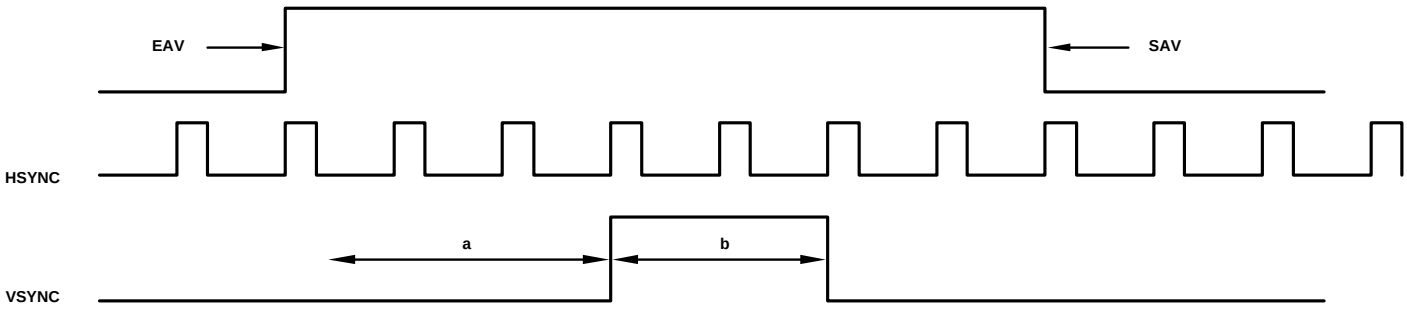
Figure 4 Hsync Reconstruction



a: HSYNC PLACEMENT
R0x30, R0x31[7:6] and
R0xD7, R0xD8[7:6]

b: HSYNC DURATION
R0x31[5:0], R0x32[7:4] and
R0xD8[5;0], R0xD9[7:4]

Figure 5 Vsync Reconstruction (Centered)



a: VSYNC PLACEMNT
R0x32[3:0], R0x33[7:2] and
R0xD9[3:0], R0xDA[7:2]
b: VSYNC DURATION
R0x33[1:0], R0x34 and
R0xDA[1:0], R0xDB

Table 24 DE and Hsync/Vsync Generation and Adjustment Common Settings

Format	Hsync Placement	Hsync Duration	Vsync Placement	Vsync Duration	Hsync Polarity	Vsync Polarity	Hsync Delay	Vsync Delay	Offset	Width	Height
480i	19	62	4	3	0	0	118	18	0	720	240
576i	12	63	2	3	0	0	131	22	0	720	288
480p	16	62	9	6	0	0	121	36	0	720	480
576p	12	64	5	5	0	0	131	44	0	720	576
720p-60	110	40	5	5	1	1	259	25	0	1280	720
720p-50	440	40	5	5	1	1	259	25	0	1280	720
1080i-30	88	44	2	5	1	1	191	20	0	1920	540
1080i-25	528	44	2	5	1	1	191	20	0	1920	540
1080p-60	88	44	4	5	1	1	191	41	0	1920	1080
1080p-50	528	44	4	5	1	1	191	41	0	1920	1080
1080p-24	638	44	4	5	1	1	191	41	0	1920	1080

Table 25 Common Register Settings for DE Generation

	0x35	0x36	0x37	0x38	0x39	0x3A
720p - 50	0x40	0xD9	0x0A	0x00	0x2D	0x00
720p – 60	0x40	0xD9	0x0A	0x00	0x2D	0x00
480p	0x1E	0x64	0x05	0xA0	0x1E	0x00
480i	0x1D	0x92	0x05	0xA0	0x0F	0x00
1080i -25	0x2F	0xD4	0x0F	0x00	0x21	0xC0
1080i – 30	0x2F	0xD4	0x0F	0x00	0x21	0xC0
576p	0x20	0xEC	0x05	0xA0	0x24	0x00
576i	0x20	0xD6	0x05	0xA0	0x12	0x00
1080p-60	0x2F	0xE9	0x0F	0x00	0x43	0x80
1080p-50	0x2F	0xE9	0x0F	0x00	0x43	0x80
1080p-24	0x2F	0xE9	0x0F	0x00	0x43	0x80

Table 26 Register Settings for Embedded Sync Processing and Sync Adjustment

Register (Main Map)	0x30	0x31	0x32	0x33	0x34	0x17[6:5]
720p - 50	0x6E	0x02	0x80	0x14	0x05	0x0
720p – 60	0x1B	0x82	0x80	0x14	0x05	0x0
480p	0x04	0x03	0xE0	0x24	0x06	0x3
480i	0x04	0xC3	0xE0	0x10	0x03	0x3
1080i -25	0x84	0x02	0xC0	0x08	0x05	0x0
1080i – 30	0x16	0x02	0xC0	0x08	0x05	0x0
576p	0x03	0x04	0x00	0x14	0x05	0x3
576i	0x03	0x03	0xF0	0x08	0x03	0x3
1080p-60	0x16	0x02	0xC0	0x10	0x05	0x0
1080p-50	0x843	0x042	0xC0	0x10	0x05	0x0
1080p-24	0x9F	0x82	0xC0	0x10	0x05	0x0

Table 27 DE, Hsync, and Vsync Generation Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x17	R/W	[6]	*0******	Vsync Polarity (Embedded Sync Decoder)	Vsync polarity for Embedded Sync Decoder and Sync Adjustment 0 = high polarity 1 = low polarity
		[5]	**0*****	Hsync Polarity (Embedded Sync Decoder)	Hsync polarity for Embedded Sync Decoder and Sync Adjustment 0 = high polarity 1 = low polarity
		[0]	*******0	DE Generator Enable	Enable DE Generator See registers 0x35 – 0x3A 0 = disable 1 = enable
► 0x30	R/W	[7:0]	00000000	Hsync Placement MSB (Embedded Sync Decoder)	Upper 8 bits for Embedded Sync Decoder Hsync Placement (In Pixels)
► 0x31	R/W	[7:6]	00******	Hsync Placement LSB (Embedded Sync Decoder)	Lower 2 bits for Embedded Sync Decoder Hsync Placement (In Pixels)
		[5:0]	**000000	Hsync Duration MSB (Embedded Sync Decoder)	Upper 6 bit for Embedded Sync Decoder Hsync Duration (In Pixels)
► 0x32	R/W	[7:4]	0000****	Hsync Duration LSB (Embedded Sync Decoder)	Lower 4 bits for Embedded Sync Decoder Hsync Duration (In Pixels)
		[3:0]	****0000	Vsync Placement MSB (Embedded Sync Decoder)	Upper 4 bits for Embedded Sync Decoder Vsync Placement (In Hsyncs)
► 0x33	R/W	[7:2]	000000**	Vsync Placement LSB (Embedded Sync Decoder)	Lower 6 bits for Embedded Sync Decoder Vsync Placement (In Hsyncs)
		[1:0]	******00	Vsync Duration MSB (Embedded Sync Decoder)	Upper 2 bit for Embedded Sync Decoder Vsync Duration (In Hsyncs)
► 0x34	R/W	[7:0]	00000000	Vsync Duration LSB (Embedded Sync Decoder)	Lower 8 bits for Embedded Sync Decoder Vsync Duration (In Hsyncs)

Address	Type	Bits	Default Value	Register Name	Function
► 0x35	R/W	[7:0]	00000000	Hsync Delay MSB (DE Generator)	Upper 8 bits for DE Generation Hsync Delay (In Pixels)
► 0x36	R/W	[7:6]	00******	Hsync Delay LSB (DE Generator)	Lower 2 bits for DE Generation Hsync Delay (In Pixels)
		[5:0]	**000000	Vsync Delay (DE Generator)	Vsync Delay for DE Generation. (In Hsyncs)
► 0x37	R/W	[7:5]	000*****	Interlace Offset (DE Generator)	Interlace Offset For DE Generation Sets the difference (in hsyncs) in field length between field 0 and field 1
		[4:0]	***00000	Active Width MSB (DE Generator)	Upper 5 bits for DE Generation Active Width (In Pixels)
► 0x38	R/W	[7:1]	0000000*	Active Width LSB (DE Generator)	Lower 7 bits for DE Generation Active Width (In Pixels)
► 0x39	R/W	[7:0]	00000000	Active Height MSB (DE Generator)	Upper 8 bits for DE Generation Active Height (In Lines)
► 0x3A	R/W	[7:4]	0000****	Active Height LSB (DE Generator)	Lower 4 bits for DE Generation Active Height (In Lines)
► 0x41	R/W	[1]	******0*	Sync Adjustment Enable	Sync Adjustment Enable See register 0xD7 – 0xDD and 0x17[6:5] 0 = sync adjustment disabled 1 = sync adjustment enabled

4.3.7 Color Space Converter (CSC)

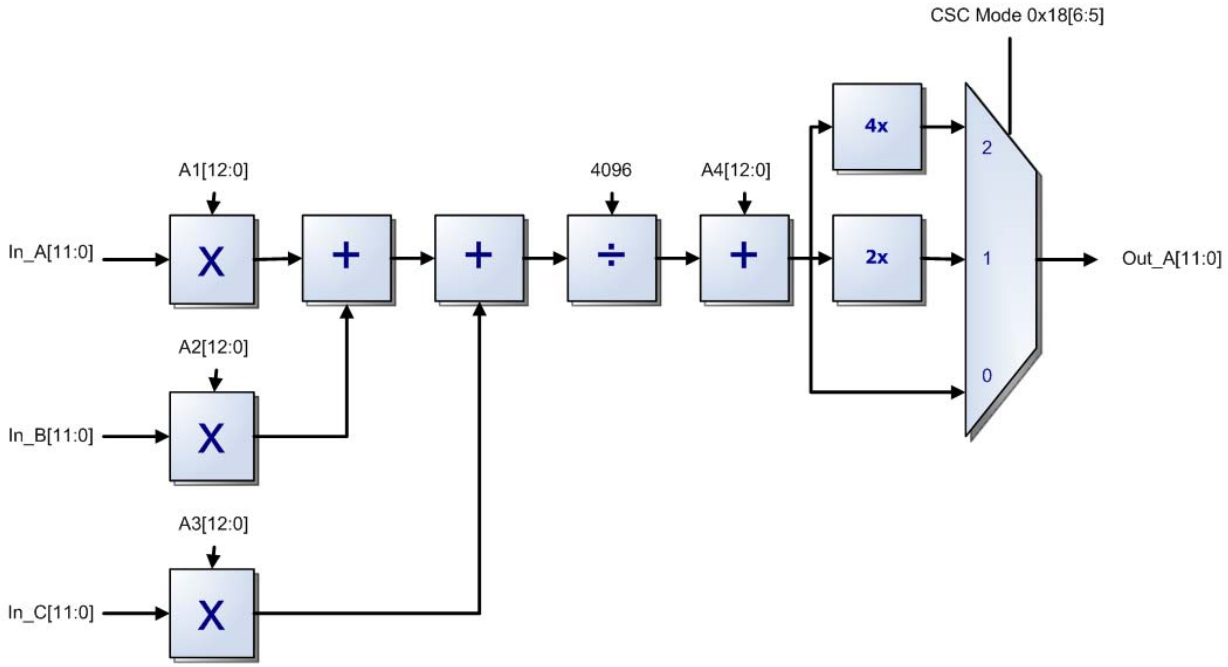
The color space converter (CSC) is a flexible 3x3 matrix that is capable of converting between a wide variety of color spaces. This section contains full details on the function of the CSC and register settings for common conversions.

4.3.7.1 *Color Space Conversion (CSC) Matrix*

The color space conversion (CSC) matrix in the AD9889B is a 3 x 3 matrix with full programmability of all coefficients in the matrix. Each coefficient is 13 bit 2s complement to ensure that signal integrity is maintained. The CSC is designed to run at pixel rates of up to 170MHz. With the "any-to-any" color space conversion capability, formats such as RGB, YUV, YCbCr and others are supported by the CSC. When changing colorspace, it is recommended that the writes to the coefficients occur during the Vsync blanking period. The Vsync interrupt of the AD9889B should be used to synchronize this timing.

The CSC contains three identical processing channels, one of these is shown in ► Figure 6. The main inputs, In_A, In_B, and In_C, come from inputs to the AD9889B. Each input to the individual channels to the CSC is multiplied by a separate coefficient. In ► Figure 6 these coefficients are marked A1, A2, and A3. The variable labeled A4 in ► Figure 6 is used as an offset control for Channel A in the CSC. The functional diagram for a single channel in the CSC, as per ► Figure 6, is repeated for the other two remaining channels, B and C. The coefficients for these channels are called B1, B2, B3, B4, C1, C2, C3 and C4.

Figure 6 Single CSC channel



The equations performed by the CSC are detailed as follows:

Equation 1: CSC Channel A

$$Out\_A = \left[In\_A\frac{A1}{4096} + In\_B\frac{A2}{4096} + In\_C\frac{A3}{4096} + A4 \right] 2^{CSC\_Mode}$$

Equation 2: CSC Channel B

$$Out\_B = \left[In\_A\frac{B1}{4096} + In\_B\frac{B2}{4096} + In\_C\frac{B3}{4096} + B4 \right] 2^{CSC\_Mode}$$

Equation 3: CSC Channel C

$$Out\_C = \left[In\_A\frac{C1}{4096} + In\_B\frac{C2}{4096} + In\_C\frac{C3}{4096} + C4 \right] 2^{CSC\_Mode}$$

As can be seen from *Equations 1-3*, the *A1-A3, B1-B3*, and *C1- C3* coefficients are used to scale the primary inputs. The values of A4, B4 and C4 are then added as offsets. The CSC Mode bits (register 0x17[4:3]) allow the user to implement conversion formulas in which the conversion coefficients are ≥ 1. In other words, if an equation is being implemented whose coefficients are ≥ 1, the CSC Mode bits can be used to ensure that the resulting output code does not exceed the 12-bit limit of 4095. ► Table 28 describes the conditions under which each CSC Mode setting should be used. Note that if any coefficient in any of the three CSC equations requires scaling (CSC Mode ≠ 0), then all coefficients, including the offset values, are scaled as indicated by *Equations 1 - 3*. The values of A1 - A4, B1 - B4, and C1 - C4 will equal the coefficients from the desired conversion formula multiplied by $\frac{4096}{2^{CSC\_Mode}}$.

► Table 39 contains the register descriptions for all of the CSC control registers.

Table 28 CSC Mode Settings

CSC Mode	Conversion Coefficient
00	N < 1
01	1 ≤ N <2
10	2 ≤ N < 4

It should be noted that, in order for the CSC to operate properly, the channel mapping shown in ► Table 29 must be followed.

Table 29 CSC Port Mapping

Channel	CSC Channel
Red/Cr	A
Green/Y	B
Blue/Cb	C

Table 30 HDTV YCbCr (16to 235) to RGB (16to 235)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xAC	0x53	0x08	0x00	0x00	0x00	0x19	0xD6
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1C	0x56	0x08	0x00	0x1E	0x88	0x02	0x91
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1F	0xFF	0x08	0x00	0x0E	0x85	0x18	0xBE

Table 31 HDTV YCbCr (16to 235) to RGB (0 to 255)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1C	0x1E	0x1F
Value	0xE7	0x34	0x04	0xAD	0x00	0x00	0x1C	0x1B
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1D	0xDC	0x04	0xAD	0x1F	0x24	0x01	0x35
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x00	0x04	0xAD	0x08	0x 7C	0x1B	0x77

Table 32 SDTV YCbCr (16to 235) to RGB (16 to 235)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xAA	0xF8	0x08	0x00	0x00	0x00	0x1A	0x84
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1A	0x6A	0x08	0x00	0x1D	0x50	0x04	0x23
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1F	0xFC	0x08	0x00	0x0D	0xDE	0x19	0x13

Table 33 SDTV YCbCr (16to 235) to RGB (0 to 255) - (Default Value)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xE6	0x69	0x04	0xAC	0x00	0x00	0x1C	0x81
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1C	0xBC	0x04	0xAD	0x1E	0x6E	0x02	0x20
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1F	0xFE	0x04	0xAD	0x08	0x1A	0x1B	0xA9

Table 34 RGB (16 to 235) to HDTV YCbCr (16to 235)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x88	0x2E	0x18	0x93	0x1F	0x3F	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x03	0x67	0x0B	0x71	0x01	0x28	0x00	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1E	0x21	0x19	0xB2	0x08	0x2D	0x08	0x00

Table 35 RGB (0 to 255) to HDTV YCbCr (16to 235)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x86	0xFF	0x19	0xA6	0x1F	0x5B	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x02	0xE9	0x09	0xCB	0x00	0xFD	0x01	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1E	0x66	0x1A	0x9B	0x06	0xFF	0x08	0x00

Table 36 RGB (16 to 235) to SDTV YCbCr (16to 235)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x88	0x2E	0x19	0x26	0x1E	0xAC	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x04	0xC9	0x09	0x65	0x01	0xD2	0x00	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1D	0x3F	0x1A	0x93	0x08	0x2E	0x08	0x00

Table 37 RGB (0 to 255) to SDTV YCbCr (16to 235)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x86	0xFF	0x1A	0x24	0x1E	0xDD	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x04	0x18	0x08	0x0A	0x01	0x8F	0x01	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1D	0xA5	0x1B	0x5C	0x06	0xFF	0x08	0x00

Table 38 Identity Matrix (Input = Output)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xA8	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x00	0x00	0x08	0x00	0x00	0x00	0x00	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x00	0x00	0x00	0x08	0x00	0x00	0x00

Table 39 Color Space Converter (CSC) Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x17	R/W	[4:3]	***10***	Color Space Converter Mode	Color Space Converter Mode Sets the fixed point position of the CSC coefficients. Including the a4, b4, c4, offsets. 00 = +/- 1.0, -4096<->4095 01 = +/- 2.0, -8192<->8190 1x = +/- 4.0, -16384<->16380
► 0x18	R/W	[4:0]	***00110	A1 MSB (CSC)	Color space Converter (CSC) coefficient for equations: $Out\_A = \left[In\_A\frac{A1}{4096} + In\_B\frac{A2}{4096} + In\_C\frac{A3}{4096} + A4 \right] 2^{CSC\_Mode}$ $Out\_B = \left[In\_A\frac{B1}{4096} + In\_B\frac{B2}{4096} + In\_C\frac{B3}{4096} + B4 \right] 2^{CSC\_Mode}$ $Out\_C = \left[In\_A\frac{C1}{4096} + In\_B\frac{C2}{4096} + In\_C\frac{C3}{4096} + C4 \right] 2^{CSC\_Mode}$
► 0x19	R/W	[7:0]	01100010	A1 LSB (CSC)	
► 0x1A	R/W	[4:0]	***00100	A2 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x1B	R/W	[7:0]	10101000	A2 LSB (CSC)	
► 0x1C	R/W	[4:0]	***00000	A3 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x1D	R/W	[7:0]	00000000	A3 LSB (CSC)	
► 0x1E	R/W	[4:0]	***11100	A4 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x1F	R/W	[7:0]	10000100	A4 LSB (CSC)	
► 0x20	R/W	[4:0]	***11100	B1 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x21	R/W	[7:0]	10111111	B1 LSB (CSC)	
► 0x22	R/W	[4:0]	***00100	B2 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x23	R/W	[7:0]	10101000	B2 LSB (CSC)	
► 0x24	R/W	[4:0]	***11110	B3 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x25	R/W	[7:0]	01110000	B3 LSB (CSC)	
► 0x26	R/W	[4:0]	***00010	B4 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x27	R/W	[7:0]	00011110	B4 LSB (CSC)	
► 0x28	R/W	[4:0]	***00000	C1 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x29	R/W	[7:0]	00000000	C1 LSB (CSC)	
► 0x2A	R/W	[4:0]	***00100	C2 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x2B	R/W	[7:0]	10101000	C2 LSB (CSC)	
► 0x2C	R/W	[4:0]	***01000	C3 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x2D	R/W	[7:0]	00010010	C3 LSB (CSC)	
► 0x2E	R/W	[4:0]	***11011	C4 MSB (CSC)	See description for registers 0x18 and 0x19
► 0x2F	R/W	[7:0]	10101100	C4 LSB (CSC)	
► 0x3B	R/W	[0]	*******0	Color Space Converter Enable	Color Space Converter Enable 0 = Color space converter disabled 1 = Color space converter enabled

4.3.8 Video InfoFrame and Other Video Related Packet

Video related InfoFrames include the AVI InfoFrame, MPEG InfoFrame, SP Packet.

4.3.8.1 *AVI InfoFrame*

The AVI InfoFrame is sent to the receiver to help it determine the intended aspect ratio and other formatting parameters of the video being transmitted across the HDMI link. The Y1Y0 bits (0x45[5:4]), which tell the sink whether YCbCr 4:2:2,4:4:4 or RGB are sent, and the Picture Aspect Ratio bits (0x46[3:2]) are required fields. Other field data can be entered if the information is available.

The Active Format Information Status bit (0x45[3]) tells whether the Bar Information, Scan Information, Colorimetry, Non-uniform Picture Scaling, and Active Aspect Ratio fields contain valid information.

The Active Format Aspect Ratio bits (0x47[7:4]) give the receiver useful information about the video that can be used to improve the picture. The Active Format Description code from the ETSI TR 101 151 version 1.4.1 Digital Video Broadcasting Specification, which is mentioned in ▹ *CEA 861D*, should be entered into this field. Additional formats can be entered manually in the bar information fields.

Registers 0x48 – 0x4F tell the receiver if there are black bars included in the video stream. Register 0x45[2:1] tells the receiver which bar information is valid: none, horizontal, vertical, or both.

Table 40 InfoFrame and Other Packet Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
►0x45	R/W	[5:4]	**00****	Y1Y0 (AVI InfoFrame)	Output format - this should be written when 0x16[7] is written. 00 = RGB 01 = YCbCr 422 10 = YCbCr 444 11 = reserved
		[3]	****0***	Active Format Information Status (AVI InfoFrame)	Active Format Information Present 0 = no data 1 = Active format Information valid
		[2:1]	*****00*	Bar Information (AVI InfoFrame)	B[1:0] 00 = invalid bar 01 = vertical 10 = horizontal 11 = Both
►0x46	R/W	[7:6]	00******	Scan Information (AVI InfoFrame)	S[1:0] 00 = no data 01 = TV 10 = PC 11 =None
		[5:4]	**00****	Colorimetry (AVI InfoFrame)	C[1:0] 00 = no data 01 = ITU601 10 = ITU709 11 = Extended Colorimetry Information Valid (Indicated in register 0x57[6:4])
		[3:2]	****00**	Picture Aspect Ratio (AVI InfoFrame)	M[1:0] 00 = no data 01 = 4:3 10 = 16:9 11 = None
		[1:0]	******00	Non-uniform Picture Scaling (AVI InfoFrame)	SC[1:0] 00 = unknown 01 = scaling in Horizontal direction 10 = scaling in Vertical direction 11 = scaling in Both H and V directions
►0x47	R/W	[7:4]	0000****	Active Format Aspect Ratio (AVI InfoFrame)	R[3:0] 1000 = Same as aspect ratio 1001 = 4:3 (center) 1010 = 16:9 (center) 1011 = 14:9 (center)
►0x48	R/W	[7:0]	00000000	Active Line Start LSB (AVI InfoFrame)	Active Line Start This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar.
►0x49	R/W	[7:0]	00000000	Active Line Start MSB (AVI InfoFrame)	
►0x4A	R/W	[7:0]	00000000	Active Line End LSB (AVI InfoFrame)	Active Line End This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar.
►0x4B	R/W	[7:0]	00000000	Active Line End MSB (AVI InfoFrame)	
►0x4C	RO	[7:0]	00000000	Active Pixel Start LSB (AVI InfoFrame)	Active Pixel Start This represents the last pixel in a vertical pillar-bar at the left side of the picture. If 0, there is no left bar.
►0x4D	R/W	[7:0]	00000000	Active Pixel Start MSB (AVI InfoFrame)	

►0x4E	R/W	[7:0]	00000000	Active Pixel End LSB (AVI InfoFrame)	Active Pixel End This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar.
►0x4F	R/W	[7:0]	00000000	Active Pixel End MSB (AVI InfoFrame)	
►0xCD	R/W	[7]	0*******	AVI_PB1[7] (AVI InfoFrame)	Reserved bit from AVI PB1
		[6]	*0******	ITC (AVI InfoFrame)	IT Content 0 = no IT content 1 = IT content is present
		[5:3]	**000***	EC[2:0] (AVI InfoFrame)	Extended Colorimetry 000 = $xvYCC_{601}$ 001 = $xvYCC_{709}$ See latest HDMI specification for other values
►0xCE	R/W	[7:0]	0000****	AVI_PB5[7:4] (AVI InfoFrame)	Reserved bits from AVI PB5

4.3.8.2 *MPEG InfoFrame*

The MPEG InfoFrame is defined in ▹ *CEA 861D*. Currently, the specification does not recommend using this InfoFrame. Register 0x40[5] tells the AD9889B whether or not to send the MPEG InfoFrame.

Table 41 MPEG Packet Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
►0x6B	R/W	[7:0]	00000000	MPEG_DB1	Lower byte of MPEG bit rate: Hz
►0x6C	R/W	[7:0]	00000000	MPEG_DB2	Lower middle byte of MPEG bit rate: Hz
►0x6D	R/W	[7:0]	00000000	MPEG_DB3	Upper middle byte of MPEG bit rate: Hz
►0x6E	R/W	[7:0]	00000000	MPEG_DB4	Upper byte of MPEG bit rate: Hz
►0x6F	R/W	[7]	0*******	MPEG FR	FR – Indicates new picture or repeat 0= new field or picture 1= repeated field
►0x70	R/W	[6:5]	*00*****	MPEG MF	MPEG frame indicator – Identifies whether frame is an I, B, or P picture. 00= unknown 01= I picture 10= B picture 11= P picture

4.3.8.3 *Gamut Metadata Packet*

The Gamut Metadata Packet (GMP) contains the sources Gamut Boundary Description. It is defined in the ▹ *HDMI 1.3a* specification.

The contents of the SP InfoFrame are set in the Spare Packet Memory. The device address for the Packet Memory map is programmable and is controlled by register 0xCF of the primary register map. The default setting is 0x70. Transmission of the SP data over the HDMI link is enabled by setting the SP Enable bit (0x40[2] of the Main Register Map) to 1.

The AD9889B transmits the SP data starting 400 pixel clock cycles after the leading edge of Vsync. In order to update the SP at the expected frame, it is recommended that the user set the packet update bit to 0 after the 512th pixel following the Vsync leading edge. The Vsync interrupt of the AD9889B should be used to synchronize this timing. ► Figure 7 illustrates this timing.

Figure 7 I2C Write Timing of SP Data

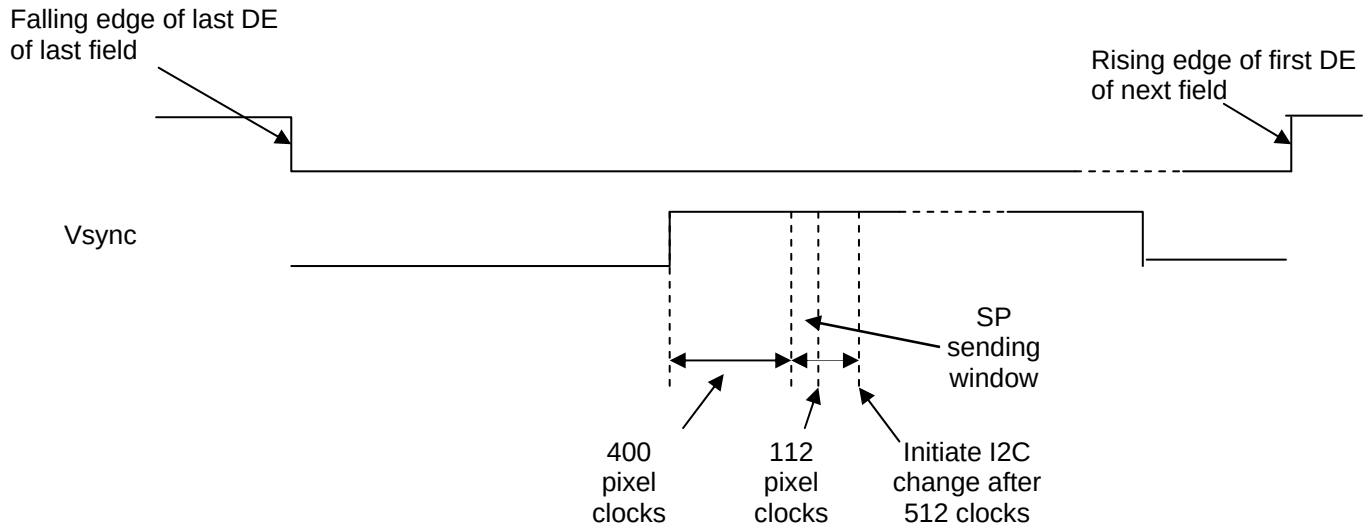


Figure 8 Complete AD9889B Spare Packet Map (device address determined by register 0xCF of main register map)

Address	Type	Bits	Default Value	Register Name	Function
0x00	R/W	[7:0]	00000000	Spare Packet – Header Byte 0 (SP_HB0)	User-defined
0x01	R/W	[7:0]	00000000	SP_HB1	User-defined
0x02	R/W	[7:0]	00000000	SP_HB2	User-defined
0x03	R/W	[7:0]	00000000	Spare Packet - Packet Byte 0 (SP_PB0)	User-defined
0x04	R/W	[7:0]	00000000	SP_PB1	User-defined
0x05	R/W	[7:0]	00000000	SP_PB2	User-defined
0x06	R/W	[7:0]	00000000	SP_PB3	User-defined
0x07	R/W	[7:0]	00000000	SP_PB4	User-defined
0x08	R/W	[7:0]	00000000	SP_PB5	User-defined
0x09	R/W	[7:0]	00000000	SP_PB6	User-defined
0x0A	R/W	[7:0]	00000000	SP_PB7	User-defined
0x0B	R/W	[7:0]	00000000	SP_PB8	User-defined
0x0C	R/W	[7:0]	00000000	SP_PB9	User-defined
0x0D	R/W	[7:0]	00000000	SP_PB10	User-defined
0x0E	R/W	[7:0]	00000000	SP_PB11	User-defined
0x0F	R/W	[7:0]	00000000	SP_PB12	User-defined
0x10	R/W	[7:0]	00000000	SP_PB13	User-defined
0x11	R/W	[7:0]	00000000	SP_PB14	User-defined
0x12	R/W	[7:0]	00000000	SP_PB15	User-defined
0x13	R/W	[7:0]	00000000	SP_PB16	User-defined
0x14	R/W	[7:0]	00000000	SP_PB17	User-defined
0x15	R/W	[7:0]	00000000	SP_PB18	User-defined
0x16	R/W	[7:0]	00000000	SP_PB19	User-defined
0x17	R/W	[7:0]	00000000	SP_PB20	User-defined
0x18	R/W	[7:0]	00000000	SP_PB21	User-defined

Address	Type	Bits	Default Value	Register Name	Function
0x19	R/W	[7:0]	00000000	SP_PB22	User-defined
0x1A	R/W	[7:0]	00000000	SP_PB23	User-defined
0x1B	R/W	[7:0]	00000000	SP_PB24	User-defined
0x1C	R/W	[7:0]	00000000	SP_PB25	User-defined
0x1D	R/W	[7:0]	00000000	SP_PB26	User-defined
0x1E	R/W	[7:0]	00000000	SP_PB27	User-defined

4.3.9 Supported 3D Formats

The AD9889B can support some 3D formats by using the Spare Packet as a VSDB packet. Only side-by-side (half) and top-and-bottom formats for video formats that are supported in 2D can be supported. For details about how to program the VSDB please see section 8.2.3 of the HDMI 1.4a specification.

4.4 Audio Setup

4.4.1 Input Format

AD9889B is capable of receiving audio data in either I2S, or SPDIF for packetization and transmission over the HDMI interface.

Table 42 Audio Input Format Summary

Input				Output		
Audio Select R0x0A[4]	I2S Format R0x0C[1:0]	Data Pin	Clock Pins	Encoding	Format	Packet Type
0	00	I2S	Required: SCLK, LRCLK Optional: MCLK	Normal	Standard I^2S	Audio Sample Packet
0	01	I2S	Required: SCLK, LRCLK Optional: MCLK	Normal	Right Justified	Audio Sample Packet
0	10	I2S	Required: SCLK, LRCLK Optional: MCLK	Normal	Left Justified	Audio Sample Packet
0	11	I2S	Required: SCLK, LRCLK Optional: MCLK	Normal	AES3 Direct	Audio Sample Packet
1	**	SPDIF	Optional: MCLK	Biphase Mark	IEC60958 or IEC61937	Audio Sample Packet

Table 43 Audio Input Format Summary

4.4.1.1 *Inter-IC Sound (I2S) Audio*

The AD9889B can accommodate from two to eight channels of Inter-IC Sound (I2S) audio at up to a 192KHz sampling rate. The number of channels can be selected in register 0x50[7:5]. Which I2S channels are active can be selected in register 0x0C[5:2] If all eight channels (I2S0 – I2S3) are required, setting all bits in registers 0x50[7:5] and 0x0C[5:2] to 1 will select eight channels. If I2S0 only is needed, setting the Channel Count register (0x50[7:5]) and I2S enable (0x0C[2]) to 1 will select this. The I2S Sampling Frequency (0x15[7:4]) must be set appropriately. This value is used along with the VIC to determine pixel repeat (see ► 4.3.4) and sent across the TMDS link in the channel status - information contained in the Audio Sample Packet.

The AD9889B supports standard I2S, left-justified, right-justified, and direct AES3 stream formats via register 0x0C[1:0] and sample word lengths between 16 bits and 24 bits (0x14[3:0]). The AD9889B supports only 64-bit mode, so 64 SCLK edges per channel are required. See ► Figure 11 – Figure 14 for I2S format details.

In the direct AES3 stream I2S format, the user can send an IEC60958 sub-frame, seen in ► Figure 9. The data should be aligned as seen in ► Figure 14, with the Preamble left out as shown in ► Figure 10. Notice that the parity bit is replaced by the block start flag. The information contained in "C" of I2S0 is used in the HDMI audio sample packet. This information can either be extracted from the stream or programmed through the AD9889B register map. To choose the channel status source, use register 0x3B[7].

Figure 9 IEC60958 Sub-Frame

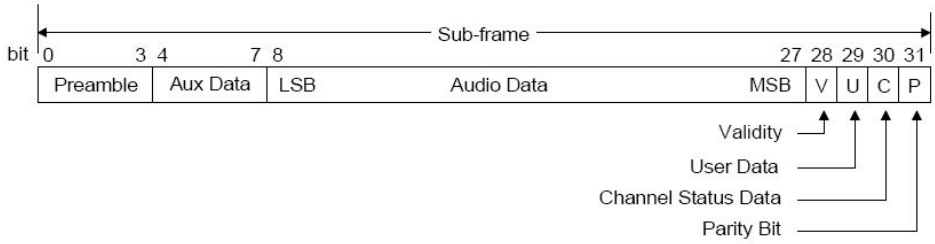


Figure 10 Sub-Frame Format for AD9889B

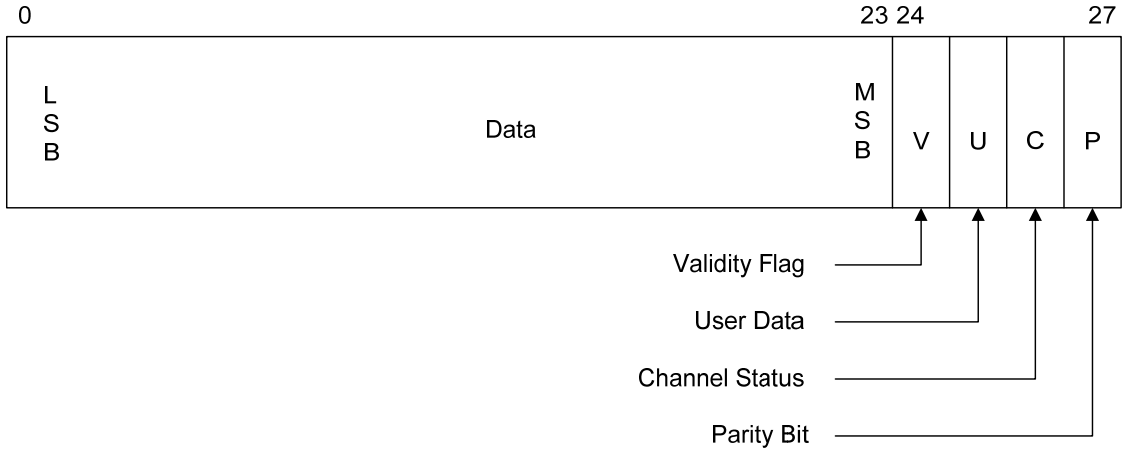


Figure 11 Standard I2S Timing

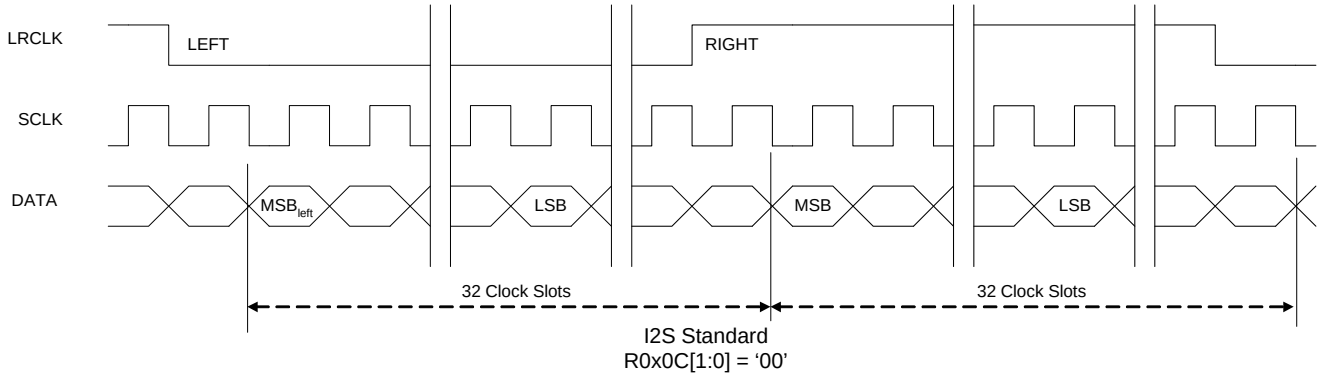
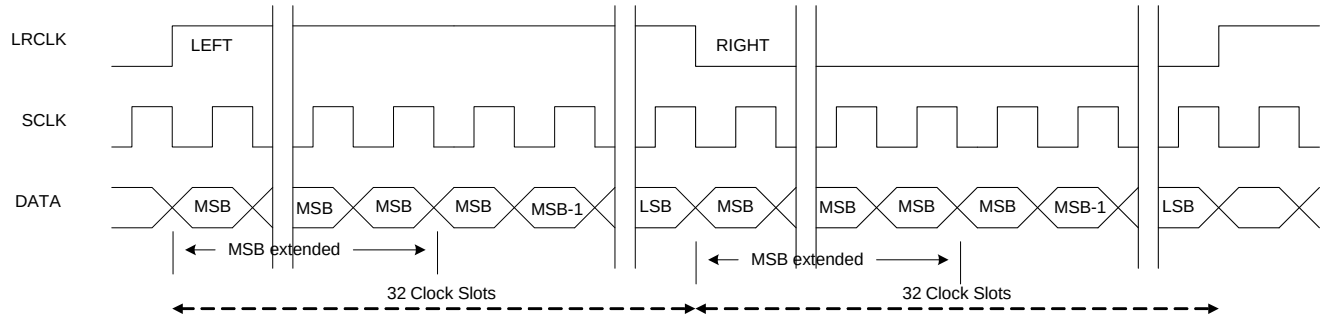
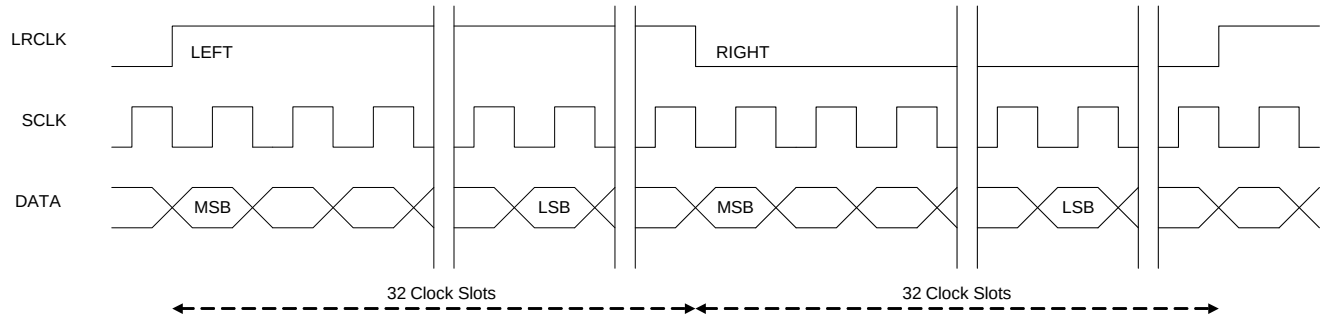


Figure 12 Right-Justified Timing



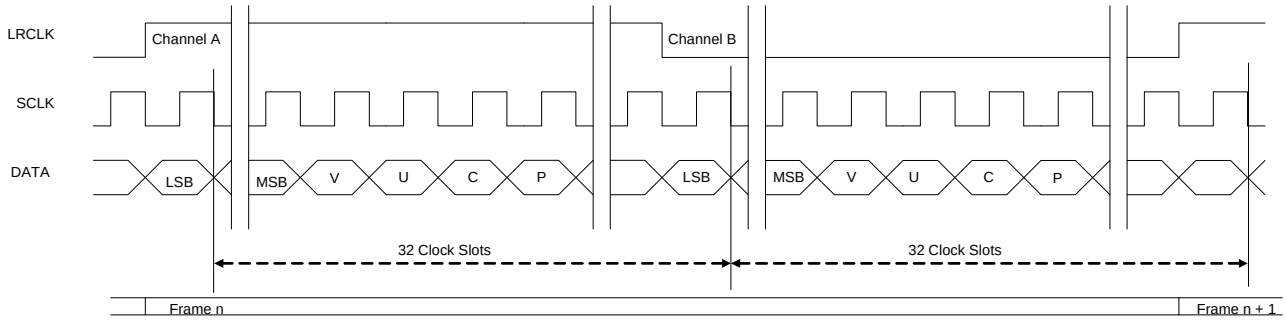
Serial Audio
Right Justified
R0x0C[1:0] = '01'

Figure 13 Left-Justified Timing



Serial Audio
Left Justified
R0x0C[1:0] = '10'

Figure 14 AES3 Direct Timing



AES3 Direct Audio
R0x0C[1:0] = '11'

4.4.1.2 *Sony/Philips Digital Interface (SPDIF) Audio*

The AD9889B is capable of accepting two-channel LPCM and encoded multi-channel audio up to a 192KHz sampling rate via the Sony/Philips Digital Interface (SPDIF). The detected sampling frequency for SPDIF (from 32KHz to 192KHz) can be read in register 0x04[7:4]. For SPDIF, by setting the Audio Frequency Select register (0x0C[7]) to 1, the sampling frequency used to determine pixel repeat can be obtained by the Sampling Frequency register (0x15[7:4]) instead of extracted from the stream; however the sampling frequency read in the SPDIF Sampling Frequency register (0x04) will be sent in the audio sample packet channel status. The AD9889B is capable of accepting SPDIF with or without an MCLK input. When no MCLK is present, the AD9889B uses SCLK to internally generate the MCLK and determine the CTS value.

Table 44 Audio Input Format Related Registers (Main Register Map)

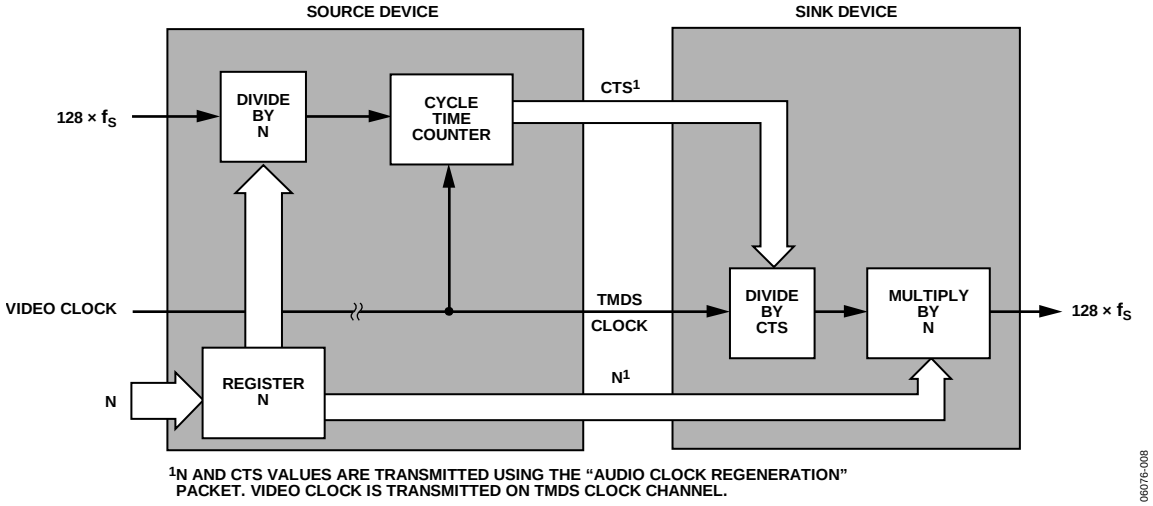
Address	Type	Bits	Default Value	Register Name	Function
▸0x0A	R/W	[4]	***0****	Audio Select	Audio type select. 0 = I2S 1 = SPDIF
		[3]	****0***	MCLK SPDIF	MCLK for SPDIF. 1 = MCLK active 0 = MCLK inactive
		[2]	*****0**	MCLK I2S	MCLK for I2S 1 = MCLK active 0 = MCLK inactive
		[1:0]	******01	MCLK Ratio	MCLK Ratio The ratio between the audio sampling frequency and the clock described using N and CTS 00 = 128xfs 01 = 256xfs 10 = 384xfs 11 = 512xfs
▸0x0B	R/W	[6]	*0******	Audio Clock Polarity	SPDIF MCLK, I2S SCLK, and DSD Clock Polarity Indicates edge where input data is latched 0 = rising edge 1 = falling edge
		[5]	**0*****	Flat Line Audio	Flat Line 0=normal 1=flat line audio –audio sample not valid
▸ 0x0C	R/W	[5:2]	**1*****	I2S 3 enable	I2S Enable for the I2S[3] pin 0 = disable 1 = enable
		[4]	***1****	I2S 2 enable	I2S Enable for the I2S[2] pin 0 = disable 1 = enable
		[3]	****1***	I2S 1 enable	I2S Enable for the I2S[1] pin 0 = disable 1 = enable
		[2]	*****1**	I2S 0 enable	I2S Enable for the I2S[0] pin 0 = disable 1 = enable
		[1:0]	******00	I2S Format	I2S Format 00 = standard I2S mode 01 = right Justified Serial Audio Mode 10 = left Justified Serial Audio Mode 11 = AES3 Direct Stream Mode
▸ 0x0D	R/W	[4:0]	***11000	I2S Bit Width	I2S Bit Width For right justified audio only. Default is 24. Not valid for widths greater than 24.
▸ 0x15	R/W	[7:4]	0000****	Sampling Frequency	Sampling frequency for I2S audio. This information is used both by the audio Rx and the pixel repetition. 0011 = 32kHz 0000 = 44.1kHz 0010 = 48kHz 1000 = 88.2kHz 1001 = 768kHz (for HBR Audio) 1010 = 96kHz 1100 = 176.4kHz 1110 = 192kHz

Address	Type	Bits	Default Value	Register Name	Function
► 0x3B	R/W	[7]	0******	Audio Sampling Frequency Select	Select source of audio sampling frequency for pixel repeat and I2S AES3 Direct Mode 0 = use sampling frequency from I2S stream 1 = use sampling frequency from I2C register
► 0x50	R/W	[7:5]	000*****	CC (Audio InfoFrame)	Channel Count 000 = Refer to Stream Header 001 = 2 channels 010 = 3 channels -- 111 = 8 channels

4.4.2 N and CTS

Audio data carried across the HDMI link, which is driven by a TMDS (video) clock only, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration. There are varieties of clock regeneration methods that can be implemented in an HDMI Sink, each with a different set of performance characteristics. The ▹ HDMI specification does not attempt to define exactly how these mechanisms operate. It does, however, present a possible configuration and define the data items that the HDMI Source shall supply to the HDMI Sink in order to allow the HDMI Sink to adequately regenerate the audio clock. It also defines how that data shall be generated. In many video source devices, the audio and video clocks are generated from a common clock (coherent clocks). In this situation, there exists a rational (integer divided by integer) relationship between these two clocks. The HDMI clock regeneration architecture can take advantage of this rational relationship and can also work in an environment where there is no such relationship between these two clocks; that is, where the two clocks are truly asynchronous or where their relationship is unknown.

Figure 15 Audio Clock Regeneration



The Audio Clock Regeneration model in ► Figure 15 illustrates the overall system architecture model used by HDMI for audio clock regeneration. The Source shall determine the fractional relationship between the video clock and an audio reference clock (128*audio sample rate) and shall pass the numerator and denominator for that fraction to the Sink across the HDMI link. The Sink may then recreate the audio clock from the TMDS clock by using a clock divider and a clock multiplier. The exact relationship between the two clocks will be:

$$128\,f_s = f_{TMDS\_CLK}\,\frac{N}{CTS}$$

The Source shall determine the value of the numerator *N* as specified in Section 7.2.1 of the ▹ HDMI specification. Typically, this value *N* will be used in a clock divider to generate an intermediate clock that is slower than the 128*f_S clock by the factor *N*. The Source will typically determine the value of the denominator Cycle Time Stamp (*CTS*) by counting the number of TMDS clocks in each of the 128*f_S/*N* clocks.

4.4.2.1 *N Parameter*

N shall be an integer number and shall meet the following restriction: *128*f_S/1500Hz ≤*N* ≤128*f_S/300Hz with a recommended optimal value of 128*f_S/1000Hz approximately equals *N* for coherent audio and video clock Sources. ► Table 45 – Table 47 can be used to determine the value of *N*. For non-coherent sources or sources where coherency is not known, the equations above should be used.

4.4.2.2 *CTS Parameter*

CTS shall be an integer number that satisfies the following:

$$CTS_{Average} = \frac{f_{TMDS\_CLK}\,N}{128\,f_s}$$

4.4.2.3 *Recommended N and Expected CTS Values*

The recommended value of *N* for several standard pixel clocks are given in ► Table 45 – Table 47. It is recommended that Sources with non-coherent clocks use the values listed for a pixel clock of "Other."

The AD9889B has two modes for CTS generation: manual mode and automatic mode. In manual mode, the user can program the CTS number directly into the chip (R0x07–R0x09) and select this external mode by setting 0x0A[7] to 1. In automatic mode, the chip computes the CTS based on the actual audio and video rates. This can be selected by setting 0x0A[7] to 0 and the results can be read from 0x04 – 0x06. The manual mode is good for coherent audio and video, where the audio and video clock are generated from the same crystal; thus CTS should be a fixed number. The auto mode is good for incoherent audio -video, where there is no simple integer ratio between the audio and video clock. The 20 bit *N* value can be programmed into the AD9889B in registers 0x01–0x03.

Table 45 Recommended N and Expected CTS Values for 32KHz Audio

	32KHz	
Pixel Clock (MHz)	**N**	**CTS**
25.2 / 1.001	4576	28125
25.2	4096	25200
27	4096	27000
27 * 1.001	4096	27027
54	4096	54000
54 * 1.001	4096	54054
74.25 / 1.001	11648	210937 – 210938*
74.25	4096	74250
148.5 / 1.001	11648	421875
148.5	4096	148500
Other	4096	Measured

Table 46 Recommended N and Expected CTS values for 44.1KHz Audio and Multiples

	44.1KHz		88.2KHz		176.4KHz	
Pixel Clock (MHz)	**N**	**CTS**	**N**	**CTS**	**N**	**CTS**
25.2 / 1.001	7007	31250	14014	31250	28028	31250
25.2	6272	28000	12544	28000	25088	28000
27	6272	30000	12544	30000	25088	30000
27 * 1.001	6272	30030	12544	30030	25088	30030
54	6272	60000	12544	60000	25088	60000
54 * 1.001	6272	60060	12544	60060	25088	60060
74.25 / 1.001	17836	234375	35672	234375	71344	234375
74.25	6272	82500	12544	82500	25088	82500
148.5 / 1.001	8918	234375	17836	234375	35672	234375
148.5	6272	16500	12544	16500	25088	16500
Other	6272	measured	12544	measured	25088	Measured

Table 47 Recommended N and Expected CTS values for 448KHz Audio and Multiples

	48KHz		96KHz		192KHz	
Pixel Clock (MHz)	**N**	**CTS**	**N**	**CTS**	**N**	**CTS**
25.2 / 1.001	6864	28125	13728	28125	27456	28125
25.2	6144	25200	12288	25200	24576	25200
27	6144	27000	12288	27000	24576	27000
27 * 1.001	6144	27027	12288	27027	24576	27027
54	6144	54000	12288	54000	24576	54000
54 * 1.001	6144	54054	12288	54054	24576	54054
74.25 / 1.001	11648	140625	35672	140625	46592	140625
74.25	6144	74250	12288	74250	24576	74250
148.5 / 1.001	5824	140625	17836	140625	23296	140625
148.5	6144	148500	12288	148500	24576	148500
Other	6144	measured	12288	measured	24576	measured

Table 48 N and CTS Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x01	R/W	[3:0]	****0000	N[19:16]	The Upper 4 Bits of N 20 bit 'N' used with CTS to regenerate the audio clock in the receiver.
► 0x02	R/W	[7:0]	00000000	N[15:8]	The Middle Byte of N
► 0x03	R/W	[7:0]	00000000	N[7:0]	The Lower Byte of N
► 0x04	RO	[7:4]	0000****	SPDIF Sampling Frequency	SPDIF Sampling Frequency from SPDIF Channel Status. 0011 = 32kHz 0000 = 44.1kHz 0010 = 48kHz 1000 = 88.2kHz 1010 = 96kHz 1100 = 176.4kHz 1110 = 192kHz
		[3:0]	****0000	CTS Automatic[19:16]	Cycle Time Stamp (CTS) Automatically Generated This 20 bit value is used in the receiver with the 'N' value to regenerate an audio clock. For remaining bits see 0x05 and 0x06.
► 0x05	RO	[7:0]	00000000	CTS Automatic[15:8]	Middle Byte of Automatically Generated CTS
► 0x06	RO	[7:0]	00000000	CTS Automatic[7:0]	Low Byte of Automatically Generated CTS
► 0x07	R/W	[3:0]	****0000	CTS Manual[19:16]	Cycle Time Stamp Manually Entered This 20 bit value is used in the receiver with the 'N' value to regenerate an audio clock. For remaining bits see 0x08 and 0x09.
► 0x08	R/W	[7:0]	00000000	CTS Manual[15:8]	Middle Byte of Manually Entered CTS
► 0x09	R/W	[7:0]	00000000	CTS Manual[7:0]	Low Byte of Manually Entered CTS
►0x0A	R/W	[7]	0*******	CTS Select	CTS Source Select. 0 = Automatic CTS 1 = Manual CTS

4.4.3 Audio Sample Packets

By setting the Chanel Count (CC) register (0x50[7:5]) to greater than three channels, the eight-channel audio packet format will be used. The I2S can be routed to different subpackets using registers 0x0E – 0x11. The Channel Allocation (CA) register (0x51[7:0]) must be set to a speaker mapping that corresponds to the I2S to subpacket routing. Using SPDIF has a default setting of two channels.

The placement of I2S channels into the Audio Sample Packet Subpackets, defined in the ▹ HDMI specification, can be specified in registers 0x0E – 0x11. Default settings place all channels in their respective position (I2S0 left channel in channel 0 left position, I2S3 right channel in channel 3 right position), but this mapping is completely programmable if desired.

The audio packets in HDMI use the channel status format from IEC60958. When using I2S, the information sent in the channel status fields is provided by registers Copyright Bit (0x12[5]), Pre-emphasis (0x12[4:2]), clock accuracy (0x12[1:0]), category code (0x13), source number (0x14[7:4]), word length (0x14[3:0]), bits [1:0] 0x12[7:6], and audio sampling frequency (0x15[7:4]). In SPDIF mode the channel status information is taken from the SPDIF stream.

4.4.3.1 *Details for I2S Channel Status*

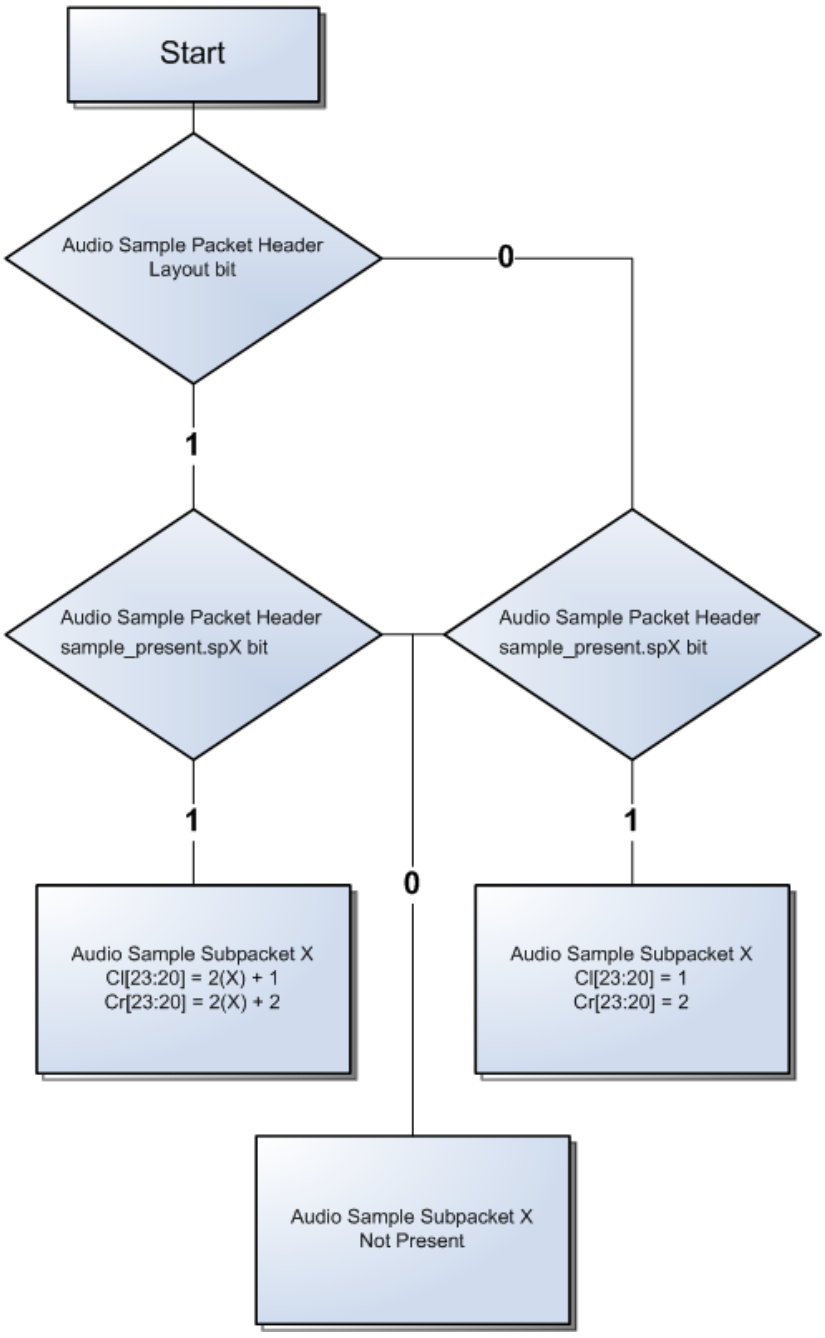
► Table 49 shows the AD9889B register map location or fixed value for each bit in the channel status information sent across the HDMI link. This is applicable for I2S modes 0 – 3 as set in register 0x0C[1:0].

Table 49 I2S Channel Status AD9889B Register Map Location or Fixed Value

Bit	Name	AD9889B Register Used to Set Field or Fixed Value
0	consumer use.	0
1	audio sample word	0
2	copyright	0x12[5]
3	emphasis	0x12[2]
4	emphasis	0x12[3]
5	emphasis	0x12[4]
6	mode	0
7	mode	0
8	category code	0x13[0]
9	category code	0x13[1]
10	category code	0x13[2]
11	category code	0x13[3]
12	category code	0x13[4]
13	category code	0x13[5]
14	category code	0x13[6]
15	category code	0x13[7]
16	source number	0x14[4]
17	source number	0x14[5]
18	source number	0x14[6]
19	source number	0x14[7]
20	channel number	See ▶ Figure 16
21	channel number	See ▶ Figure 16
22	channel number	See ▶ Figure 16
23	channel number	See ▶ Figure 16
24	sampling frequency	0x15[4]
25	sampling frequency	0x15[5]
26	sampling frequency	0x15[6]
27	sampling frequency	0x15[7]
28	clock accuracy	0x12[0]
29	clock accuracy	0x12[1]
30	Not Defined	0
31	Not Defined	0
32	word length	0x14[0]
33	word length	0x14[1]
34	word length	0x14[2]
35	word length	0x14[3]
36	original sampling frequency	0
37	original sampling frequency	0
38	original sampling frequency	0
39	original sampling frequency	0
40	CGMS-A	0
41	CGMS-A	0
42	Not Defined	0
191	Not Defined	0

In ► Figure 16 the layout bit in the Audio Sample Packet Header and the sample_present.spX bit are determined based on the Audio InfoFrame Channel Count register (0x73[2:0]). For example, if Channel Count = 0b001, indicating stereo audio, the layout bit will be zero and all Audio Sample Subpackets will contain information for channel 1 and 2. If Channel Count = 0b011, indicating four channels, the layout bit will be one, and sample_present.sp0 = 1, sample_present.sp1 = 1, sample_present.sp2 = 0, and sample_present.sp2 = 0. ► Figure 16 shows how the channel number bits will be set based on the layout bit and sample_present.spX.

Figure 16 Definition of Channel Status Bits 20 to 23



Address	Type	Bits	Default Value	Register Name	Function
► 0x0E	R/W	[5:3]	**000***	Subpacket 0 L Source	Source of sub packet 0, left channel
		[2:0]	*****001	Subpacket 0 R Source	Source of sub packet 0, right channel
► 0x0F	R/W	[5:3]	**010***	Subpacket 1 L Source	Source of sub packet 1, left channel
		[2:0]	*****011	Subpacket 1 R Source	Source of sub packet 1, right channel
► 0x10	R/W	[5:3]	**100***	Subpacket 2 L Source	Source of sub packet 2, left channel
		[2:0]	*****101	Subpacket 2 R Source	Source of sub packet 2, right channel
► 0x11	R/W	[5:3]	**110***	Subpacket 3 L Source	Source of sub packet 3, left channel
		[2:0]	*****111	Subpacket 3 R Source	Source of sub packet 3, right channel
► 0x12	R/W	[5]	**0*****	CR Bit (Channel Status)	Copy Right Bit 0 = copy right 1 = not copy right protected
		[4:2]	***000**	A_INFO (Channel Status)	Additional information for channel status bits 000 = 2 audio channels w/o pre-emphasis 001 = 2 audio channels with 50/15uS pre-emphasis 010 = Fixed 011 = Fixed Other values reserved in IEC 60958
		[1:0]	******00	CLK_ACC (Channel Status)	Clock Accuracy 00 = level II – normal accuracy +/-1000 X 10-6 10 = level III – variable pitch shifted clock 01 = level I – high accuracy +/-50 X 10-6 11 = fixed
► 0x13	R/W	[7:0]	00000000	Category Code (Channel Status)	Category Code for audio InfoFrame – see IEC 60958
► 0x14	R/W	[7:4]	0000****	Source Number (Channel Status)	source number
		[3:0]	****0000	Word Length	Audio Word Length 0000 not specified 0010 16 bits 1100 17 bits 0100 18 bits 1000 19 bits 1010 20 bits 0001 not specified 0011 20 bits 1101 21 bits 0101 22 bits 1001 23 bits 1011 24 bits Other values reserved in IEC 60958
► 0x15	R/W	[7:4]	0000****	Sampling Frequency	Sampling frequency for I2S audio. This information is used both by the audio Rx and the pixel repetition. 0011 = 32kHz 0000 = 44.1kHz 0010 = 48kHz 1000 = 88.2kHz 1001 = HBR Audio 1010 = 96kHz 1100 = 176.4kHz 1110 = 192kHz Other values reserved in IEC 60958

► 0x50	R/W	[7:5]	000*****	CC (Audio InfoFrame)	Channel Count 000 = Refer to Stream Header 001 = 2 channels 010 = 3 channels -- 111 = 8 channels

4.4.4 Audio InfoFrame

The audio InfoFrame allows the receiver to identify the characteristics of an audio stream before the channel status information is available. The Audio Channel Count register (0x59[7:5]) sets the channel count field for the InfoFrame, and determines the number of channels to send in the audio sample packets. Down Mix Inhibit (0x50[4]), Level Shift Values (0x50[3:0]), and Speaker Mapping (0x51) are defined in the ▹ *CEA-861D* specification. The number of channels in the Channel Count register must match the number of channels in the Speaker Mapping register. The values for the Speaker Mapping bits are included in ► Table 50 for reference.

Table 50 Audio Channel Mapping bits 4-0 (bits 7-5 are not used in CEA 861D)

CA (Speaker Mapping)					Channel Number[2]							
4	3	2	1	0	8	7	6	5	4	3	2	1
0	0	0	0	0					-	-	FR	FL
0	0	0	0	1					-	LFE	FR	FL
0	0	0	1	0					FC	-	FR	FL
0	0	0	1	1					FC	LFE	FR	FL
0	0	1	0	0				RC	-	-	FR	FL
0	0	1	0	1				RC	-	LFE	FR	FL
0	0	1	1	0				RC	FC	-	FR	FL
0	0	1	1	1				RC	FC	LFE	FR	FL
0	1	0	0	0			RR	RL	-	-	FR	FL
0	1	0	0	1			RR	RL	-	LFE	FR	FL
0	1	0	1	0			RR	RL	FC	-	FR	FL
0	1	0	1	1	-	-	RR	RL	FC	LFE	FR	FL
0	1	1	0	0	-	RC	RR	RL	-	-	FR	FL
0	1	1	0	1	-	RC	RR	RL	-	LFE	FR	FL
0	1	1	1	0	-	RC	RR	RL	FC	-	FR	FL
0	1	1	1	1	-	RC	RR	RL	FC	LFE	FR	FL
1	0	0	0	0	RRC	RLC	RR	RL	-	-	FR	FL
1	0	0	0	1	RRC	RLC	RR	RL	-	LFE	FR	FL
1	0	0	1	0	RRC	RLC	RR	RL	FC	-	FR	FL
1	0	0	1	1	RRC	RLC	RR	RL	FC	LFE	FR	FL
1	0	1	0	0	FRC	FLC	-	-	-	-	FR	FL
1	0	1	0	1	FRC	FLC	-	-	-	LFE	FR	FL
1	0	1	1	0	FRC	FLC	-	-	FC	-	FR	FL
1	0	1	1	1	FRC	FLC	-	-	FC	LFE	FR	FL
1	1	0	0	0	FRC	FLC	-	RC	-	-	FR	FL
1	1	0	0	1	FRC	FLC	-	RC	-	LFE	FR	FL
1	1	0	1	0	FRC	FLC	-	RC	FC	-	FR	FL
1	1	0	1	1	FRC	FLC	-	RC	FC	LFE	FR	FL
1	1	1	0	0	FRC	FLC	RR	RL	-	-	FR	FL
1	1	1	0	1	FRC	FLC	RR	RL	-	LFE	FR	FL
1	1	1	1	0	FRC	FLC	RR	RL	FC	-	FR	FL
1	1	1	1	1	FRC	FLC	RR	RL	FC	LFE	FR	FL

[2] FL = Front Left, FC = Front Center, FR = Front Right, FLC = Front Left Center, FRC = Front Right Center, RL = Rear Left, RC = Rear Center, RR = Rear Right, RLC = Rear Left Center, RRC = Rear Right Center, LFE = Low Frequency Effect

Table 51 Audio InfoFrame and Other Packets Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x44	R/W	[3]	****1***	Audio InfoFrame Enable	Audio InfoFrame Enable 0 = disable audio InfoFrame 1 = enable audio InfoFrame
► 0x50	R/W	[7:5]	000*****	CC (Audio InfoFrame)	Channel Count 000 = refer to stream header 001 = 2 channels 010 = 3 channels -- 111 = 8 channels
		[4]	***0****	DM_INH (Audio InfoFrame)	Down-mix Inhibit 0 = permitted or no information about this 1 = prohibited
		[3:0]	****0000	Level Shift (Audio InfoFrame)	LSV[3:0] – Audio Level Shift Values With Attenuation Information 0000 = 0dB attenuation 0001 = 1dB attenuation --- 1111 = 15dB attenuation
► 0x51	R/W	[7:0]	00000000	Speaker Mapping (Audio InfoFrame)	CA[7:0] Speaker mapping or placement for up to 8 channels

4.4.5 Audio Content Protection (ACP) Packet

The Audio Content Protection (ACP) packet is used for transmitting content-related information about the active audio stream. Use of the ACP will be defined in the license agreements of the protected audio stream.

Table 52 ACP Packet Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x40	R/W	[4]	***0****	ACP Packet Enable	ACT Packet Enable 0 = disable 1 = enable
► 0x71	R/W	[7:0]	00000000	Audio Content Protection Packet (ACP) Type	ACP Type 0 = generic audio 1 = IEC 60958-identified audio 2 = DVD audio 3 = Reserved for SACD
► 0x72	R/W	[7:6]	00******	Audio Copy Permission	See CEA861D
		[5:3]	**000***	Audio Copy Number	See CEA861D
		[2:1]	*****00*	Quality	See CEA861D
		[0]	*******0	Transaction	See CEA861D

4.4.6 International Standard Recording Code (ISRC) Packet

If the Supports_AI bit in the Vendor Specific Data Block (VSDB) of the sink EDID is 1 then the International Standard Recording Code (ISRC) packets 1 and 2 can be transmitted. The use of the ISRC fields is described in ▹ "DVD Specifications for Read-Only Disc", Part 4: AUDIO SPECIFICATIONS Version 1.0, March 1999, Annex B.

Table 53 ISRC Packet Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x40	R/W	[3]	****0***	ISRC Packet Enable	ISRC Packet Enable 0 = disable ISRC packet 1 = enable ISRC packet
►0x73	R/W	[7]	0*******	ISRC 1 Continued	International Standard Recording Code (ISRC1) Continued – This indicates an ISRC2 packet is being transmitted 0 = only 1 ISRC packet is needed 1 = the 2nd ISRC packet is needed
		[6]	*0******	ISRC Valid	ISRC Valid 0 = ISRC1Status bits and Packet Bytes not valid 1 = ISRC1 Status bits and Packet Bytes valid
		[5:3]	**000***	ISRC1 Status	ISRC1 Status indicates the beginning, middle, or end of a track 001 = start 010 = middle 100 = end
►0x74	R/W	[7:0]	00000000	ISRC 1 - Packet Byte 0 (ISRC1_PB0)	User-defined
…	…	…	…	…	…
►0x83	R/W	[7:0]	00000000	ISRC1_PB15	User-defined
►0x84	R/W	[7:0]	00000000	ISRC 2 Packet - Packet Byte 0 (ISRC2_PB0)	User-defined
…	…	…	…	…	…
►0x93	R/W	[7:0]	00000000	ISRC2_PB15	User-defined

4.5 EDID Handling

4.5.1 Reading EDID

The AD9889B has an I2C master (DDCSDA and DDCSCL) to read the EDID. It begins buffering segment 0 of the Sink's EDID after HPD is detected and AD9889B is powered up. The system can request additional segments by programming the EDID Segment register (0xC4). An interrupt bit 0x96[2] indicates that a 256-byte EDID read has been completed, and the information is available in the EDID Memory. The EDID Memory is at I2C address 0x7E by default. This is the default address but can be changed by writing the desired address into the EDID Memory Address register (0x43).

4.5.1.1 *EDID Definitions*

Enhanced EDID (E-EDID) supports up to 256 segments. A segment is a 256-byte segment of EDID containing information for either one or two 128-byte EDID blocks. A typical HDMI system will have only two EDID blocks and so will only use segment 0. The first EDID block is always a base EDID structure defined in VESA EDID specifications; the second EDID block is usually the CEA extension defined in the ▹ *CEA-861D Specification*.

EDID and HDCP use a shared memory space. During HDCP repeater initialization, the EDID data is overwritten with HDCP information. EDID is not re-read after HDCP initialization. If the user would like to re-buffer an EDID segment the EDID re-read register described in section should be used.

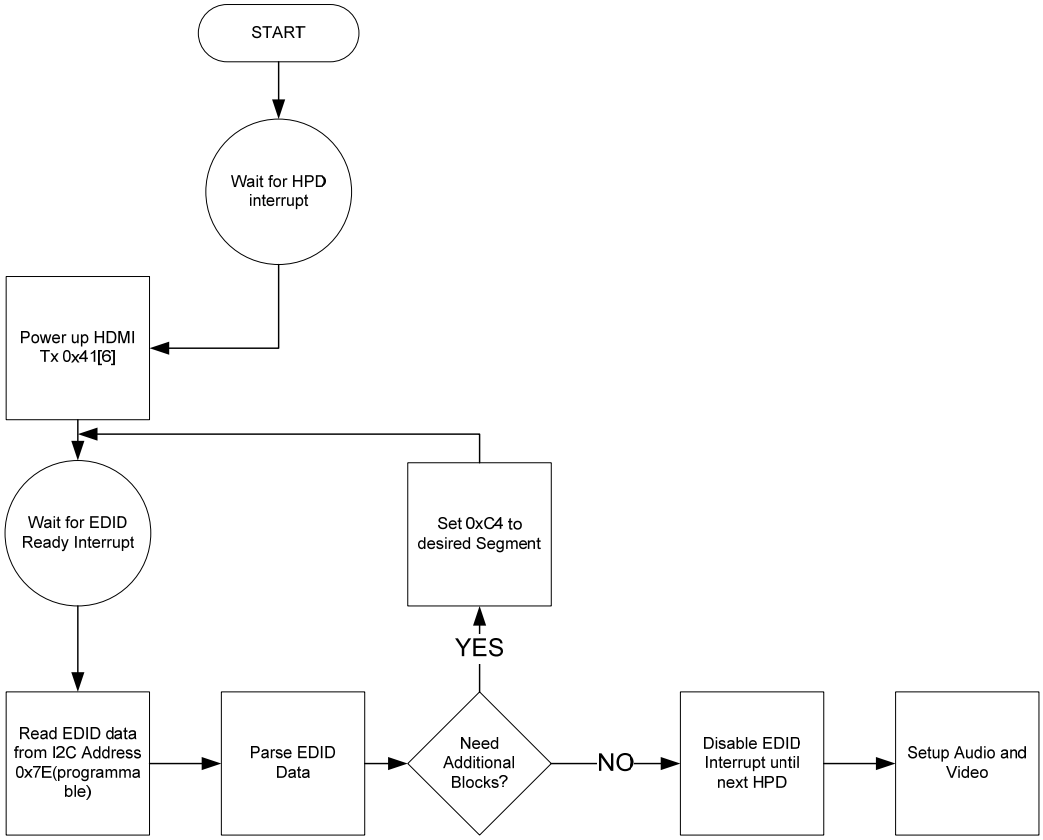
4.5.1.2 *Additional Segments*

EDID block 0 byte number 0x7E tells how many additional EDID blocks are available. If byte 0x7E is greater than 1, additional EDID segments will need to be read. If there is more than one segment, the second block (block 1) is required to be an EDID extension map. This map should be parsed according to the ▹ *VESA EDID* specifications to determine where additional EDID blocks are stored in the receiver's EDID EEPROM.

The AD9889B is capable of accessing any of the up to 256 segments allowed by the ▹ EDID specification. By writing the desired segment number to register 0xC4, the AD9889B will automatically access the correct portion of the EDID EEPROM over the DDC lines and load the 256 bytes into the EDID memory. When the action is complete, an EDID ready interrupt will occur to tell the user. If the host controller needs access to previously requested EDID information, then it can be stored in its own memory.

► Figure 17 shows how to implement software to read EDID from the receiver using the AD9889B.

Figure 17 Reading EDID through the AD9889B



4.5.1.3 ***EDID Tries Register (0xC9 [3:0])***

The EDID Tries register limits the number of times the HDCP/EDID controller will try to read the EDID. Each time an EDID read fails with an I2C "Not Acknowledged" (NACK), this value is decremented. The default start-up value of this register is 3. Once the EDID Tries register is 0, the controller will not attempt to read the EDID until this register is set to something other than 0. This could be used if a sink asserts HPD before the DDC bus is ready resulting in several NACKs as the Tx attempts to read the EDID.

4.5.1.4 *EDID Reread Register (0xC9[4])*

If the EDID data is read in and the host determines that the data needs to be reread, this bit can be set from 0 to 1 for 10 times consecutively, and the current segment will be reread each time. This register should be toggled from 0 to 1 for 10 times consecutively to ensure a successful capture of the register value. This could be useful if the EDID checksum is calculated and determined not to match.

Another method to reread the EDID is to toggle the Main Power Down register bit (0x41[6]) from 0 to 1.

Table 54 EDID-Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x43	R/W	[7:0]	01111110	EDID Memory Address	The I2C address for EDID memory.
► 0x94	R/W	[2]	*****0**	EDID Ready Interrupt Enable	EDID Ready Interrupt Enable.
► 0x96	R/W	[2]	*****0**	EDID Ready Interrupt	Interrupt for EDID Ready.
► 0xC4	R/W	[7:0]	00000000	EDID Segment	Sets the E-DDC segment used by the EDID Fetch routine.
► 0xC9	R/W	[4]	***0****	EDID Reread	Rereads current segment if toggled from 0 to 1 for 10 times consecutively.
		[3:0]	****0011	EDID Tries	Number of times that the EDID read will be attempted if unsuccessful.

4.6 HDCP Handling

4.6.1 For One Sink and No Upstream Devices

The AD9889B has a built-in micro-controller to handle HDCP transmitter states, including handling down-stream HDCP repeaters. To activate HDCP from a system level the main controller needs to set the HDCP Desired register (0xAF[7]) to 1 and the Frame Encryption register (0xAF[4]) to 1. This informs the AD9889B that the video stream should be encrypted. The AD9889B takes control from there, and implements all of the remaining tasks defined by the HDCP 1.4 specification. Before sending audio and video, the BKSVs stored in registers 0xBF – 0xC3 should be compared with the revocation list which is compiled by managing System Renewability Messages (SRMs) provided on the source content (typically a DVD), and the BKSV Ready Interrupt register should be cleared. After the link is established, the system controller should monitor the status of HDCP by reading the HDCP Encrypted register (0xB8[6]) every two seconds. The HDCP Controller Error Interrupt register (0x97[6]) will become active if there is an error relating to the controller. The meaning of the error can be determined by checking the HDCP Controller Error register (0xC8[7:4]).

4.6.2 For Multiple Sinks and No Upstream Devices

When connecting the AD9889B to a repeater, it is necessary to read all BKSV from downstream devices. These BKSVs must be checked against a revocation list, which will be provided on the source content.

The BKSV Count register (0xC7[6:0]) will read 0 when the first BKSV interrupt occurs. After the first BKSV interrupt is cleared, if the device is a repeater, a second BKSV interrupt will occur. The AD9889B will automatically read up to 13 5-byte BKSVs at a time and store these in the EDID memory location (default location I2C address 0x7E). Refer to ► Table 55 for details about the location of the downstream BKSVs. The number of additional BKSVs currently stored in the EDID memory location can be read in register 0xC7[6:0]. If there are more than 13 additional BKSVs to be processed, the AD9889B will collect the next up to 13 BKSVs across the DDC lines, then generate another interrupt when the next set is ready. There can be a maximum of 127 BKSVs total.

The BKVS Flag Interrupt register (0x97[6]) should be cleared by writing a 1 after each set of BKSVs is read. To check when authentication is complete, the system should monitor the HDCP Controller State register (0xC8[3:0]) and wait until this reaches state 4. At this time, the last step is to compare the BKSV list with the revocation list and then send the content.

4.6.3 For Use in a Repeater

The AD9889B can be used in a repeater, which is a device that has one or more HDMI Rx upstream from the AD9889B. To use the AD9889B as a repeater, there are some additional requirements. The system software needs to pass the BKSVs of all downstream devices upstream through the repeater's receiver. In addition, the depth of the device tree and the total number of devices need to be communicated upstream. This depth and device count information can be found in the BSTATUS information, which is supplied in the EDID memory (default location I2C address 0x7E) at an offset of 0xF9 for the LSB's and 0xFA for the MSB's. ► Table 55 shows the meaning of the bits in the BSTATUS bit field.

The BSTATUS information is only available when the BKSVs are in the memory space. This is from the time there is a BKSV ready interrupt with BKSV Count register (0xC7[6:0]) greater than 0 to the time the interrupt flag is cleared. The EDID will not automatically be re-buffered. If the user would like to re-buffer an EDID segment the EDID re-read register described in section should be used.

4.6.4 Software Implementation

► Figure 18 is a block diagram of HDCP software implementation for all cases using the AD9889B HDCP controller state machine. The necessary interactions with the AD9889B registers and EDID memory as well as when these interactions should take place are covered in the block diagram. Note that there is no need to interact with the DDC bus directly, because all of the DDC functionality is controlled by the HDCP controller and follows the ▹ *HDCP specification 1.4*.

4.6.5 AV Mute

AV Mute can be enabled once HDCP authentication is completed. This can be used to maintain HDCP synchronization while changing video resolutions. While the BKSVs for downstream devices are being collected, an active HDCP link capable of sending encrypted video is established, but video should not be sent across the link until the BKSVs have been compared with the revocation list. It is not recommended to rely on AV mute to avoid sending audio and video during HDCP authentication. This is because AV Mute does not actually mute audio or video in the Tx. It requests the function from the Sink device. The best way to avoid sending unauthorized audio and video is to not send data to the AD9889B inputs until authentication is complete. Another option is to use the color space converter to black out the video and disable the audio inputs to mute the audio.

Figure 18 Flow Chart for the HDCP Software Implementation

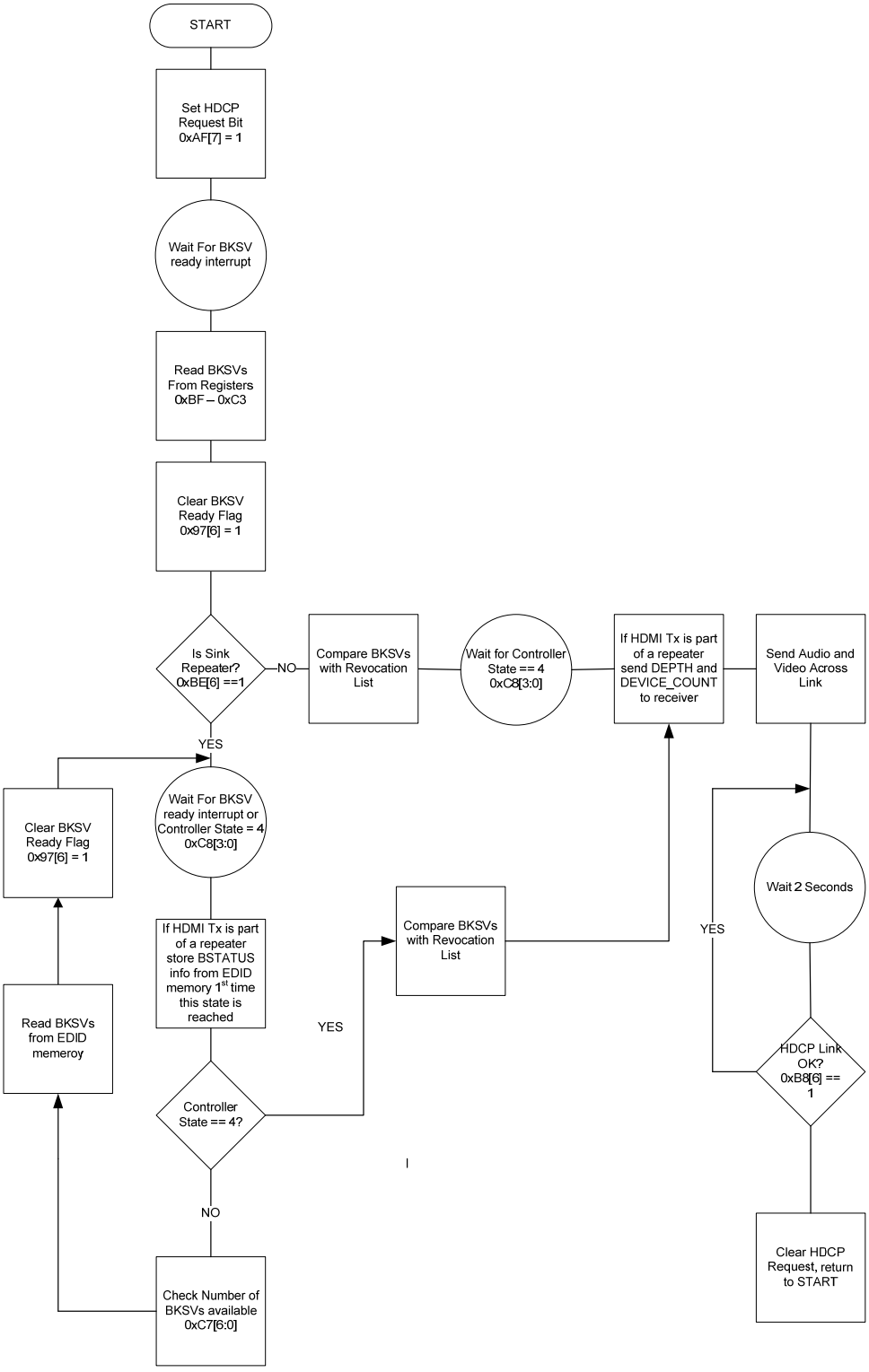


Table 55 HDCP Related Register (EDID Memory)

Address	Type	Bits	Default Value	Register Name	Function
0x00	RO	[7:0]	0000000	BKSV0 – Byte 0	Downstream BKSV
0x01	RO	[7:0]	0000000	BKSV0 – Byte 1	…
0x02	RO	[7:0]	0000000	BKSV0 – Byte 2	…
0x03	RO	[7:0]	0000000	BKSV0 – Byte 3	…
0x04	RO	[7:0]	0000000	BKSV0 – Byte 4	…
0x05	RO	[7:0]	0000000	BKSV1 – Byte 0	…
…	…	…	…	…	…
0x60	RO	[7:0]	0000000	BKSV12 – Byte 0	…
0x61	RO	[7:0]	0000000	BKSV12 – Byte 1	…
0x62	RO	[7:0]	0000000	BKSV12 – Byte 2	…
0x63	RO	[7:0]	0000000	BKSV12 – Byte 3	…
0x64	RO	[7:0]	0000000	BKSV12 – Byte 4	…
0xF9	RO	[7]	0*******	BSTATUS Bit 7	Maximum Downstream Devices Exceeded (MAX_DEVS_EXCEEDED) 0 = Less than or equal to 127 devices 1 = More than 127 devices
		[6:0]	*0000000	BSTATUS Bits 6:0	Device Count (DEVICE_COUNT) Number of Downstream Devices
0xFA	RO	[7:5]	000*****	BSTATUS Bits 15:13	Reserved in HDCP 1.3 Specification
		[4]	***0****	BSTATUS Bit 12	HDMI Mode (HDMI_MODE) 0 = Sink is in DVI mode 1 = Sink is in HDMI mode
		[3]	****0***	BSTATUS Bit 11	Maximum Levels Exceeded (MAX_CASCADE_EXCEEDED) 0 = Less than or equal to 7 levels 1 = More than 7 levels
		[2:0]	*****000	BSTATUS Bits 10:8	Depth (DEPTH) Number of downstream levels

Table 56 HDCP Related Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x43	R/W	[7:0]	01111110	EDID Memory Address	The I2C address for EDID memory.
► 0x95	R/W	[7]	0*******	HDCP Controller Error Interrupt Enable	HDCP Controller Error Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[6]	*0******	BKSV Flag Interrupt Enable	BKSV Flag Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
► 0x97	R/W	[7]	0*******	HDCP Controller Error Interrupt	HDCP Controller Error Interrupt See the HDCP Controller Error register 0xC8[7:4] for the error code 0 = error code not valid 1 = error code valid
		[6]	*0******	BKSV Flag Interrupt	BKSV Flag Interrupt
► 0xAF	R/W	[7]	0*******	Enable HDCP	Enable HDCP 0 = input A/V content not to be encrypted 1 = ihe input A/V content should be encrypted
		[4]	***1****	Frame Encryption	Enable HDCP Frame Encryption 0 = the current frame should not be encrypted 1 = the current frame should be encrypted
► 0xBE	RO	[7]	0*******	HDMI Reserved (Bcaps)	HDMI Reserved 0 = Sink not capable of HDMI 1 = Reserved per HDCP 1.3
		[6]	*0******	Repeater (Bcaps)	HDCP Repeater 0 = HDCP receiver (sink) is not repeater capable 1 = HDCP receiver (sink) is repeater capable
		[5]	**0*****	KSV FIFO Ready (Bsaps)	KSV FIFO Ready 1 = HDCP receiver has compiled list of attached KSVs
		[1]	******0*	HDCP support (Bcaps)	HDCP 1.1 Features Support 0 = HDCP Receiver does not support v. 1.1 features 1 = HDCP Receiver supports 1.1 features such as EESS (Enhanced Encryption Status Signaling)
		[0]	*******0	Fast HDCP (Bcaps)	Fast Authentication 0 = HDCP Receiver not capable of fast authentication. 1 = HDCP Receiver capable of receiving unencrypted video during the session re-authentication.
► 0xB8	RO	[6]	*0******	HDCP Encrypted	HDCP Encryption On 1 = the A/V content is being encrypted. 0 = not encrypted.
		[4]	***0****	Key Reading Error	HDCP Key Reading Error Status 0 = HDCP key reading successful 1 = HDCP key reading error
► 0xBF	RO	[7:0]	00000000	BKSV – Byte 0	BKSV read from Rx by the HDCP controller 40 bits (5 bytes)
► 0xC0	RO	[7:0]	00000000	BKSV – Byte 1	
► 0xC1	RO	[7:0]	00000000	BKSV – Byte 2	
► 0xC2	RO	[7:0]	00000000	BKSV – Byte 3	
► 0xC3	RO	[7:0]	00000000	BKSV – Byte 4	
► 0xC7	R/W	[6:0]	*0000000	BKSV Count	BKSV Count Total number of down-link HDCP devices

Address	Type	Bits	Default Value	Register Name	Function
► 0xC8	RO	[7:4]	0000****	HDCP Controller Error	HDCP Controller Error Error code report when the HDCP Controller Error Interrupt register 0x97[7] = 1
		[3:0]	****0000	HDCP Controller State	HDCP Controller State State of the controller used for HDCP debug purposes

4.7 Power Management

4.7.1 Power-Down Level I

Power-down level I is used when the HDMI Tx should be powered down, but interrupt monitoring is still needed. The AD9889B power-down pin polarity depends on the chip I2C address selection. If the user wants to use 0x72, then the PD/AD pin is active high. If the user wants to use 0x7A, the PD/AD pin is active low. At any time the power-down pin polarity can be verified by reading register 0x42[7]. If SPDIF is not being used, the SPDIF Enable register (0x44[7]) can be set to 0. This will turn off the SPDIF receiver. This is not necessary during main power-down mode as the SPIDF receiver will be already powered down.

▹ See the *AD9889B Hardware User's Guide* for more information about the PD/AD pin and power specifications.

The AD9889B can be powered down or reset either by the power-down pin or by register 0x41[6]. During power-down modes, all the circuits are inactive except the I2C slave and circuits related to mode and activity detection. During power-down mode the chip status can still be read through I2C slave. Anytime after power-down, the user needs to set the power down pin to inactive and set 0x41[6] to 0 to activate the chip. Some registers will also be reset when the chip is put into power down mode. The details are in ► Table 57.

Table 57 Register Reset Control

Address	HPD Pin or Power Down Pin	Power Down Register 0x41[1]
0x00 – 0x93	Reset	Not Reset
0x94 - 0x97 (except 0x96[7:6])	Reset	Reset
0x96[7:6]	Not Reset	Not Reset
0x98 – 0xAE	Not Reset	Not Reset
0xAF-0xCC	Reset	Reset
0xCD -0xCF	Not Reset	Not Reset

4.7.2 Power-Down Level II

Power-down level II is used when an ultra-low power-down is needed. As a tradeoff interrupt handling and Rx Sense monitoring cannot be used. To achieve significantly lower power-down power consumption, the Rx Sense Monitoring and Interrupt Power Down register (0xA1[6]) can be set to 1 while the HDMI Tx is in power down mode. This will disable the Rx Sense detection and interrupts will not be usable. With Rx Sense Power-Down active, the HPD State register (0x42[6]) is still valid. Polling of this register can be used to determine if a Sink is connected.

If the inputs to the AD9889B are toggling while the HDMI Tx is in power down mode, some power will be consumed. It is best to disable toggling of the inputs in Power-Down Level II if possible.

Table 58 Power Management Registers (Main Register Map)

Address	Type	Bits	Default Value	Register Name	Function
► 0x41	R/W	[6]	*1******	Power Down	Main Power Down 0 = all circuits powered up. 1 = power down the whole chip, except I2C, HPD interrupt and Rx Sense interrupt, and CEC.
►0x44	R/W	[7]	0*******	SPDIF Enable	Enable or Disable SPDIF receiver 0 = disable 1 = enable
► 0x42	RO	[7]	1*******	PD/AD Polarity Detection	Polarity Detected for the PD/AD pin 0 = I2C Address 0x7A and Power Down pin is active low 1 = I2C Address 0x72 and Power Down pin is active high
► 0xA1	R/W	[6]	*0******	Rx Sense Power Down	Rx Sense Monitoring and Interrupt Power Down. 0 = Rx Sense monitoring enabled 1 = Rx Sense monitoring disabled

4.8 HDCP/EDID Controller

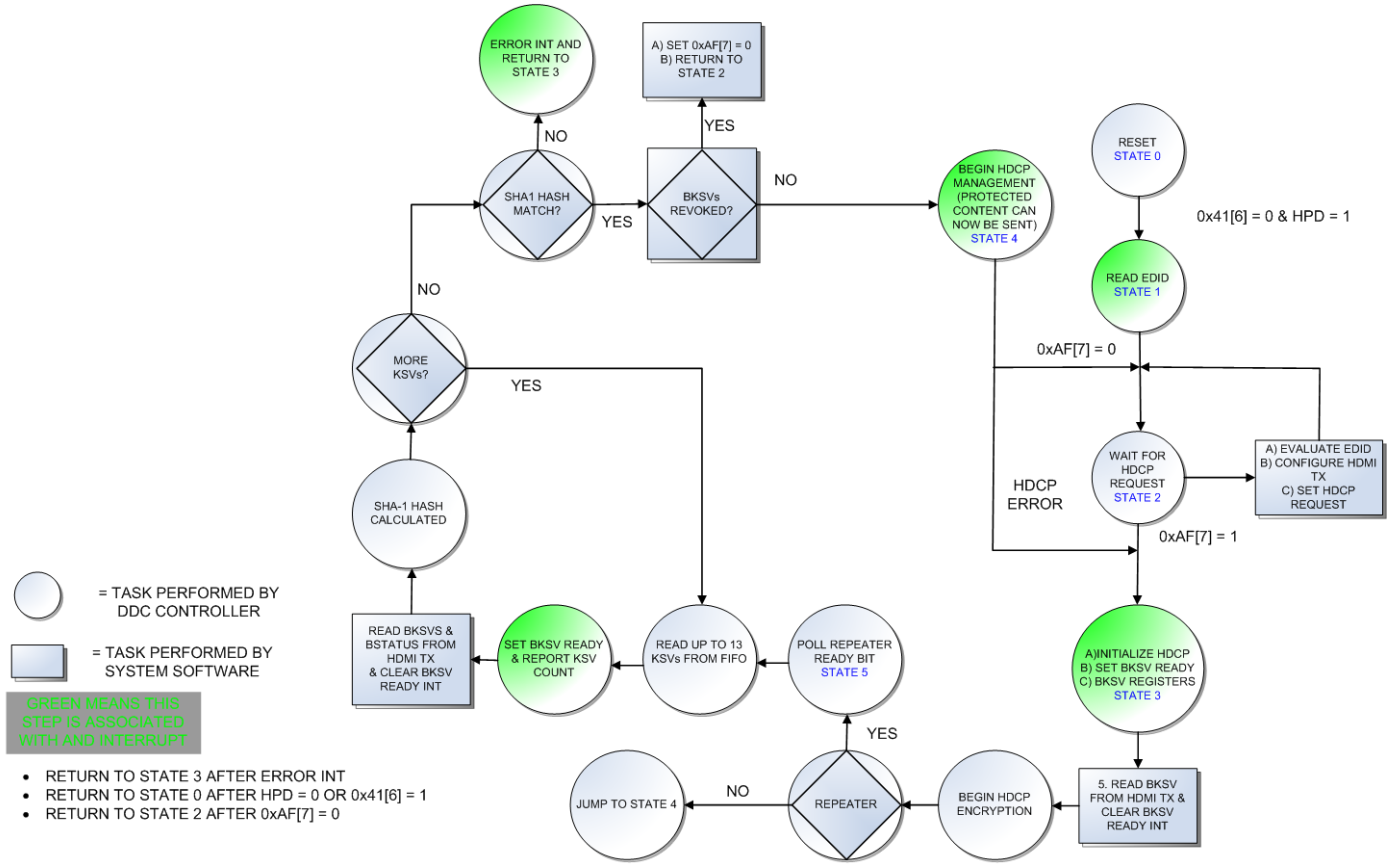
4.8.1 AD9889B EDID/HDCP Support Features

The AD9889B's EDID and HDCP controller performs three main functions to support the system's EDID and HDCP handling. These features are outlined below. A block diagram is illustrated in ► Figure 19.

- Reads EDID segment 0 from the display as soon as Hot Plug is detected and the chip is set to powered up mode.
  - The 256-byte EDID segment is stored in internal RAM and can be read via I2C and has its own I2C address. The I2C slave address of the EDID memory can be programmed in the EDID ID register (0x43). The default value for this register is 0x7E.
  - Reads additional EDID segments on demand.
  - These segments are stored in the same location as the first segment. Therefore, the controller should store the first segment prior to initializing another EDID segment download.
- Implements the HDCP transmitter state machine including handling of downstream repeaters.
- Includes robust error reporting to report various error conditions to the system firmware.

► Figure 19 shows a flow chart of the State Machine implemented by the internal controller. Circles indicate functions that are controlled automatically within the AD9889B, and squares indicate functions that must be implemented in the system software.

Figure 19 AD9889B EDID and HDCP Controller Functional Flow



4.9 Interrupt Handling

The AD9889B has interrupts (INT pin is low active) to help with the system design. The interrupts allow the internal HDCP/EDID controller to alert the system of the events listed in ► Table 59. For Hot Plug Detect and Rx Sense, the interrupt will be triggered for every transition, so the read-only register must be used to determine if the HPD or Rx Sense is logic high or logic low.

Table 59 Interrupt Handling Registers

Interrupt	Interrupt Register	Read Only Register	Mask Register
Hot Plug Detect	0x96[7]	0x42[6]	0x94[7]
Rx Sense	0x96[6]	0xC6[2]	0x94[6]
Active Vsync Edge	0x96[5]	NA	0x94[5]
Audio FIFO full	0x96[4]	NA	0x94[4]
Embedded Sync Parity Error	0x96[3]	NA	0x94[3]
EDID Ready	0x96[2]	NA	0x94[2]
HDCP Error	0x97[7]	NA	0x95[7]
BKSV Flag	0x97[6]	NA	0x95[6]

4.9.1.1 *Hot Plug Detect*

This interrupt is triggered every time there is an HPD transition from high to low or low to high

4.9.1.2 *Rx Sense*

This interrupt is triggered every time the TMDS clock line voltages both cross 1.8V from high to low or low to high.

4.9.1.3 *Active Vsync Edge*

This interrupt is triggered whenever AD9889B detects a Vsync leading edge. This applies to all input types. Vsync edge detection is useful for timing some I2C writes such as enabling CSC and Gamut Metadata Packet information. See the following sections for further information:

- 4.3.8.3 - Gamut Metadata Packet

4.9.1.4 *Audio FIFO Full*

This interrupt is triggered if more data goes into the audio FIFO than comes out. If it happens at initialization period, it is not a problem. If it happens after the system is fully configured, then there is a problem with the system.

4.9.1.5 *Embedded Sync Parity Error*

This interrupt is triggered when the embedded sync parity protection encounters two errors in F/V/H bits of EAV or SAV bits. AD9889B is able to correct a one-bit error and flag a two-bit error.

4.9.1.6 *EDID Ready*

This interrupt is triggered when the EDID has been read from the receiver and is available in the AD9889B EDID memory to be read at I2C address 0x7E (programmable). If the EDID Ready flag does not occur after EDID is expected, an I2C Error on the HDCP Error interrupt will occur if enabled.

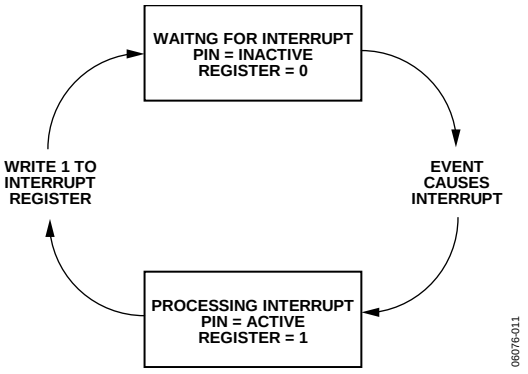
4.9.1.7 *HDCP Error*

This interrupt is triggered when the HDCP/EDID Controller is reporting an error to the system software. The error which occurred is represented by an error code contained in I2C register 0xC8[7:4].

4.9.1.8 *BKSV Flag*

This interrupt is triggered when KSVs from a downstream device are read into the AD9889B. If the BKSV count register (0xC7[6:0]) is zero, then the 5 byte KSV from the receiver directly connected to the AD9889B will be available in registers 0xBF – 0xC3. If the BKSV count register 1 or greater, then the specified amount of 5 byte KSVs from downstream devices will be available in the EDID memory.

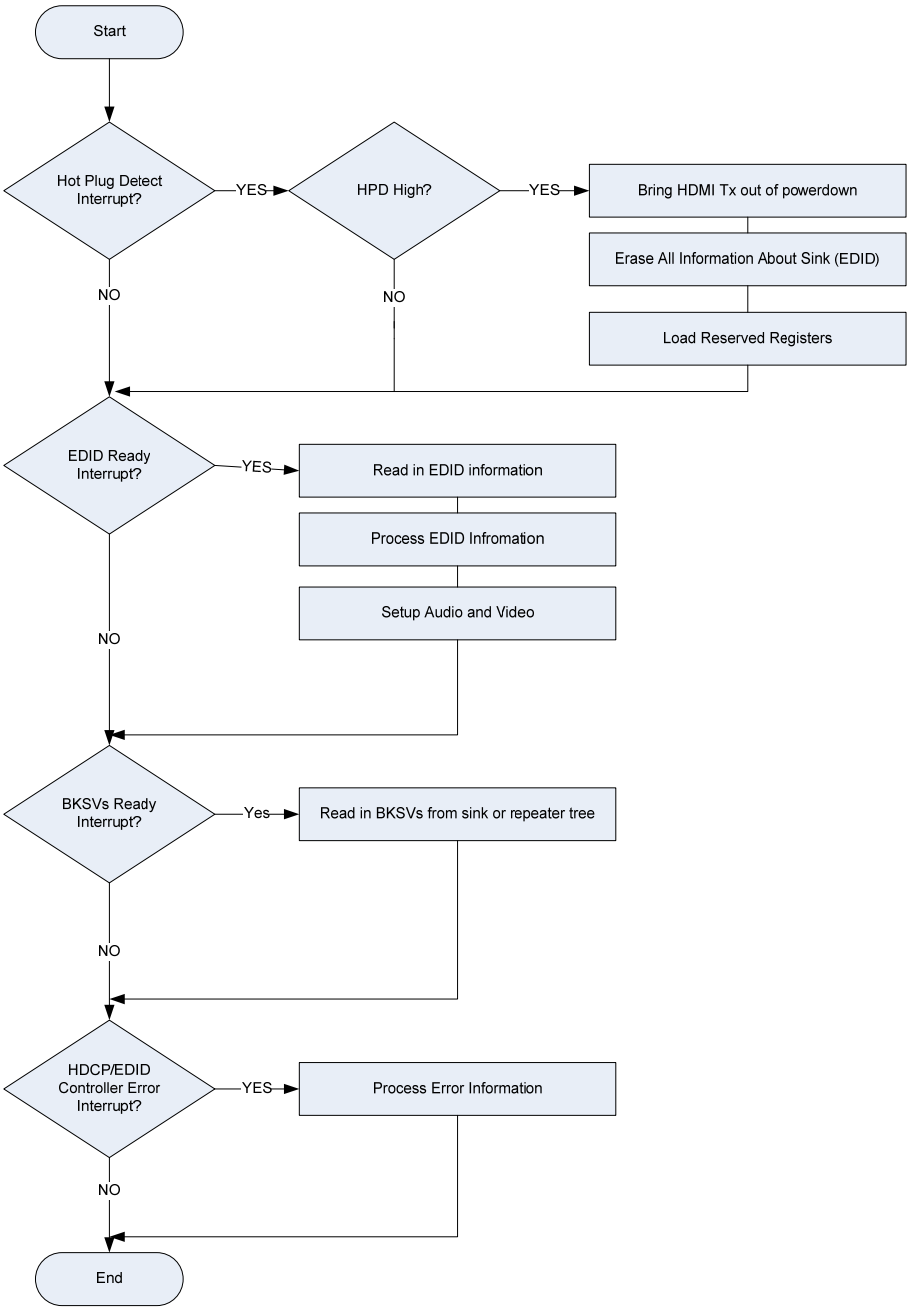
Figure 20 Interrupt Handling



Masks are available to let the user selectively activate each interrupt. To enable a specific interrupt register, write 1 to the corresponding mask bit. The mask bits will not affect the interrupt registers, only the interrupt pin. For some interrupts there are read-only registers available for checking the state.

► Figure 21 shows a recommended flow for processing AD9889B interrupts.

Figure 21 Interrupt Handling Example



SECTION 5: REGISTER MAP

Addresses between 0x00 and 0xFF not included in the register map are not affected by I2C writes and will always read 0. The far right column of the following tables contain a linked reference to the Programming Guide section that provides more detail as to the operation of the particular register being described.

Table 60 Complete Main AD9889B Register Map (Device Address 0x72 or 0x7A)

Address	Type	Bits	Default Value	Register Name	Function	Reference
0x00	RO	[7:0]	00000000	Chip Revision	Revision of the chip	
0x01	R/W	[3:0]	****0000	N[19:16]	The Upper 4 Bits of N 20 bit 'N' used with CTS to regenerate the audio clock in the receiver.	4.4.2
0x02	R/W	[7:0]	00000000	N[15:8]	The Middle Byte of N	4.4.2
0x03	R/W	[7:0]	00000000	N[7:0]	The Lower Byte of N	4.4.2
0x04	RO	[7:4]	0000****	SPDIF Sampling Frequency	SPDIF Sampling Frequency from SPDIF Channel Status. 0011 = 32kHz 0000 = 44.1kHz 0010 = 48kHz 1000 = 88.2kHz 1010 = 96kHz 1100 = 176.4kHz 1110 = 192kHz	4.3.4 4.4.1.1
		[3:0]	****0000	CTS Automatic[19:16]	Cycle Time Stamp (CTS) Automatically Generated This 20 bit value is used in the receiver with the 'N' value to regenerate an audio clock. For remaining bits see 0x05 and 0x06.	4.4.2
0x05	RO	[7:0]	00000000	CTS Automatic[15:8]	Middle Byte of Automatically Generated CTS	4.4.2
0x06	RO	[7:0]	00000000	CTS Automatic[7:0]	Low Byte of Automatically Generated CTS	4.4.2
0x07	R/W	[3:0]	****0000	CTS Manual[19:16]	Cycle Time Stamp Manually Entered This 20 bit value is used in the receiver with the 'N' value to regenerate an audio clock. For remaining bits see 0x08 and 0x09.	4.4.2
0x08	R/W	[7:0]	00000000	CTS Manual[15:8]	Middle Byte of Manually Entered CTS	4.4.2
0x09	R/W	[7:0]	00000000	CTS Manual[7:0]	Low Byte of Manually Entered CTS	4.4.2
0x0A	R/W	[7]	0*******	CTS Select	CTS Source Select. 0 = Automatic CTS 1 = Manual CTS	4.4.2
		[6:5]	*10*****	Reserved	Must be set to 0b00 for proper operation	
		[4]	***0****	Audio Select	Audio type select. 0 = I2S 1 = SPDIF	4.4.1
		[3]	****0***	MCLK SPDIF	MCLK for SPDIF. 1 = MCLK active 0 = MCLK inactive	4.4.1.2
		[2]	*****0**	MCLK I2S	MCLK for I2S 1 = MCLK active 0 = MCLK inactive	4.4.1

Address	Type	Bits	Default Value	Register Name	Function	Reference
		[1:0]	******01	MCLK Ratio	MCLK Ratio The ratio between the audio sampling frequency and the clock described using N and CTS 00 = 128xfs 01 = 256xfs 10 = 384xfs 11 = 512xfs	4.4.1
0x0B	R/W	[6]	*0******	Audio Clock Polarity	SPDIF MCLK, I2S SCLK, and DSD Clock Polarity Indicates edge where input data is latched 0 = rising edge 1 = falling edge	4.4
		[5]	**0*****	Flat Line Audio	Flat Line 0=normal 1=flat line audio –audio sample not valid	4.4
		[4:1]	***0111*	Fixed	Must be default for proper operation	
0x0C	R/W	[5:2]	**1*****	I2S enable	I2S Enable for the I2S[3] pin 0 = disable 1 = enable	4.4.1.1
		[4]	***1****	I2S 2 enable	I2S Enable for the I2S[2] pin 0 = disable 1 = enable	4.4.1.1
		[3]	****1***	I2S 1 enable	I2S Enable for the I2S[1] pin 0 = disable 1 = enable	4.4.1.1
		[2]	*****1**	I2S 0 enable	I2S Enable for the I2S[0] pin 0 = disable 1 = enable	4.4.1.1
		[1:0]	******00	I2S Format	I2S Format 00 = Standard I2S mode 01 = right justified mode 10 = left justified mode 11 = AES3 direct mode	4.4.1.1
0x0D	R/W	[4:0]	***11000	I2S Bit Width	I2S Bit Width For right justified audio only. Default is 24. Not valid for widths greater than 24.	4.4.1.1
0x0E	R/W	[5:3]	**000***	Subpacket 0 L Source	Source of sub packet 0, left channel	4.4.3
		[2:0]	*****001	Subpacket 0 R Source	Source of sub packet 0, right channel	4.4.3
0x0F	R/W	[5:3]	**010***	Subpacket 1 L Source	Source of sub packet 1, left channel	4.4.3
		[2:0]	*****011	Subpacket 1 R Source	Source of sub packet 1, right channel	4.4.3
0x10	R/W	[5:3]	**100***	Subpacket 2 L Source	Source of sub packet 2, left channel	4.4.3
		[2:0]	*****101	Subpacket 2 R Source	Source of sub packet 2, right channel	4.4.3
0x11	R/W	[5:3]	**110***	Subpacket 3 L Source	Source of sub packet 3, left channel	4.4.3
		[2:0]	*****111	Subpacket 3 R Source	Source of sub packet 3, right channel	4.4.3
0x12	R/W	[5]	**0*****	Copyright Bit	Copy Right Bit 0 = copy right 1 = not copy right protected	4.4.3.1
		[4:2]	***000**	Additional Audio Info	Additional information for channel status bits 000 = 2 audio channels w/o pre-emphasis 001 = 2 audio channels with 50/15uS pre-emphasis 010 = Fixed 011 = Fixed Other values reserved in IEC 60958	4.4.3.1

Address	Type	Bits	Default Value	Register Name	Function	Reference
		[1:0]	******00	Audio Clock Accuracy	Clock Accuracy 00 = level II – normal accuracy +/-1000 X 10-6 10 = level III – variable pitch shifted clock 01 = level I – high accuracy +/-50 X 10-6 11 = fixed	4.4.3.1
0x13	R/W	[7:0]	00000000	Category Code	Channel Status Category Code	4.4.3.1
0x14	R/W	[7:4]	0000****	Source Number	Channel Status source number	4.4.3.1
		[3:0]	****0000	Word Length	Audio Word Length 0000 not specified 0010 16 bits 1100 17 bits 0100 18 bits 1000 19 bits 1010 20 bits 0001 not specified 0011 20 bits 1101 21 bits 0101 22 bits 1001 23 bits 1011 24 bits Other values reserved in IEC 60958	4.4.3.1
0x15	R/W	[7:4]	0000****	Sampling Frequency	Sampling frequency for I2S audio. This information is used both by the audio Rx and the pixel repetition. 0011 = 32kHz 0000 = 44.1kHz 0010 = 48kHz 1000 = 88.2kHz 1001 = HBR Audio 1010 = 96kHz 1100 = 176.4kHz 1110 = 192kHz Other values reserved in IEC 60958	4.4.3.1
		[3:0]	****000*	Input ID	Input Video Format. See tables in section ►4.3.2 000 = 24 bit RGB or YCbCr 4:4:4 001 = 16 bit YCbCr 4:2:2 (separate syncs) 010 = 16 bit YCbCr 4:2:2 (embedded syncs) 011 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, separate syncs) 100 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, embedded syncs) 101 = 12 bit RGB 4:4:4 or YCbCr (DDR with separate syncs) 110 = 8,10,12 bit YCbCr 4:2:2 (DDR with separate syncs) 111 = undefined	4.3.1
		[0]	*******0	Low Refresh Rate Video	Video Refresh Rate 0 = Refresh rate above 30Hz 1 = Refresh rate equal or under 30Hz	4.3.4

Address	Type	Bits	Default Value	Register Name	Function	Reference
0x16	R/W	[7:6]	00******	Output Format	Video Output Format In HDMI mode, this should be written along with AVI InfoFrame Y1Y0 (0x55[6:5]). 00 = RGB 4:4:4 01 = YCbCr 4:4:4 11 = YCbCr 4:2:2	4.3.5
		[5:4]	**00****	4:2:2 Width	4:2:2 Width for Input Video Data. See tables in section ▸ 4.3.2 00 = invalid 10 = 12 bit 01 = 10 bit 11 = 8 bit	4.3.2
		[3:2]	****00**	Input Style	Styles refer to the input pin assignments. See tables in section ▸4.3.2 00 = style 1 01 = style 2 10 = style 1 11 = style 3	4.3.1
		[1]	******0*	DDRInput Edge	Video data input edge selection. Defines the first half of pixel data clocking edge. Used for DDR Input ID 5 and 6 only. 0 = falling edge 1 = rising edge	4.3.1
0x17	R/W	[6]	*0******	Vsync Polarity	VSync polarity for Embedded Sync Decoder and Sync Adjustment Case 1: Sync Adjustment Register (0x41[1]) = 1 0 = high polarity 1 = low polarity Case 2: Sync Adjustment Register (0x41[1]) = 0 0 = sync polarity pass through 1 = sync polarity invert	4.3.6.3
		[5]	**0*****	Hsync Polarity	HSync polarity for Embedded Sync Decoder and Sync Adjustment Case 1: Sync Adjustment Register (0x41[1]) = 1 0 = high polarity 1 = low polarity Case 2: Sync Adjustment Register (0x41[1]) = 0 0 = sync polarity pass through 1 = sync polarity invert	4.3.6.3
		[4:3]	***00***	Color Space Converter Mode	CSC scaling factor. Default is YCbCr to RGB for SD video. 00= +/-1.0, -4096 to 4095 01=+/-2.0,-8192 to 8190 10= +/-4.0,-16384 to 16380 11= +/-4.0,-16384 to 16380	4.3.5
		[2]	*****0**	4:2:2 to 4:4:4 Interpolation Style	4:2:2 to 4:4:4 Up Conversion Method 1 = use first order interpolation 0 = use zero order repetetion	
		[1]	******0*	Aspect Ratio	Aspect ratio of input video. 0 = 4:3 1 = 16:9	4.3.3

Address	Type	Bits	Default Value	Register Name	Function	Reference
		[0]	*******0	DE Generator Enable	Enable DE Generator See registers 0x35 – 0x3A 0 = disable 1 = enable	4.3.6.1
0x18	R/W	[4:0]	***00110	A1 MSB (CSC)	Color space Converter (CSC) coefficient for equations: $Out\_A = \left[In\_A\frac{A1}{4096} + In\_B\frac{A2}{4096} + In\_C\frac{A3}{4096} + A4 \right.$ $Out\_B = \left[In\_A\frac{B1}{4096} + In\_B\frac{B2}{4096} + In\_C\frac{B3}{4096} + B4 \right.$ $Out\_C = \left[In\_A\frac{C1}{4096} + In\_B\frac{C2}{4096} + In\_C\frac{C3}{4096} + C4 \right.$	4.3.7
0x19	R/W	[7:0]	01100010	A1 LSB (CSC)		4.3.7
0x1A	R/W	[4:0]	***00100	A2 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x1B	R/W	[7:0]	10101000	A2 LSB (CSC)		4.3.7
0x1C	R/W	[4:0]	***00000	A3 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x1D	R/W	[7:0]	00000000	A3 LSB (CSC)		4.3.7
0x1E	R/W	[4:0]	***11100	A4 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x1F	R/W	[7:0]	10000100	A4 LSB (CSC)		4.3.7
0x20	R/W	[4:0]	***11100	B1 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x21	R/W	[7:0]	10111111	B1 LSB (CSC)		4.3.7
0x22	R/W	[4:0]	***00100	B2 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x23	R/W	[7:0]	10101000	B2 LSB (CSC)		4.3.7
0x24	R/W	[4:0]	***11110	B3 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x25	R/W	[7:0]	01110000	B3 LSB (CSC)		4.3.7
0x26	R/W	[4:0]	***00010	B4 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x27	R/W	[7:0]	00011110	B4 LSB (CSC)		4.3.7
0x28	R/W	[4:0]	***00000	C1 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x29	R/W	[7:0]	00000000	C1 LSB (CSC)		4.3.7
0x2A	R/W	[4:0]	***00100	C2 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x2B	R/W	[7:0]	10101000	C2 LSB (CSC)		4.3.7
0x2C	R/W	[4:0]	***01000	C3 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x2D	R/W	[7:0]	00010010	C3 LSB (CSC)		4.3.7
0x2E	R/W	[4:0]	***11011	C4 MSB (CSC)	See description for registers 0x18 and 0x19	4.3.7
0x2F	R/W	[7:0]	10101100	C4 LSB (CSC)		4.3.7
0x30	R/W	[7:0]	00000000	Hsync Placement MSB (Embedded Sync Decoder)	Upper 8 bits for Embedded Sync Decoder Hsync Placement (In Pixels)	4.3.6.2 4.3.6.3
0x31	R/W	[7:6]	00******	Hsync Placement LSB (Embedded Sync Decoder)	Lower 2 bits for Embedded Sync Decoder Hsync Placement (In Pixels)	4.3.6.2 4.3.6.3
		[5:0]	**000000	Hsync Duration MSB (Embedded Sync Decoder)	Upper 6 bit for Embedded Sync Decoder Hsync Duration (In Pixels)	4.3.6.2 4.3.6.3
0x32	R/W	[7:4]	0000****	Hsync Duration LSB (Embedded Sync Decoder)	Lower 4 bits for Embedded Sync Decoder Hsync Duration (In Pixels)	4.3.6.2 4.3.6.3
		[3:0]	****0000	Vsync Placement MSB (Embedded Sync Decoder)	Upper 4 bits for Embedded Sync Decoder Vsync Placement (In Hsyncs)	4.3.6.2 4.3.6.3
0x33	R/W	[7:2]	000000**	Vsync Placement LSB (Embedded Sync Decoder)	Lower 6 bits for Embedded Sync Decoder Vsync Placement (In Hsyncs)	4.3.6.2 4.3.6.3

Address	Type	Bits	Default Value	Register Name	Function	Reference
		[1:0]	******00	Vsync Duration MSB (Embedded Sync Decoder)	Upper 2 bit for Embedded Sync Decoder Vsync Duration (In Hsyncs)	4.3.6.2 4.3.6.3
0x34	R/W	[7:0]	00000000	Vsync Duration LSB (Embedded Sync Decoder)	Lower 8 bits for Embedded Sync Decoder Vsync Duration (In Hsyncs)	4.3.6.2 4.3.6.3
0x35	R/W	[7:0]	00000000	Hsync Delay MSB (DE Generator)	Upper 8 bits for DE Generation Hsync Delay (In Pixels)	4.3.6.1
0x36	R/W	[7:6]	00******	Hsync Delay LSB (DE Generator)	Lower 2 bits for DE Generation Hsync Delay (In Pixels)	4.3.6.1
		[5:0]	**000000	Vsync Delay (DE Generator)	Vsync Delay for DE Generation. (In Hsyncs)	4.3.6.1
0x37	R/W	[7:5]	000*****	Interlace Offset (DE Generator)	Interlace Offset For DE Generation Sets the difference (in hsyncs) in field length between field 0 and field 1	4.3.6.1
		[4:0]	***00000	Active Width MSB (DE Generator)	Upper 5 bits for DE Generation Active Width (In Pixels)	4.3.6.1
0x38	R/W	[7:1]	0000000*	Active Width LSB (DE Generator)	Lower 7 bits for DE Generation Active Width (In Pixels)	4.3.6.1
0x39	R/W	[7:0]	00000000	Active Height MSB (DE Generator)	Upper 8 bits for DE Generation Active Height (In Lines)	4.3.6.1
0x3A	R/W	[7:4]	0000****	Active Height LSB (DE Generator)	Lower 4 bits for DE Generation Active Height (In Lines)	4.3.6.1
0x3B	R/W	[7]	1******	Audio Sampling Frequency Select	Select source of audio sampling frequency for pixel repeat and I2S AES3 Direct Mode 0 = use sampling frequency from I2S stream 1 = use sampling frequency from I2C register	4.4.3
		[6:5]	*00*****	PR Mode	Pixel Repetition Mode Selection. Set to b00 unless non standard video is supported. 00 = auto mode 01 = max mode 10 = manual mode. See 0x3B bits [4:3][3] 11 = manual mode[1]	4.3.3 4.3.4
		[4:3]	***00***	PR PLL Manual	The clock multiplication of the input clock used in pixel repetition. 00 = x1 01 = x2 10 = x4 11 = x4	4.3.3 4.3.4
		[2:1]	*****00*	PR Value Manual	User programmed pixel repetition number to send to Rx. 00 = x1 01 = x2 10 = x4 11 = x4	4.3.3 4.3.4
		[0]	*******0	Color Space Converter Enable	Color Space Converter Enable 0= Color space converter disabled 1= Color space converter enabled	
0x3C	R/W	[5:0]	**000000	VIC Manual	User programmed VIC to sent to Rx (value defined in CEA861D)	4.3.3 4.3.4

[3] 0b10 and 0b11 are the same

Address	Type	Bits	Default Value	Register Name	Function	Reference
0x3D	RO	[7:6]	00******	Pixel Repeat to Rx	The actual pixel repetition sent to Rx 00 = 1x 01 = 2x 10 = 4x 11 = 4x	4.3.3 4.3.4
		[5:0]	**000000	VIC to Rx	VIC sent to HDMI Rx and Used in the AVI InfoFrame Status (Value Defined in CEA861D)	4.3.3 4.3.4
0x3E	RO	[7:2]	000000**	VIC Detected	Input VIC Detected (value defined in CEA861D)	4.3.3 4.3.4
0x3F	RO	[7:5]	000*****	Auxiliary VIC Detected	This register is for video input formats that are not inside the 861D table. 000 = see 0x3E for video input information 001 = 240p Not Active 010 = 576i Not Active 011 = 288p Not Active 100 = 480i Active 101 = 240p Active 110 = 576i Active 111 = 288p Active	4.3.3 4.3.4
		[4:3]	***00***	Progressive Mode Information	Information about 240p and 288p modes. Case 1: 240p 01 = 262 lines 10 = 263 lines Case 2: 288p 01 = 312 lines 10 = 313 lines 11 = 314 lines	4.3.3 4.3.4
0x40	R/W	[7]	0*******	GC Packet Enable	General Control Packet Enable 0 = disable 1 = enable	4.2.3
		[6]	*0******	SPD Packet Enable	Source Product Descriptor Packet Enable 0 = disable 1 = enable	4.2.5
		[5]	**0*****	MPEG Packet Enable	MPEG Packet Enable 0 = disable MPEG packet 1 = enable MPEG packet	4.3.8.2
		[4]	***0****	ACP Packet Enable	ACP Packet Enable 0 = disable ACP packet 1 = enable ACP packet	4.4.5
		[3]	****0***	ISRC Packet Enable	ISRC Packet Enable 0 = disable ISRC packet 1 = enable ISRC packet	4.4.6
0x41	R/W	[6]	*1******	Power Down	Main Power Down 0 = all circuits powered up 1 = power down the whole chip, except I2C, HPD interrupt and Rx Sense interrupt	4.2.1 4.7
		[5:2]	**0100**	Fixed	Must be default for proper operation	
		[1]	******0*	Sync Adjustment Enable	Sync Adjustment Enable See register 0x30 – 0x34 and 0x17[6:5] 0 = sync adjustment disabled 1 = sync adjustment enabled	4.3.6.3
		[0]	*******0	Fixed	Must be default for proper operation	

Address	Type	Bits	Default Value	Register Name	Function	Reference
0x42	RO	[7]	1*******	PD/AD Polarity Detection	Polarity Detected for the PD/AD Pin 0 = I2C address 0x7A and power down pin is active low 1 = I2C address 0x72 and power down pin is active high	4.2.1 4.2.1 4.7
		[6]	*0******	HPD State	State of the hot plug detection 0 = Hot Plug Detect inactive (low) 1 = Hot Plug active (high)	4.2.1
		[5]	**0*****	Rx Sense State	State of the Rx Sense. 0 = HDMI clock termination not detected 1 = HDMI clock termination detected	4.2.1
		[4]	***0****	Fixed		
0x43	R/W	[7:0]	01111110	EDID Memory Address	The I2C address for EDID memory.	4.1
0x44	R/W	[7]	0*******	SPDIF Enable	Enable or disable SPDIF receiver 0= disable 1= enable	4.4.1.2 4.7
		[6]	*1******	N CTS Packet Enable	0 = disableN_CTS packet. 1 = enable N_CTS packet.	4.4.2
		[5]	**1*****	Audio Sample Packet Enable	0 = disable audio sample packet. 1 = enable audio sample packet.	4.4.3
		[4]	***1****	AVI InfoFrame Enable	AVI InfoFrame Packet Enable 0 = disable AVI InfoFrame packet 1 = enable AVI InfoFrame packet	4.3.8.1
		[3]	****1***	Audio InfoFrame Enable	Audio InfoFrame Enable 0 = disable audio InfoFrame 1 = enable audio InfoFrame	4.4.4
		[2]	*****0**	Fixed	Must be default for proper operation	
		[1]	******0*	Spare Packet Enable	Spare Packet Enable 0= disable Spare Packet 1= enable Spare Packet	4.3.8.3
		[0]	*******0	Fixed	Must be default for proper operation	
0x45	R/W	[7]	0*******	Clear AV Mute	Clear Audio Video Mute 0 = clear 1 = set clear av mute.	4.2.3
		[6]	*0******	Set AV Mute	Set Audio Video Mute 0 = clear 1 = set av mute.	4.2.3
		[5:4]	**00****	Y1Y0 (AVI InfoFrame)	Output format - this should be written when 0x16[7] is written. 00 = RGB 01 = YCbCr 422 10 = YCbCr 444 11 = reserved	4.3.8.1
		[3]	****0***	Active Format Information Status (AVI InfoFrame)	Active Format Information Present 0 = no data 1 = Active format Information valid	4.3.8.1
		[2:1]	*****00*	Bar Information (AVI InfoFrame)	B[1:0] 00 = invalid bar 01 = vertical 10 = horizontal 11 = Both	4.3.8.1

Address	Type	Bits	Default Value	Register Name	Function	Reference
0x46	R/W	[7:6]	00******	Scan Information (AVI InfoFrame)	S[1:0] 00 = no data 01 = TV 10 = PC 11 =None	4.3.8.1
		[5:4]	**00****	Colorimetry (AVI InfoFrame)	C[1:0] 00 = no data 01 = ITU601 10 = ITU709 11 = Extended Colorimetry Information Valid (Indicated in register 0x57[6:4])	4.3.8.1
		[3:2]	****00**	Picture Aspect Ratio (AVI InfoFrame)	M[1:0] 00 = no data 01 = 4:3 10 = 16:9 11 = None	4.3.8.1
		[1:0]	******00	Non-uniform Picture Scaling (AVI InfoFrame)	SC[1:0] 00 = unknown 01 = scaling in Horizontal direction 10 = scaling in Vertical direction 11 = scaling in Both H and V directions	4.3.8.1
0x47	R/W	[7:4]	0000****	Active Format Aspect Ratio (AVI InfoFrame)	R[3:0] 1000 = Same as aspect ratio 1001 = 4:3 (center) 1010 = 16:9 (center) 1011 = 14:9 (center)	4.3.8.1
0x48	R/W	[7:0]	00000000	Active Line Start LSB (AVI InfoFrame)	Active Line Start This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar.	4.3.8.1 CEA861D
0x49	R/W	[7:0]	00000000	Active Line Start MSB (AVI InfoFrame)		4.3.8.1 CEA861D
0x4A	R/W	[7:0]	00000000	Active Line End LSB (AVI InfoFrame)	Active Line End This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar.	4.3.8.1 CEA861D
0x4B	R/W	[7:0]	00000000	Active Line End MSB (AVI InfoFrame)		4.3.8.1 CEA861D
0x4C	RO	[7:0]	00000000	Active Pixel Start LSB (AVI InfoFrame)	Active Pixel Start This represents the last pixel in a vertical pillar-bar at the left side of the picture. If 0, there is no left bar.	4.3.8.1 CEA861D
0x4D	R/W	[7:0]	00000000	Active Pixel Start MSB (AVI InfoFrame)		4.3.8.1 CEA861D
0x4E	R/W	[7:0]	00000000	Active Pixel End LSB (AVI InfoFrame)	Active Pixel End This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar.	4.3.8.1 CEA861D
0x4F	R/W	[7:0]	00000000	Active Pixel End MSB (AVI InfoFrame)		4.3.8.1 CEA861D
0x50	R/W	[7:6]	000*****	CC (Audio InfoFrame)	Channel Count 000 = Refer to Stream Header 001 = 2 channels 010 = 3 channels -- 111 = 8 channels	4.4.4 CEA861D
		[5]	***0****	DM_INH (Audio InfoFrame)	Down-mix Inhibit 0 = permitted or no information about this 1 = prohibited	4.4.4 CEA861D

Address	Type	Bits	Default Value	Register Name	Function	Reference
		[4:0]	****0000	Level Shift (Audio InfoFrame)	LSV[3:0] – Audio Level Shift Values With Attenuation Information 0000 = 0dB attenuation 0001 = 1dB attenuation --- 1111 = 15dB attenuation	4.4.4 CEA861D
0x51	R/W	[7:0]	00000000	Speaker Mapping (Audio InfoFrame)	CA[7:0] Speaker mapping or placement for up to 8 channels	4.4.4 CEA861D
0x52	R/W	[7:0]	00000000	SPD_DB1	Vendor name character 1 (VN1)	4.2.5
0x53	R/W	[7:0]	00000000	SPD_DB2	VN2	4.2.5
0x54	R/W	[7:0]	00000000	SPD_DB3	VN3	4.2.5
0x55	R/W	[7:0]	00000000	SPD_DB4	VN4	4.2.5
0x56	R/W	[7:0]	00000000	SPD_DB5	VN5	4.2.5
0x57	R/W	[7:0]	00000000	SPD_DB6	VN6	4.2.5
0x58	R/W	[7:0]	00000000	SPD_DB7	VN7	4.2.5
0x59	R/W	[7:0]	00000000	SPD_DB8	VN8	4.2.5
0x5A	R/W	[7:0]	00000000	SPD_DB9	Product description character 1 (PD1)	4.2.5
0x5B	R/W	[7:0]	00000000	SPD_DB10	PD2	4.2.5
0x5C	R/W	[7:0]	00000000	SPD_DB11	PD3	4.2.5
0x5D	R/W	[7:0]	00000000	SPD_DB12	PD4	4.2.5
0x5E	R/W	[7:0]	00000000	SPD_DB13	PD5	4.2.5
0x5F	R/W	[7:0]	00000000	SPD_DB14	PD6	4.2.5
0x60	R/W	[7:0]	00000000	SPD_DB15	PD7	4.2.5
0x61	R/W	[7:0]	00000000	SPD_DB16	PD8	4.2.5
0x62	R/W	[7:0]	00000000	SPD_DB17	PD9	4.2.5
0x63	R/W	[7:0]	00000000	SPD_DB18	PD10	4.2.5
0x64	R/W	[7:0]	00000000	SPD_DB19	PD11	4.2.5
0x65	R/W	[7:0]	00000000	SPD_DB20	PD12	4.2.5
0x66	R/W	[7:0]	00000000	SPD_DB21	PD13	4.2.5
0x67	R/W	[7:0]	00000000	SPD_DB22	PD14	4.2.5
0x68	R/W	[7:0]	00000000	SPD_DB23	PD15	4.2.5
0x69	R/W	[7:0]	00000000	SPD_DB24	PD16	4.2.5
0x6A	R/W	[7:0]	00000000	SPD_DB25	Vendor name character 1 (VN1)	4.2.5
0x6B	R/W	[7:0]	00000000	MPEG_DB1	Lower byte of MPEG bit rate: Hz	4.3.8.1 CEA861D
0x6C	R/W	[7:0]	00000000	MPEG_DB2	Lower middle byte of MPEG bit rate: Hz	4.3.8.1 CEA861D
0x6D	R/W	[7:0]	00000000	MPEG_DB3	Upper middle byte of MPEG bit rate: Hz	4.3.8.1 CEA861D
0x6E	R/W	[7:0]	00000000	MPEG_DB4	Upper byte of MPEG bit rate: Hz	4.3.8.1 CEA861D
0x6F	R/W	[7]	0*******	MPEG FR	FR – Indicates new picture or repeat 0= new field or picture 1= repeated field	4.3.8.2 CEA861D
0x70	R/W	[6:5]	*00*****	MPEG MF	MPEG frame indicator – Identifies whether frame is an I, B, or P picture. 00= unknown 01= I picture 10= B picture 11= P picture	4.3.8.2

Address	Type	Bits	Default Value	Register Name	Function	Reference
0x71	R/W	[7:0]	00000000	Audio Content Protection Packet (ACP) Type	ACP Type 0 = generic audio 1 = IEC 60958-identified audio 2 = DVD audio 3 = Reserved for SACD	4.4.5
0x72	R/W	[7:6]	00******	Audio Copy Permission	See CEA861D	4.4.5
		[5:3]	**000***	Audio Copy Number	See CEA861D	4.4.5
		[2:1]	*****00*	Quality	See CEA861D	4.4.5
		[0]	*******0	Transaction	See CEA861D	4.4.5
0x73	R/W	[7]	0*******	ISRC 1 Continued	International Standard Recording Code (ISRC1) Continued – This indicates an ISRC2 packet is being transmitted 0 = only 1 ISRC packet is needed 1 = the 2nd ISRC packet is needed	4.4.4 CEA861D
		[6]	*0******	ISRC Valid	ISRC Valid 0 = ISRC1Status bits and Packet Bytes not valid 1 = ISRC1 Status bits and Packet Bytes valid	4.4.4 CEA861D
		[5:3]	**000***	ISRC1 Status	ISRC1 Status indicates the beginning, middle, or end of a track 001 = start 010 = middle 100 = end	4.4.4 CEA861D
0x74	R/W	[7:0]	00000000	ISRC 1 - Packet Byte 0 (ISRC1_PB0)	User-defined	4.4.6
0x75	R/W	[7:0]	00000000	ISRC1_PB1	User-defined	4.4.6
0x76	R/W	[7:0]	00000000	ISRC1_PB2	User-defined	4.4.6
0x77	R/W	[7:0]	00000000	ISRC1_PB3	User-defined	4.4.6
0x78	R/W	[7:0]	00000000	ISRC1_PB4	User-defined	4.4.6
0x79	R/W	[7:0]	00000000	ISRC1_PB5	User-defined	4.4.6
0x7A	R/W	[7:0]	00000000	ISRC1_PB6	User-defined	4.4.6
0x7B	R/W	[7:0]	00000000	ISRC1_PB7	User-defined	4.4.6
0x7C	R/W	[7:0]	00000000	ISRC1_PB8	User-defined	4.4.6
0x7D	R/W	[7:0]	00000000	ISRC1_PB9	User-defined	4.4.6
0x7E	R/W	[7:0]	00000000	ISRC1_PB10	User-defined	4.4.6
0x7F	R/W	[7:0]	00000000	ISRC1_PB11	User-defined	4.4.6
0x80	R/W	[7:0]	00000000	ISRC1_PB12	User-defined	4.4.6
0x81	R/W	[7:0]	00000000	ISRC1_PB13	User-defined	4.4.6
0x82	R/W	[7:0]	00000000	ISRC1_PB14	User-defined	4.4.6
0x83	R/W	[7:0]	00000000	ISRC1_PB15	User-defined	4.4.6
0x84	R/W	[7:0]	00000000	ISRC 2 Packet - Packet Byte 0 (ISRC2_PB0)	User-defined	4.4.6
0x85	R/W	[7:0]	00000000	ISRC2_PB1	User-defined	4.4.6
0x86	R/W	[7:0]	00000000	ISRC2_PB2	User-defined	4.4.6
0x87	R/W	[7:0]	00000000	ISRC2_PB3	User-defined	4.4.6
0x88	R/W	[7:0]	00000000	ISRC2_PB4	User-defined	4.4.6
0x89	R/W	[7:0]	00000000	ISRC2_PB5	User-defined	4.4.6
0x8A	R/W	[7:0]	00000000	ISRC2_PB6	User-defined	4.4.6
0x8B	R/W	[7:0]	00000000	ISRC2_PB7	User-defined	4.4.6
0x8C	R/W	[7:0]	00000000	ISRC2_PB8	User-defined	4.4.6

Address	Type	Bits	Default Value	Register Name	Function	Reference
0x8D	R/W	[7:0]	00000000	ISRC2_PB9	User-defined	4.4.6
0x8E	R/W	[7:0]	00000000	ISRC2_PB10	User-defined	4.4.6
0x8F	R/W	[7:0]	00000000	ISRC2_PB11	User-defined	4.4.6
0x90	R/W	[7:0]	00000000	ISRC2_PB12	User-defined	4.4.6
0x91	R/W	[7:0]	00000000	ISRC2_PB13	User-defined	4.4.6
0x92	R/W	[7:0]	00000000	ISRC2_PB14	User-defined	4.4.6
0x93	R/W	[7:0]	00000000	ISRC2_PB15	User-defined	4.4.6

Address	Type	Bits	Default Value	Register Name	Function	Reference
0x94	R/W	[7]	1*******	HPD Interrupt Enable	HPD Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled	4.2.1 4.8
		[6]	*1******	Rx Sense Interrupt Enable	Rx Sense Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled	4.2.1 4.8
		[5]	**0*****	Vsync Interrupt Enable	Vsync Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled	4.8 4.9
		[4]	***0****	Audio FIFO Full Interrupt Enable	Audio FIFO Full Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled	4.8 4.9
		[3]	****0***	Embedded Sync Parity Error Interrupt Enable	Embedded Sync Parity Error Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled	4.8 4.9
		[2]	*****0**	EDID Ready Interrupt Enable	EDID Ready Interrupt Enable 1 = interrupt enabled 0 = interrupt disabled	4.8
		[1:0]	******00	Fixed	Must be default for proper operation	4.8
0x95	R/W	[7]	0*******	HDCP Controller Error Interrupt Enable	HDCP Controller Error Interrupt Enable 1 = Interrupt Enabled 0 = Interrupt Disabled	4.8
		[6]	*0******	BKSV Flag Interrupt Enable	BKSV Flag Interrupt Enable 1 = Interrupt Enabled 0 = Interrupt Disabled	
0x96	R/W	[7]	0*******	HPD Interrupt	Interrupt for Hot Plug Detect (HPD) 1 = Interrupt Active 0 = Interrupt Not Active	4.2.1 4.8
		[6]	*0******	Rx Sense Interrupt	Interrupt for monitor connection (Rx Sense) 1 = Interrupt Active 0 = Interrupt Not Active	4.2.1 4.8
		[5]	**0*****	Vsync Interrupt	Interrupt for active VS edge 1 = Interrupt Active 0 = Interrupt Not Active	4.8
		[4]	***0****	Audio FIFO Full Interrupt	Interrupt for audio FIFO overflow 1 = Interrupt Active 0 = Interrupt Not Active	4.8
		[3]	****0***	Embedded Sync Parity Error Interrupt	Interrupt for Embedded Sync Parity Error (1st error corrected 2nd error flagged) 1 = Interrupt Active 0 = Interrupt Not Active	4.8
		[2]	*****0**	EDID Ready Interrupt	Interrupt for EDID Ready 1 = Interrupt Active 0 = Interrupt Not Active	4.5 4.8
		[1]	******0*	HDCP Authenticated	HDCP controller has transitioned to state 4 1 = Interrupt Active 0 = Interrupt Not Active	4.6 4.8
		[1:0]	******00	Fixed	Must be default for proper operation	
0x97	R/W	[7]	0*******	HDCP Controller Error Interrupt	HDCP Controller Error Interrupt See the HDCP Controller Error register 0xC8[7:4] for the error code 0 = error code not valid 1 = error code valid	4.6 4.8

Address	Type	Bits	Default Value	Register Name	Function	Reference
		[6]	*0******	BKSV Flag Interrupt	Interrupt occurs when BKSVs are ready 1 = Interrupt Active 0 = Interrupt Not Active	4.6 4.8
0x98	R/W	[7:0]	00001011	Fixed	Must be written as 0x07 for proper operation	4.2.7
0x99	R/W	[7:0]	00000010	Fixed	Must be default for proper operation	
0x9A	R/W	[7:1]	0000000*	Fixed	Must be default for proper operation	
0x9B	R/W	[5:0]	**011000	Fixed	Must be default for proper operation	
0x9C	R/W	[7:0]	01011010	Fixed	Must be written as 0x38 for proper operation	4.2.7
0x9D	R/W	[7:3]	01100***	Fixed	Must be default for proper operation	
		[2]	*****0**	CLK Divide	Input Video CLK Divide 0 = input clock is not divided 1 = input clock is divided by 2 (if 0xA4[6] = 1)	
		[1:0]	******00	Fixed	Must be written to 0b01 for proper operation	4.2.7
0x9E	RO	[4]	***0****	PLL Lock Status	PLL Lock Status 0 = PLL not locked 1 = PLL locked	4.2.6
		[3:0]	****0000	Fixed		
0x9F	R/W	[7:0]	00000000	Fixed	Must be default for proper operation	
0xA0	RO	[7:0]	00000000	Fixed		
0xA1	R/W	[7]	0*******	Fixed	Must be default for proper operation	
		[6]	*0******	Rx Sense Power Down	Rx Sense Monitoring and Level II Power Down 0 = Rx Sense monitoring enabled 1 = Rx Sense monitoring disabled	4.2.1 4.7.2
		[5]	**0*****	Channel 0 Power Down	Channel 0 Power Down 0 = power up 1 = power down	4.2.4
		[4]	***0****	Channel 1 Power Down	Channel 1 Power Down 0 = power up 1 = power down	4.2.4
		[3]	****0***	Channel 2 Power Down	Channel 2 Power Down 0 = power up 1 = power down	4.2.4
		[2]	*****0**	Clock Driver Power Down	Clock Driver Power Down 0 = power up 1 = power down	4.2.4
0xA2	R/W	[7:0]	10000000	Differential Data Output Drive Strength	Must be written as 0x87 for high speed operation (pixel clock > 80MHz) Can be 0x84 for lower power consumption (up to 80MHz)	4.2.7
0xA3	R/W	[7:0]	10000000	Differential Clock Output Drive Strength	Must be written as 0x87 for high speed operation (pixel clock > 80MHz) Can be 0x84 for lower power consumption (up to 80MHz)	4.2.7
0xA4	R/W	[7]	0*******	Fixed	Must be default for proper operation	
		[6]	*0******	CLK Divide Reset	Input Video CLK Divide Reset 0 = clock disabled if 0x9D[2] ≠ 0 1 = clock divider set by 0x9D[2]	4.3.2.1
		[5:1]	**00100*	Fixed	Must be default for proper operation	
0xA5	R/W	[7:1]	00000100	Fixed	Must be default for proper operation	
0xA6	R/W	[7:0]	00000000	Fixed	Must be default for proper operation	
0xA7	R/W	[7:0]	00000000	Fixed	Must be default for proper operation	
0xA8	R/W	[7:0]	00000000	Fixed	Must be default for proper operation	

Address	Type	Bits	Default Value	Register Name	Function	Reference
0xA9	R/W	[7:1]	00000000	Fixed	Must be default for proper operation	
0xAA	R/W	[7:0]	00000000	Fixed	Must be default for proper operation	
0xAB	R/W	[7:4]	01000000	Fixed	Must be default for proper operation	
0xAC	RO	[7:0]	00000000	Fixed		
0xAD	RO	[7:0]	00000000	Fixed		
0xAE	RO	[7:5]	01000000	Fixed		
0xAF	R/W	[7]	0*******	HDCP Desired	Enable HDCP 0 = input A/V content not to be encrypted 1 = ihe input A/V content should be encrypted	4.6
		[6:5]	*00*****	Fixed	Must be default for proper operation	
		[4]	***1****	Frame Encryption	Enable HDCP Frame Encryption 0 = the current frame should not be encrypted 1 = the current frame should be encrypted	4.6
		[3:2]	****01**	Fixed	Must be default for proper operation	
		[1]	******0*	HDMI/DVI Select	HDMI Mode 0 = DVI 1 = HDMI	4.2.2
		[0]	*******0	Fixed	Must be default for proper operation	
0xB0	RO	[7:0]	00000000	Fixed		
0xB1	RO	[7:0]	00000000	Fixed		
0xB2	RO	[7:0]	00000000	Fixed		
0xB3	RO	[7:0]	00000000	Fixed		
0xB4	RO	[7:0]	00000000	Fixed		
0xB5	RO	[7:0]	00000000	Fixed		
0xB6	RO	[7:0]	00000000	Fixed		
0xB7	RO	[7:0]	00000000	Fixed		
0xB8	RO	[7]	0******	Fixed		
		[6]	*0******	HDCP Encryption	HDCP Encryption On 1 = the A/V content is being encrypted. 0 = not encrypted.	4.6
		[5]	**0*****	Fixed		
		[4]	***0****	Key Reading Error	HDCP Key Reading Error Status 0 = HDCP key reading successful 1 = HDCP key reading error	4.2.6 4.6
0xB9	R/W	[7:0]	0000 0000	Fixed	Must be default for proper operation	
0xBA	R/W	[7:5]	000*****	Clock Delay	Delay Adjust for the Input Video CLK Capture Should be set to 0b011 if no delay is desired 000 = -1200ps 001 = -800ps 010 = -400ps 011 = no delay 100 = 400ps 101 = 800ps 110 = 1200ps 111 = invert	4.3.2.1
		[4]	***0****	AD9389B/AD9889B Selection	AD9389B/AD9889B Selection 0 = AD9889B 1 = AD9389B	
		[3:0]	****0000	Fixed	Must be default for proper operation	
0xBB	R/W	[7:0]	00000000	Fixed	Must be written as 0xFF for proper operation	
0xBC	RO	[7:0]	00000000	Fixed		
0xBD	RO	[7:0]	00000000	Fixed		

Address	Type	Bits	Default Value	Register Name	Function	Reference
0xBE	RO	[7]	0*******	HDMI Reserved (Bcaps)	HDMI Reserved 0 = Sink not capable of HDMI 1 = Reserved per HDCP 1.3	
		[6]	*0******	Repeater (Bcaps)	HDCP Repeater 0 = HDCP receiver (sink) is not repeater capable 1 = HDCP receiver (sink) is repeater capable	4.6
		[5]	**0*****	KSV FIFO Ready (Bsaps)	KSV FIFO Ready 1 = HDCP receiver has compiled list of attached KSVs	4.6
		[4:2]	***000**	BCAPS [4:2]	HDCP BCAPS	4.6
		[1]	******0*	HDCP support (Bcaps)	HDCP 1.1 Features Support 0 = HDCP Receiver does not support v. 1.1 features 1 = HDCP Receiver supports 1.1 features such as EESS (Enhanced Encryption Status Signaling)	4.6
		[0]	*******0	Fast HDCP (Bcaps)	Fast Authentication 0 = HDCP Receiver not capable of fast authentication. 1 = HDCP Receiver capable of receiving unencrypted video during the session re-authentication.	4.6
0xBF	RO	[7:0]	00000000	BKSV1	BKSV read from Rx by the HDCP controller 40 bits (5 bytes)	4.6
0xC0	RO	[7:0]	00000000	BKSV2		4.6
0xC1	RO	[7:0]	00000000	BKSV3		4.6
0xC2	RO	[7:0]	00000000	BKSV4		4.6
0xC3	RO	[7:0]	00000000	BKSV5		4.6
0xC4	R/W	[7:0]	00000000	EDID Segment	Sets the E-DDC segment used by the EDID Fetch routine.	4.5
0xC5	R/W	[7]	0*******	Fixed	Do not write to this register	
	RO	[6:0]	*0000000	Fixed		
0xC6	RO	[7:0]	00000000	Fixed		
0xC7	R/W	[7]	0*******	Fixed	Do not write to this register	
	RO	[6:0]	*0000000	BKSV Count	BKSV Count Total number of down-link HDCP devices	4.6
0xC8	RO	[7:4]	0000****	HDCP Controller Error	HDCP Controller Error Error code report when the HDCP Controller Error Interrupt register 0x97[7] = 1	4.6
		[3:0]	****0000	HDCP Controller State	HDCP Controller State State of the controller used for HDCP debug purposes	4.6
0xC9	R/W	[3:0]	****0011	EDID Tries	Number of times that the EDID read will be attempted if unsuccessful.	4.5
0xCD	R/W	[7]	0*******	AVI_PB1[7] (AVI InfoFrame)	Reserved bit from AVI PB1	4.3.8.1
		[6]	*0******	ITC (AVI InfoFrame)	IT Content 0 = no IT content 1 = IT content is present	4.3.8.1
		[5:3]	**000***	EC[2:0] (AVI InfoFrame)	Extended Colorimetry 000 = $xvYCC_{601}$ 001 = $xvYCC_{709}$ See latest HDMI specification for other values	4.3.8.1
0xCE	R/W	[7:0]	0000****	AVI_PB5[7:4] (AVI InfoFrame)	Reserved bits from AVI PB5	4.3.8.1

Address	Type	Bits	Default Value	Register Name	Function	Reference
0xCF	R/W	[7:0]	0111000	Spare Packet Memory Address	I2C Address for the Spare Packet memory	4.1

SECTION 6: GLOSSARY

BKSV	HDCP Key Selection Vector for Device B.
CSC	Colorspace Convert is used to convert RGB to YCrCb or YCrCb to RGB. Adjustments can be factored in for differing ranges.
CTS	Cycle Time Stamp used in Audio Clock Recovery.
DDC	Display Data Channel is used to communicate between to the source and sink to determine sink capabilities. It is also used as the HDCP key communications channel.
DDR	Double Data Rate clocks capture data on both the rising and falling edge of the clock.
EDID	Enhanced Display Identification is used to store monitor (sink) capabilities in an EEPROM.
GCP	HDMI General Control Packet.
HDCP	High Definition Content Protection is a method of protecting content from unauthorized digital copying.
HDMI	High Definition Multimedia Interface is composed of three TMDS differential data channels and one differential clock channel. It is defined to include video streams up to 3.7Gbps as well as audio.
I2C	Inter-IC Communications is a Philips two-wire serial bus for low-speed (up to 400kHz) data.
I2S	Inter-IC Sound is a serial Philips bus designed specifically for audio.
LPCM	Linear Pulse-Code Modulation is a method of encoding audio samples.
LQFP	Low-Profile Quad Flat Pack is the type of package in which the AD9889B is supplied.
RGB	Red Green Blue is the standard definition for three-color graphics and video.
RO	Read only.
SPDIF	Sony/Philips Digital Interface.
TMDS	Transition Minimized Differential Signaling is the format used by the three data channels in HDMI. This encodes 8 bits into 10 and serializes them.
VIC	Video Identification Code as defined in ▹ *CEA 861*.
x.v.Color	This is feature of HDMI v.1.3 in which the color gamut may be extended or altered beyond the normal range in order to accommodate a given sink.
YCrCb	This is a common color format for video where the 'Y' component is luminance and the Cr and Cb signals are color difference signals. 4:4:4 defines a Y, Cr, and Cb for each pixel; 4:2:2 defines a Y for each pixel and a sharing of Cr and Cb between 2 sequential pixels. In this manner, compression of 33% is possible.