AD9889B

Low-Power HDMI 1.2 Compliant Transmitter

HARDWARE

USER'S GUIDE

- Revision B -
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Advantiv
Advanced Television Solutions
by Analog Devices

ANALOG DEVICES

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SECTION 1: INTRODUCTION

1.1 Scope and Organization

This document is intended to help the hardware designer understand what is necessary to design for the AD9889B and maintain the highest levels of performance. The *AD9889B Hardware User's Guide* (HUG) provides guidelines to design the schematics and board layout. Included are sections on the 3 package options and an overview of the functional blocks (including a brief description for each block) to provide an understanding of the AD9889B functional and performance capabilities. The *AD9889B Programming Guide(PG)* is available as a separate document and should be used to gain a complete understanding on how to configure the AD9889B within a system application

It is divided into the following sections:

Section 2: **Reference Documents** is a list of other references, which will be helpful when designing with the AD9889B HDMI Transmitter.

Section 3: **Block Diagram** gives an overall functional view of the HDMI transmitter.

Section 4: **Specifications** give all pertinent data such as: timing, power and testing.

Section 5:**Pin and Package Information** give the mechanical details of the interface.

Section 6:**Functional Description** serves to elaborate on input, output and internal operations.

Section 7: **PCB Layout Recommendations** are an aid to low noise operation.

1.1.1 Symbols

Symbols are used to indicate internal and external document references as follows:

- ► Indicates a linked reference to another section of this document.
- ▹ Indicates a reference to another document, either an ADI document or an external specification.

1.1.2 Format Standards

In this document, ADI has chosen to represent data in the following ways:

0xNN Hexadecimal (base-16) numbers are represented using the "C" language notation, preceded by 0x.

0bNN Binary (base-2) numbers are represented using "C" language notation, preceded by 0b.

NN Decimal (base-10) numbers are represented using no additional prefixes or suffixes.

Bit Bits are numbered in little-endian format; i.e., the least-significant bit of a byte or word is referred to as bit 0.

1.2 Overview

The AD9889B is a low-power, high-speed High-Definition Multimedia Interface (HDMI) transmitter that is capable of supporting an input data rate up to 165MHz (1080p). Careful hardware design (schematics and PCB layout) is recommended to optimize the performance and to ensure HDMI compliance.

The *AD9889B Programming Guide* and *AD9889B Software Driver User Guide* are also available if required.

1.3 Hardware Features

- Operation up to 165MHz (TMDS link frequency)
- Interrupt (INT) output pin eliminates constant I2C monitoring
- Supports I2S and SPDIF audio input formats
- No audio Master Clock (MCLK) required for I2S and SPDIF
- Requires 1.8V supply
- EDID buffered on chip
- Color Space Converter (CSC)
- 3 package options
  - 64-lead LFCSP
  - 80-lead LQFP
  - 76-ball CSPBGA
- 0°C to +85°C temperature range

1.4 Supported Input Formats

- 24 bit RGB 4:4:4 (separate syncs)
- 24 bit YCbCr 4:4:4 (separate syncs)
- 24, 20, or 16 bit YCbCr 4:2:2 (embedded or separate syncs)
- 12, 10, or 8 bit YCbCr 4:2:2 (2x pixel clock with embedded or separate syncs)
- 12, 10, or 8 bit YCbCr 4:2:2 (DDR with embedded or separate syncs)
- 12 bit RGB 4:4:4 (DDR with separate syncs)
- 12 bit YCbCr 4:4:4 (DDR with separate syncs)

1.5 Supported Output Formats

- 24 bit RGB 4:4:4
- 24 bit YCbCr 4:4:4
- 24 bit YCbCr 4:2:2

SECTION 2: REFERENCE DOCUMENTS

2.1 ADI Documents

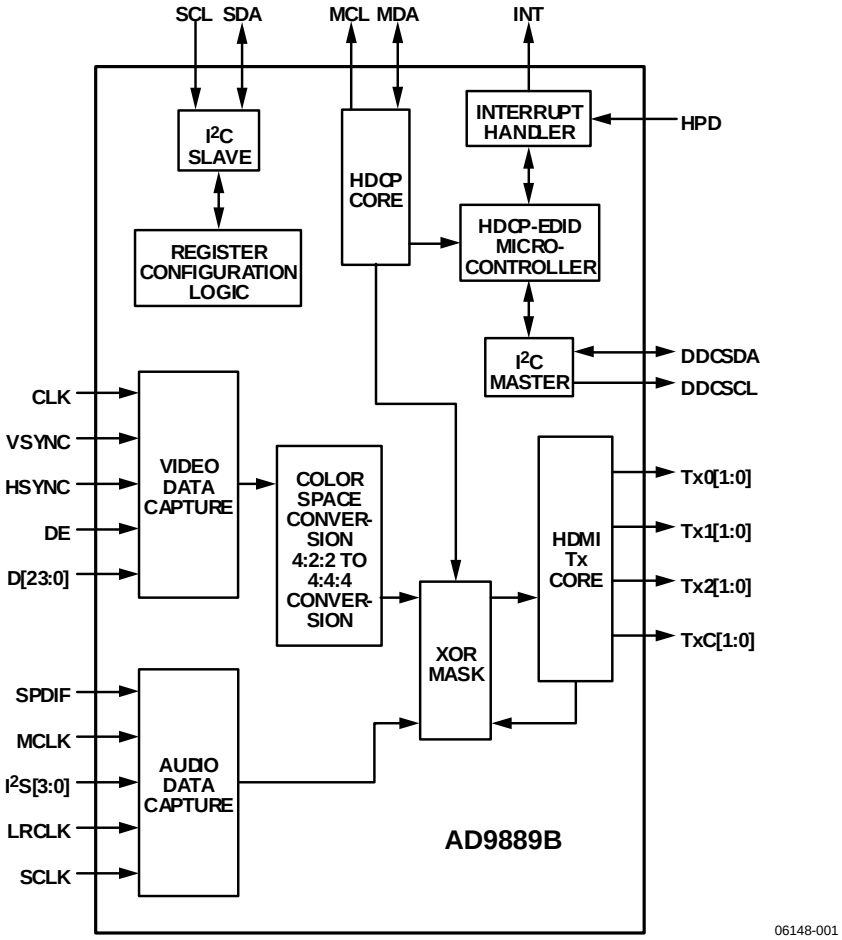
AD9889B Data Sheet
AD9889B Hardware User's Guide
AD9889B Programming Guide
AN-810 - EDID/HDCP Controller Application Note

2.2 Specifications

EIA/CEA-861
HDMI Specification 1.2
HDCP 1.1

SECTION 3: BLOCK DIAGRAM

Figure 1 AD9889B Functional Block Diagram



SECTION 4: SPECIFICATIONS

Table 1 Specifications

Parameter	Conditions	AD9889B					
		Temp	Test Level[1]	Min	Typ	Max	Unit
DIGITAL INPUTS							
Data Inputs – Video and Audio							
Input Voltage, High (V_{IH})		Full	VI	1.4		3.5	V
Input Voltage, Low (V_{IL})		Full	VI	-0.3		0.7	V
Input Capacitance		25°C	VIII		1.0	1.5	pF
I2C Lines (DDCSDA, DDCSCL, SDA, SCL)							
Input Voltage, High (V_{IH})		Full	VI	1.4		3.5	V
Input Voltage, Low (V_{IL})		Full	VI	-0.3		0.7	V
DIGITAL OUTPUTS							
Output Voltage, High (V_{OH})		Full	VI	V_{DD} – 0.1			V
Output Voltage, Low (V_{OL})		Full	VI			0.4	V
THERMAL CHARACTERISTICS							
Thermal Resistance							
θ_{JC} Junction-to-Case		Full	V		20		°C/W
θ_{JA} Junction-to-Ambient		Full	V		43		°C/W
Ambient Temperature		Full	V	0	+25	+85	°C
DC SPECIFICATIONS							
Input Leakage Current, I_{IL}		25°C	VI	–1		+1	µA
POWER SUPPLY							
1.8V Supply Voltage (DVdd, AVdd)		Full	IV	1.71	1.8	1.89	V
1.8V Supply Voltage Noise Limit							
DVdd		Full	IV			32	mV RMS
AVdd	See ► section ►7.1	Full	IV				
Power-Down Current	Refer to the AD9889B Programming Guide	25°C	IV			TBD	mA
Transmitter Total Power	1080p, typical random pattern	Full	VI			216	mW
AC SPECIFICATIONS							
TMDS Output Clock Frequency		25°C	IV	20		165	MHz
TMDS Output Clock Duty Cycle		25°C	IV	48		52	%
Input Video Clock Frequency		Full				165	MHz
Input Video Data Setup Time – t_{VSU}		Full	IV	1			nS
Input Video Data Hold Time – t_{VHLD}		Full	IV	0.7			nS
TMDS Differential Swing		25°C	VII	900	1000	1100	mV
Differential Output Timing							
Low-to-High Transition Time		25°C	VII	75	175		pS
High-to-Low Transition Time		25°C	VII	75	175		pS
V_{SYNC} and H_{SYNC} Delay from DE Falling Edge		25°C	IV		1		UI[2]
V_{SYNC} and H_{SYNC} Delay to DE Rising Edge		25°C	IV		1		UI

Parameter	Conditions	AD9889B					
		Temp	Test Level[1]	Min	Typ	Max	Unit
AUDIO AC TIMING (Figure 3 and Figure 4)							
I^2S[3:0], SPDIF Setup – t_{ASU}		Full	IV	2			nS
I^2S[3:0], SPDIF – t_{AHLD}		Full	IV	2			nS
LRCLK Setup Time – t_{ASU}		Full	IV	2			nS
LRCLK Hold Time – t_{AHLD}		Full	IV	2			nS
I2C Interface (see Figure 25)							
SCL Clock Frequency		Full				400	kHz
SDA Setup Time - t_{DSU}		Full		100			nS
SDA Hold Time – t_{DHO}		Full		100			nS
Setup for Start – t_{STASU}		Full		0.6			uS
Hold Time for Start – t_{STAH}		Full		0.6			uS
Setup for Stop – t_{STOSU}		Full		0.6			uS

[1].See Explanation of Test Levels section.
[2].UI = unit interval.

Figure 2 Timing for Video Data Interface

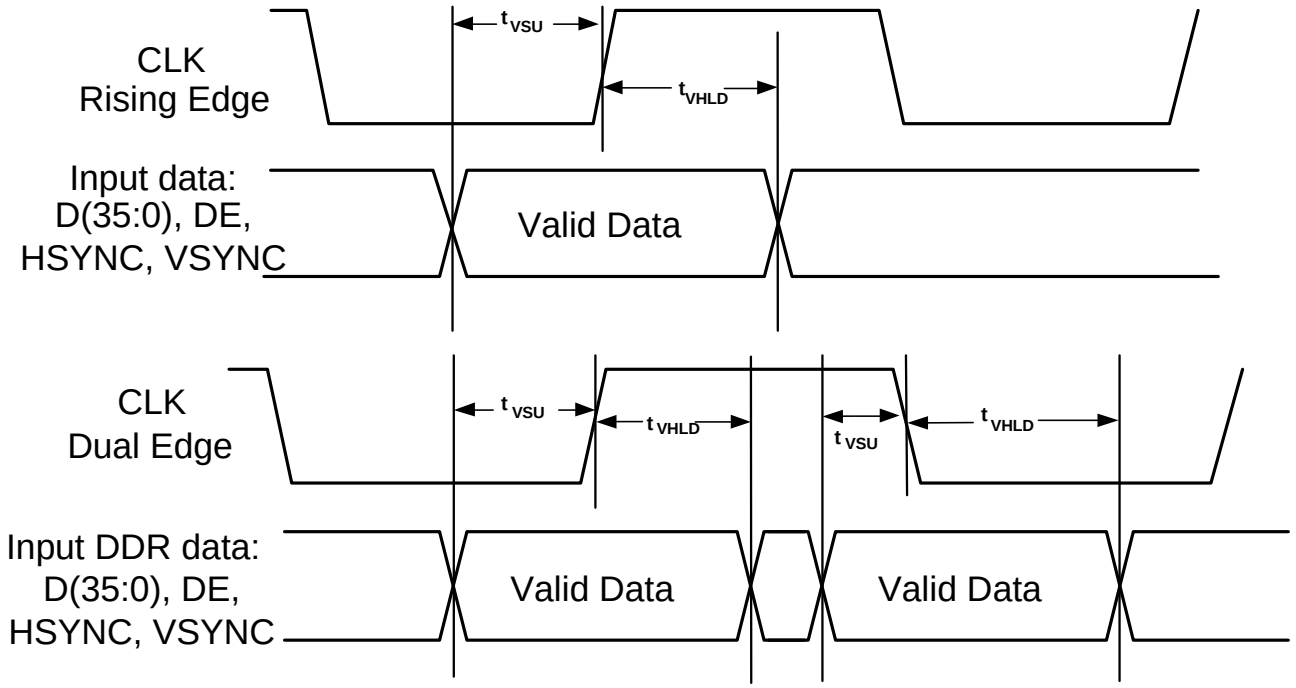


Figure 3 Timing for I2S Audio Interface

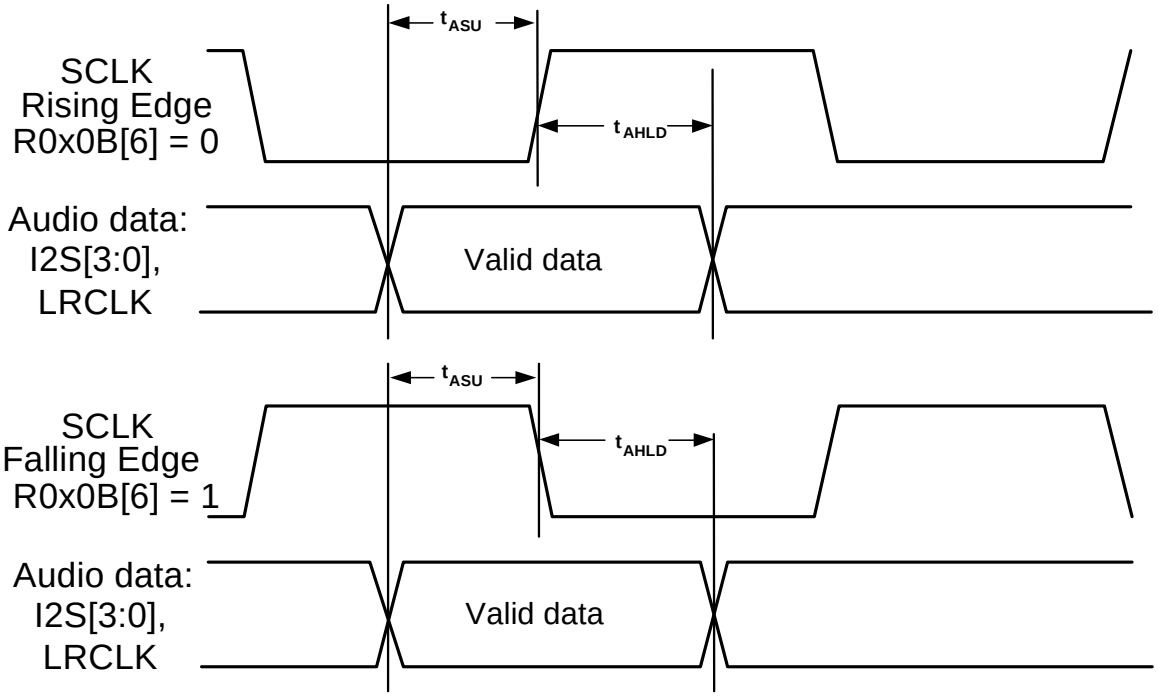


Figure 4 Timing for SPDIF Audio Interface

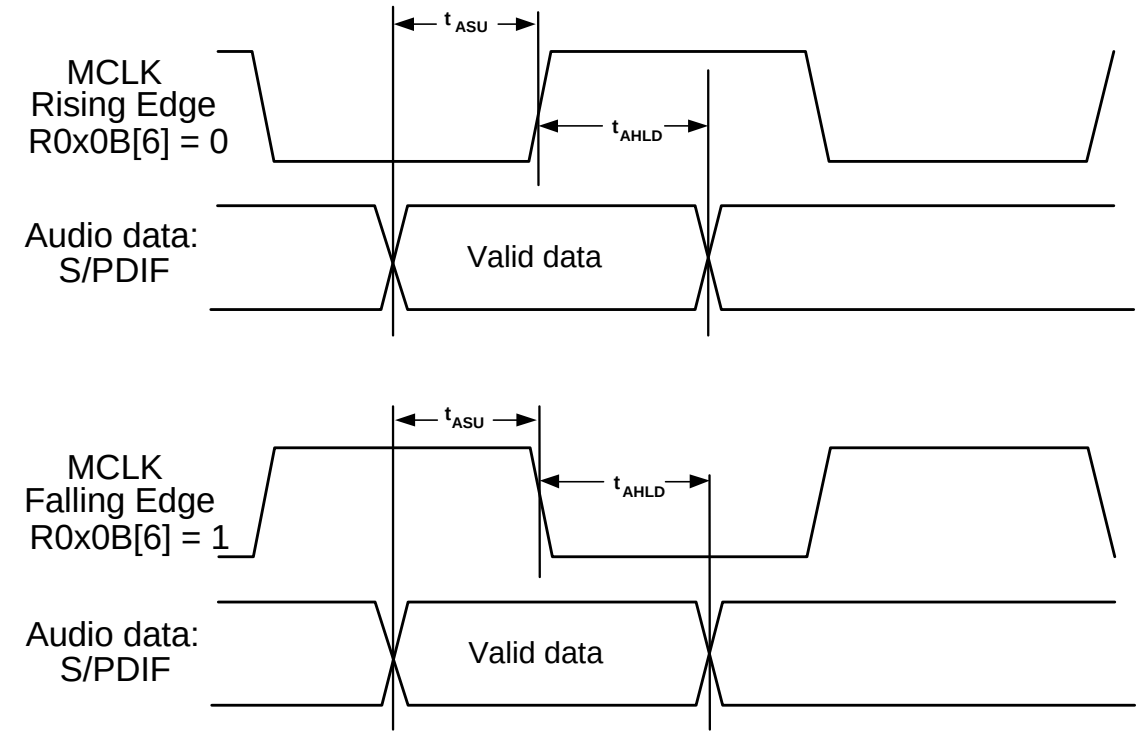


Table 2 Absolute Maximum Ratings

Parameter	Rating
Digital Inputs – I2CHPD	5.5V to -0.3V
Digital Inputs – video/audio inputs	3.6V to -0.3V
Digital Output Current	20 mA
Operating Temperature Range	-40°C to +100°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage ratings assume that all power supplies are at nominal levels.

4.1 Explanation of Test Levels

I.	100% production tested.
II.	100% production tested at 25°C and sample tested at specified temperatures.
III.	Sample tested only.
IV.	Parameter is guaranteed by design and characterization testing.
V.	Parameter is a typical value only.
VI.	100% production tested at 25°C; guaranteed by design and characterization testing.
VII.	Limits defined by HDMI specification; guaranteed by design and characterization testing.
VIII.	Parameter is guaranteed by design.

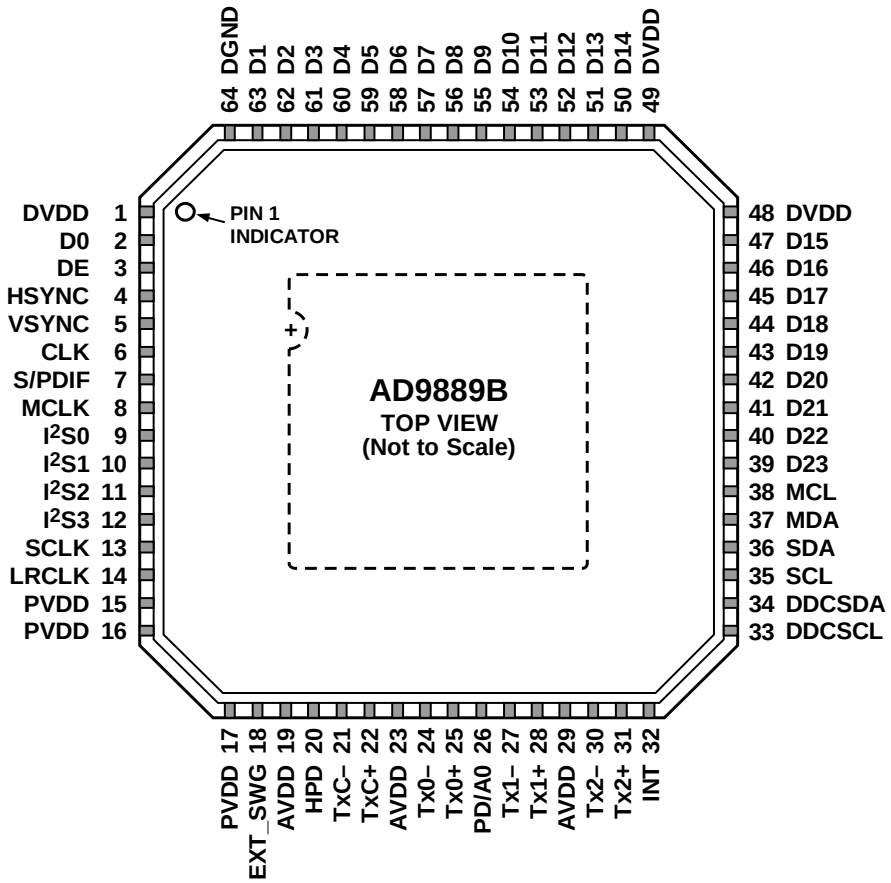
4.2 ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SECTION 5: PIN AND PACKAGE INFORMATION

This section shows the pinout available for the 64-lead LFCSP package, the 80 pin LQFP package and the 76-ball CSPBGA package. This section also contains a brief description of the different pins as well as the mechanical drawings

Figure 5 64-Lead LFCSP Configuration (Top View)



NOTES
1. GND PADDLE ON BOTTOM OF PACKAGE.

06291-003

Figure 6 80-Lead LQFP Configuration (Top View)

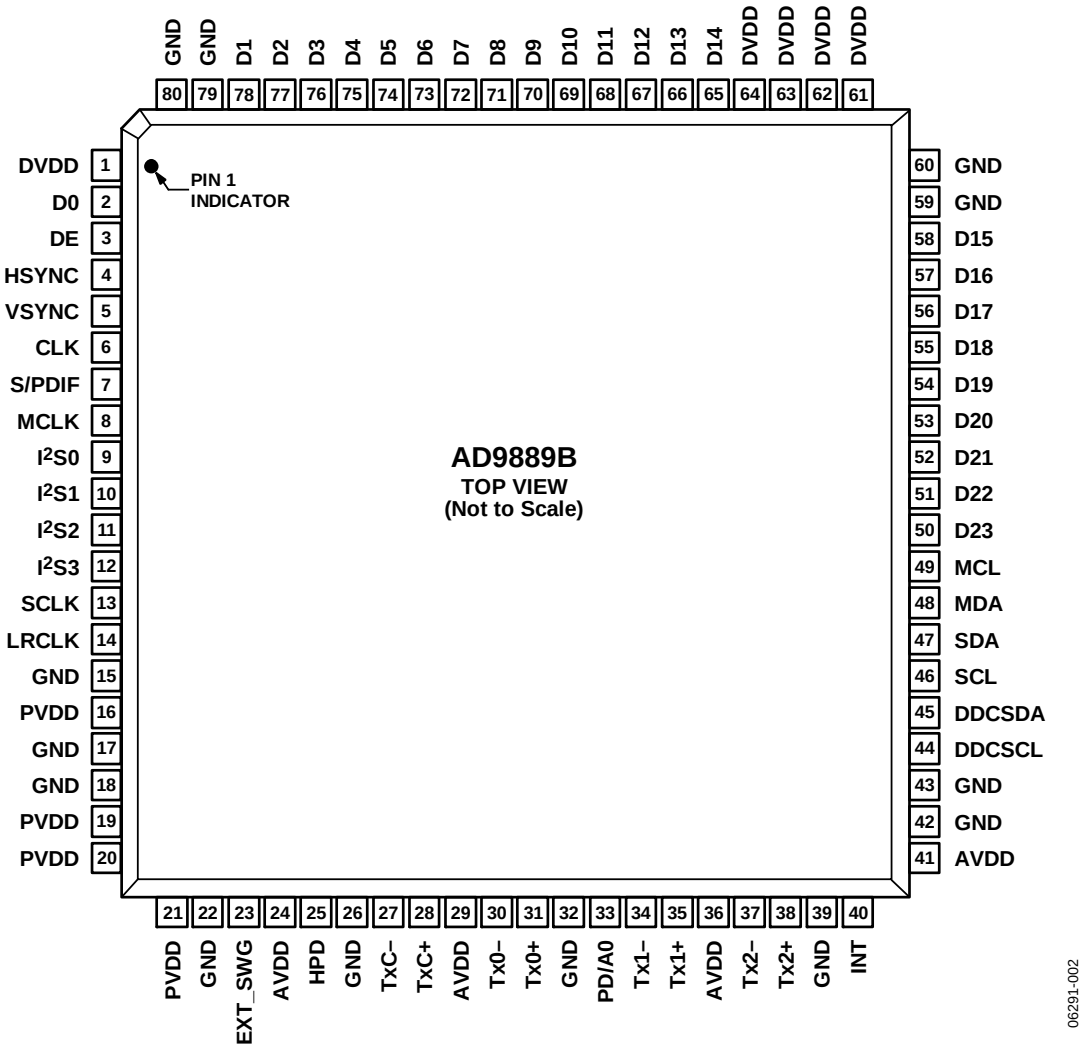


Figure 7 **76-Lead Chip Scale Package BGA Configuration (Top View)**

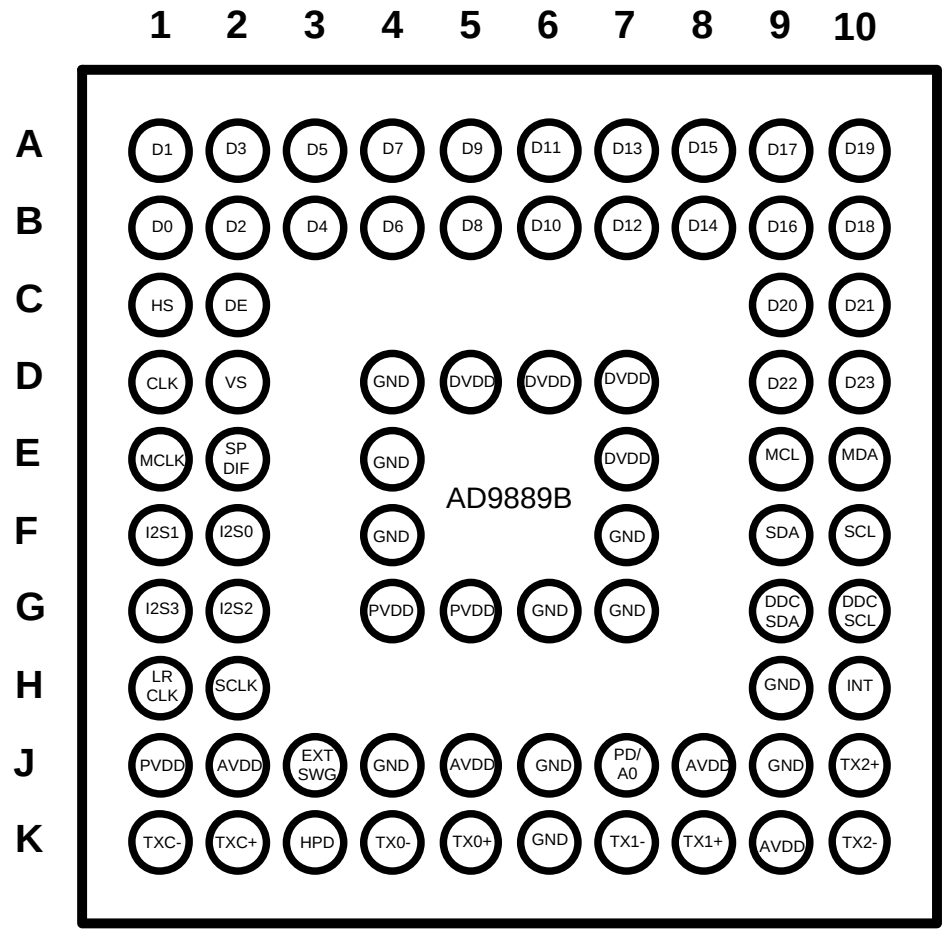


Table 3 **Complete Pinout List AD9889B**

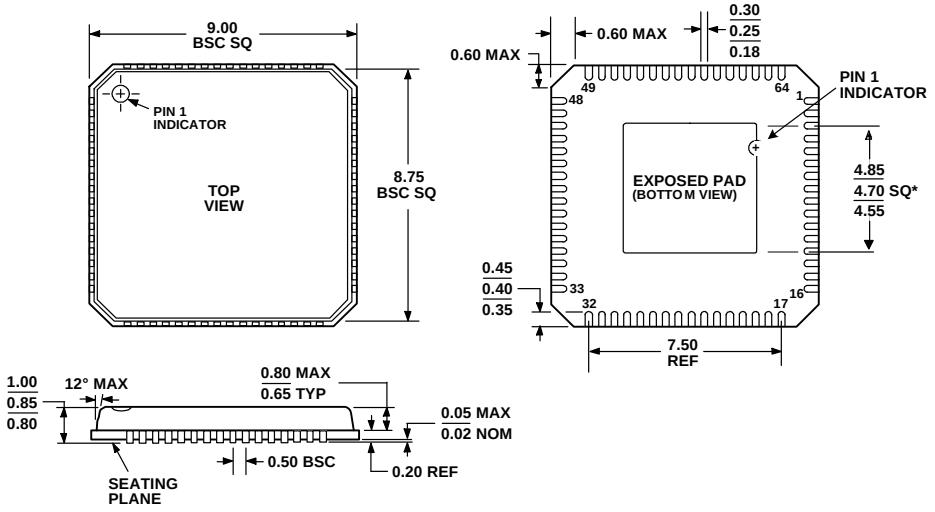
Pin No. LFCSP	Pin No. LQFP	Pin No. BGA	Mnemonic	Type[1]	Description
39 – 47, 50 -63, 2	50-58, 65-78, 2	D10, D9, C10, C9,A10, B10, A9, B9,A8, B8, A7, B7, A6, B6, A5, B5, A4, B4, A3, B3, A2, B2, A1, B1	D[23:0]	I	Video Data Input. Digital input in RGB or YCbCr format. Supports typical CMOS logic levels from1.8V up to 3.3V. • Figure 2 for timing diagram details.
6	6	D1	CLK	I	Video Clock Input. Supports typical CMOS logic levels from1.8V up to 3.3V.
3	3	C2	DE	I	Data Enable Bit for Digital Video. Supports typical CMOS logic levels from1.8V up to 3.3V.
4	4	C1	HSYNC	I	Horizontal Sync Input. Supports typical CMOS logic levels from1.8V up to 3.3V.
5	5	D2	VSYNC	I	Vertical Sync Input. Supports typical CMOS logic levels from1.8V up to 3.3V.
18	23	J3	R_EXT	I	Sets internal reference currents. Place 887 Ω resistor (1% tolerance) between this pin and ground.
20	25	K3	HPD	I	Hot Plug Detect Signal. This indicates to the interface whether the

Pin No. LFCSP	Pin No. LQFP	Pin No. BGA	Mnemonic	Type[1]	Description
					receiver is connected. 1.8V to 5.0 V CMOS logic level.
7	7	E2	SPDIF	I	SPDIF (Sony/Philips Digital Interface) Audio Input. This is the audio input from a Sony/Philips digital interface. Supports typical CMOS logic levels from1.8V up to 3.3V. See Figure 4 for timing diagram details.
8	8	E1	MCLK	I	Audio Reference Clock. 128 × N × f_S with N = 1, 2, 3, or 4. Set to 128 × sampling frequency (f_S), 256 × f_S, 384 × f_S, or 512 × f_S. Supports typical CMOS logic levels from1.8V up to 3.3V.
12 - 9	9-12	F2, F1, G2, G1	I^2S[3:0]	I	I^2S Audio Data Inputs. These represent the eight channels of audio (two per input) available through I^2S. Supports typical CMOS logic levels from1.8V up to 3.3V. See Figure 3 for timing diagram details.
13	13	H2	SCLK	I	I^2S Audio Clock. Supports typical CMOS logic levels from1.8V up to 3.3V.
14	14	H1	LRCLK	I	Left/Right Channel Selection. Supports typical CMOS logic levels from1.8V up to 3.3V.
26	33*	J7	PD/AD	I	Power-Down Control and I^2C Address Selection. The I^2C address and the PD polarity are set by the PD/AD pin state when the power supplies are applied to the AD9889B. Supports typical CMOS logic levels from1.8V up to 3.3V.
21, 22	27, 28	K1, K2	TxC–/TxC+	O	Differential Clock Output. Differential clock output at pixel clock rate; TMDS logic level.
30, 31	37, 38	K10, J10	Tx2–/Tx2+	O	Differential Output Channel 2. Differential output of the red data at 10× the pixel clock rate; TMDS logic level.
27, 28	34, 35	K4, K5	Tx1–/Tx1+	O	Differential Output Channel 1. Differential output of the green data at 10× the pixel clock rate; TMDS logic level.
24, 25	30, 31	K7, K8	Tx0–/Tx0+	O	Differential Output Channel 0. Differential output of the blue data at 10× the pixel clock rate; TMDS logic level.
32	40	H10	INT	O	Interrupt. CMOS logic level. A 2 kΩ pull up resistor to AVDD is recommended.
19, 23, 29	24, 29, 36, 41	J2, J5, J8, K9	AVDD	P	1.8V Power Supply for TMDS Outputs.
1, 48, 49	1, 61, 62, 63, 64	D5, D6, D7, E7	DVDD	P	1.8V Power Supply for Digital and I/O Power Supply. These pins supply power to the digital logic and I/Os. They should be filtered and as quiet as possible.
15, 16, 17	16, 19, 20, 21	G4, G5, J1	PVDD	P	1.8V PLL Power Supply. The most sensitive portion of the AD9889B is the clock generation circuitry. These pins provide power to the clock PLL. The designer should provide quiet, noise-free power to these pins.
64	15, 17, 18, 22, 26, 32, 39, 42, 43, 59, 60, 79, 80	D4, E4, F4, J4, G6, J6, K6, F7, G7, H9, J9	GND	P	Ground. The ground return for all circuitry on-chip. It is recommended that the AD9889B be assembled on a single, solid ground plane with careful attention given to ground current paths. Note that pad beneath package is ground.
36	47	F9	SDA	C[2]	Serial Port Data I/O. This pin serves as the serial port data I/O slave for register access. Supports CMOS logic levels from 1.8V to 3.3V.
35	46	F10	SCL	C	Serial Port Data Clock. This pin serves as the serial port data clock slave for register access. Supports CMOS logic levels from 1.8V to 3.3V.
37	48	E10	MDA	C	Serial Port Data I/O to EEPROM for HDCP Keys
38	49	E9	MCL	C	Serial Port Data Clock to EEPROM for HDCP Keys
33	45	G9	DDCSDA	C	Serial Port Data I/O to Receiver. This pin serves as the master to the DDC bus. 5 V CMOS logic level.
34	44	G10	DDCSCL	C	Serial Port Data Clock to Receiver. This pin serves as the master clock for the DDC bus. 5 V CMOS logic level.

1. I = input, O = output, P = power supply, C = control

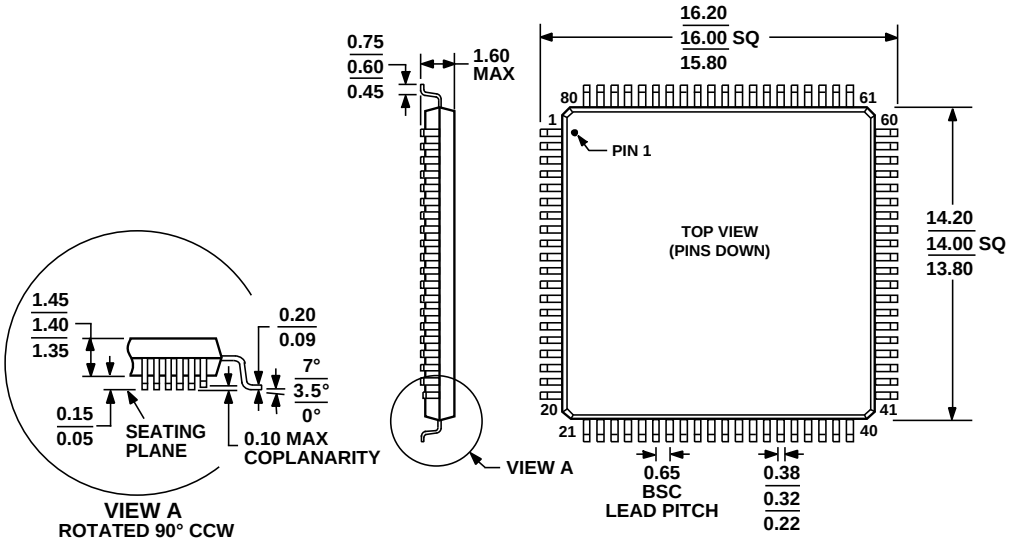
5.1 Mechanical Drawings and Outline Dimensions

Figure 8 64-Lead Lead Frame Chip Scale Package [LFCSP] (CP-64-1)



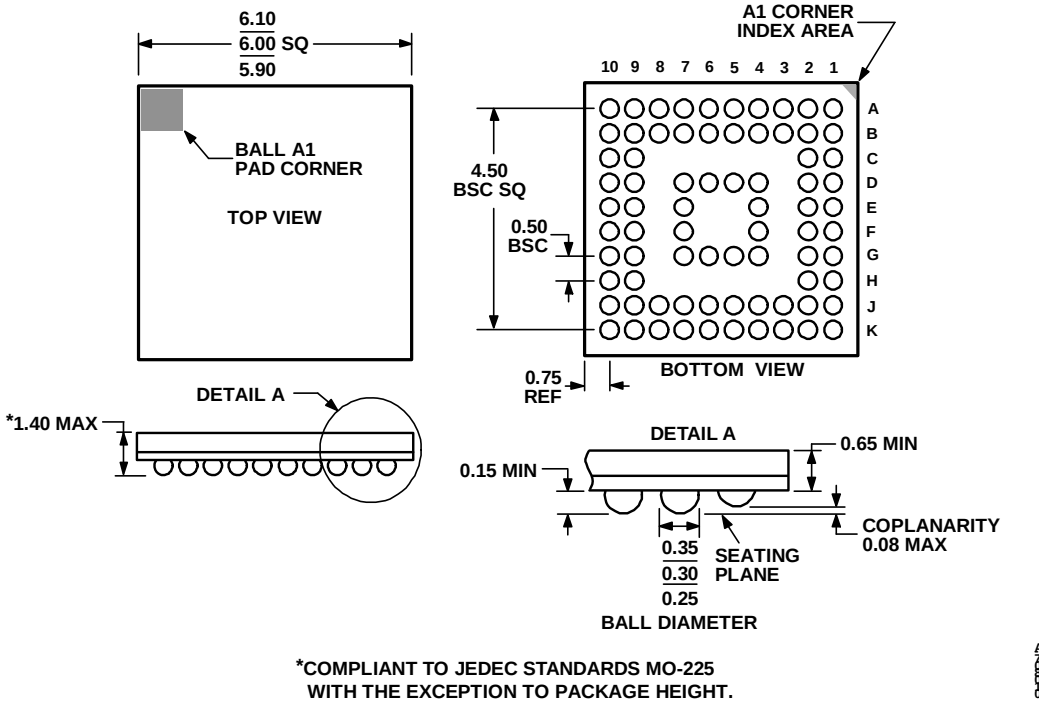
64 LFCSP (LEAD FRAME CHIP SCALE PACKAGE)
*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD
EXCEPT FOR EXPOSED PAD DIMENSION
DIMENSIONS in Millimeters

Figure 9 80-Pin LQFP Package (ST-80-2)



COMPLIANT TO JEDEC STANDARDS MS-026-BEC

Figure 10 76-Ball Chip Scale Package Ball Grid Array [CSPBGA] (BC-76-1)



*COMPLIANT TO JEDEC STANDARDS MO-225
WITH THE EXCEPTION TO PACKAGE HEIGHT.

SECTION 6: FUNCTIONAL DESCRIPTION

6.1 Input Connections

6.1.1 Unused Inputs

Any input data signals which are not used should be tied to ground.

6.1.2 Video Data Capture Block

The AD9889B can accept video data from as few as eight pins (either YCbCr 4:2:2 double data rate [DDR] or YCbCr 4:2:2 with 2x pixel clock) to as many as 24 pins (RGB 4:4:4 or YCbCr 4:4:4). In addition it can accept HSYNC, VSYNC and DE (Data Enable). The AD9889B can detect all of the 59 video formats defined in the EIA/CEA-861D specification. Either separate HSYNC, VSYNC, and DE, or embedded syncs in the style of the ITU BT.656, SMPTE 274M, and SMPTE 296M specifications are accepted. For timing details for video capture, see ► Figure 2. For complete details on how to set these, refer to the AD9889B Programming Guide.

The tables in ► section 6.1.2.1 define how the many different formats are accepted on the input data lines.

6.1.2.1 *Video Input Connections*

The following table is a summary of the input options which are shown in detail in ► Table 5 through ► Table 9 and in ► Figure 11 through ► Figure 15.

Table 4 Input ID Selection

Input ID	Bits per Color	Pin Assignment Table	Maximum Input Clock	Format Name	Sync Type
0	8	Table 5	165.0 MHz	RGB 4:4:4, YCbCr 4:4:4	Separate syncs
1	8, 10, 12	Table 6	165.0 MHz	YCbCr 4:2:2	Separate syncs
2	8, 10, 12		165.0 MHz	YCbCr 4:2:2	Embedded syncs
3	8, 10, 12	Table 7	82.5 MHz	YCbCr 4:2:2 2X clock	Separate syncs
4	8, 10, 12		82.5 MHz	YCbCr 4:2:2 2X clock	Embedded syncs
5	8	Table 8	82.5 MHz	RGB 4:4:4, YCbCr 4:4:4 DDR	Separate syncs
6	8, 10, 125	Table 9	82.5 MHz	YCbCr 4:2:2 DDR	Separate syncs

Table 5 Normal RGB or YCbCr 4:4:4 (24 bits) with Separate Syncs; Input ID = 0

Input Format	Data<23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RGB 444	R[7:0]								G[7:0]								B[7:0]							
YCbCr 444	Cr[7:0]								Y[7:0]								Cb[7:0]							
An input format of RGB 4:4:4 or YCbCr 4:4:4 can be selected by setting the input ID (R0x15 [3:1]) to 0b000. There is no need to set the Input Style (R0x16[3:2]).																								

Table 6 YCbCr 4:2:2 Formats (24, 20, or 16 bits) Input ID = 1 or 2

Input Format	Data<23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Style 1																								
YCbCr422 Sep. Sync (24 bit)	Cb[11:4]								Y[11:4]								Cb[3:0]				Y[3:0]			
	Cr[11:4]								Y[11:4]								Cr[3:0]				Y[3:0]			
YCbCr422 Sep. Sync (20 bit)	Cb[9:2]								Y[9:2]								Cb[1:0]				Y[1:0]			
	Cr[9:2]								Y[9:2]								Cr[1:0]				Y[1:0]			
YCbCr422 Sep. Sync (16 bit)	Cb[7:0]								Y[7:0]															
	Cr[7:0]								Y[7:0]															
Style 2																								
24 bit	Cb[11:0]												Y[11:0]											
	Cr[11:0]												Y[11:0]											
20 bit	Cb[9:0]										Y[9:0]													
	Cr[9:0]										Y[9:0]													
16 bit	Cb[7:0]								Y[7:0]															
	Cr[7:0]								Y[7:0]															
Style 3																								
24 bit	Y[11:0]												Cb[11:0]											
	Y[11:0]												Cr[11:0]											
20 bit	Y[9:0]										Cb[9:0]													
	Y[9:0]										Cr[9:0]													
16 bit	Y[7:0]								Cb[7:0]															
	Y[7:0]								Cr[7:0]															

An input with YCbCr 422 with separate syncs can be selected by setting the Input ID (R0x15[3:1]) to 0b001. The data bit width (24, 20, or 16 bits) must be set with R0x16 [5:4]. The 3 input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2].

An input with YCbCr 422 with embedded syncs (SAV [Start of Active Video] and EAV [End of Active Video]) can be selected by setting the Input ID (R0x15[3:1]) to 0b010. The data bit width (24 = 12bit, 20 = 10 bit, or 16 = 8 bits) must be set with R0x16 [5:4]. The 3 input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The only difference between Input ID 1 and Input ID 2 is that the syncs on ID 2 are embedded in the data much like an ITU 656 style bus running at 1X clock and double width.

Table 7 YCbCr 4:2:2 Formats (12, 10, or 8 bits) Input ID = 3, 4

Input Format	Data <23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Style 1																								
12 bit									Cb/Y/Cr/Y[11:4]												[3:0]			
10 bit									Cb/Y/Cr/Y[9:2]												[1:0]			
8 bit									Cb/Y/Cr/Y[7:0]															
Style 2																								
12 bit													Cb/Y/Cr/Y[11:0]											
10 bit															Cb/Y/Cr/Y[9:0]									
8 bit																	Cb/Y/Cr/Y[7:0]							
An input with YCbCr 422 data and separate syncs can be selected by setting the Input ID (R0x15[3:1]) to 0b011. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The 2 input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. This mode requires an input clock 2X the pixel rate																								
An input with YCbCr 422 and embedded syncs (ITU 656 based) can be selected by setting the Input ID (R0x15[3:1]) to 0b100. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The 2 input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The order of data input is the order in the table. For example, data is accepted as: Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3… This mode requires an input clock 2X the pixel rate.																								

Figure 11 DDR DE timing - register 0x16[1] = 0

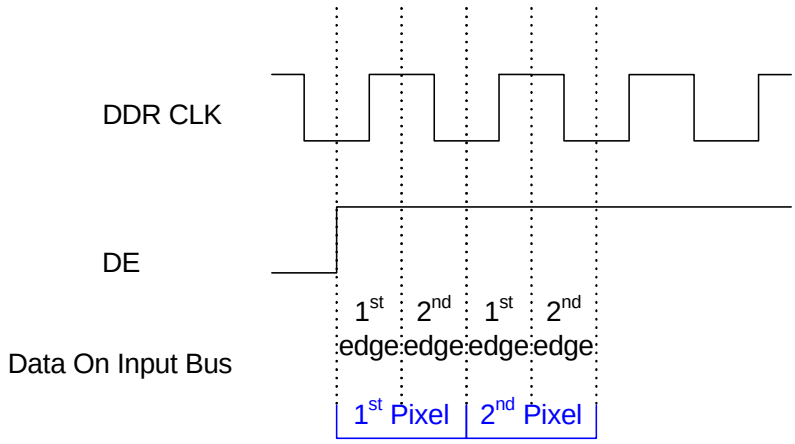


Figure 12 DDR DE timing - register 0x16[1] = 1

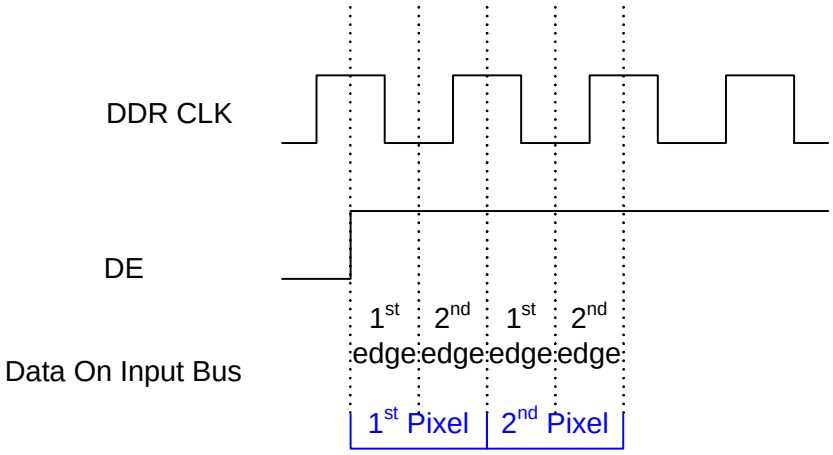


Figure 13 2X Clock DE timing - register 0x0B[6] = 0

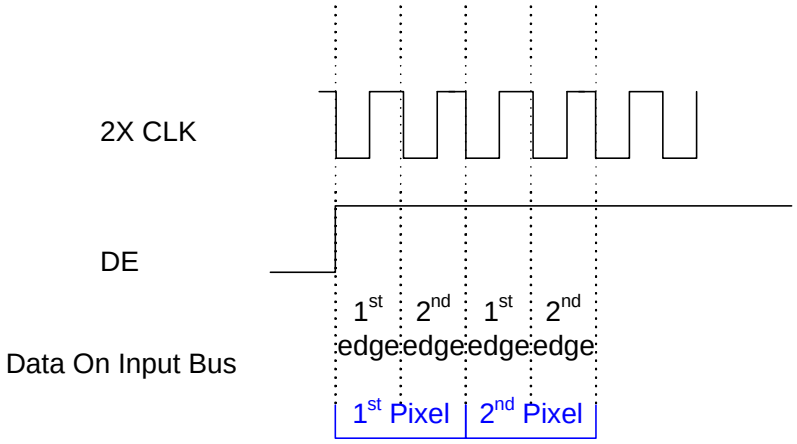


Figure 14 2X Clock DE timing - register 0x0B[6] = 1

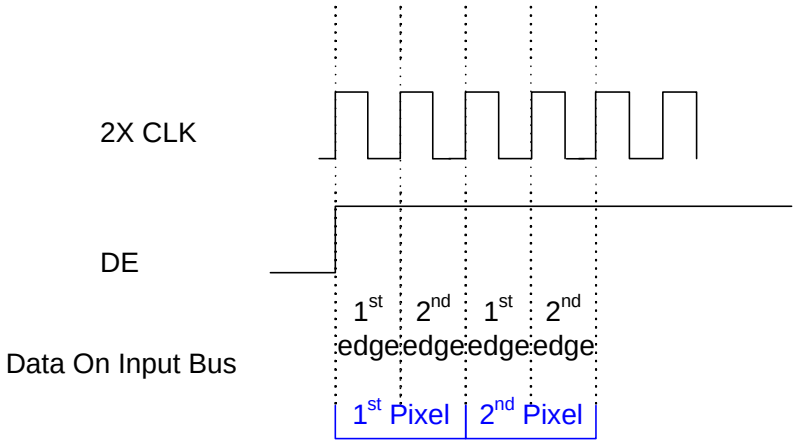


Table 8 RGB or YCbCr 4:4:4 (12 bits) DDR with Separate Syncs; Input ID = 5

Input Format	Data <23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Style 1																								
RGB 444 (DDR) (1st edge, 2nd edge)													G[3:0]				B[7:0]							
													R[7:0]							G[7:4]				
YCbCr444(DDR) (1st edge, 2nd edge)													Y[3:0]				Cb[7:0]							
													Cr[7:0]							Y[7:4]				
Style 2																								
RGB 444 (DDR) (1st edge, 2nd edge)													R[7:0]							G[7:4]				
													G[3:0]				B[7:0]							
YCbCr444 (DDR) (1st edge, 2nd edge)													Cr[7:0]							Y[7:4]				
													Y[3:0]				Cb[7:0]							
Style 3																								
YCbCr444 (DDR) (1st edge, 2nd edge)													Y[7:0]							Cb[7:4]				
													Cb[3:0]				Cr[7:0]							

An input format of RGB 4:4:4 DDR or YCbCr 4:4:4 DDR can be selected by setting the input ID (R0x15 [3:1]) to 0b101. The 3 input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:2:2 word and should be where DE starts. See ► Figure 11 and► Figure 12.

Figure 15 DDR DE timing - register 0x16[1] = 0

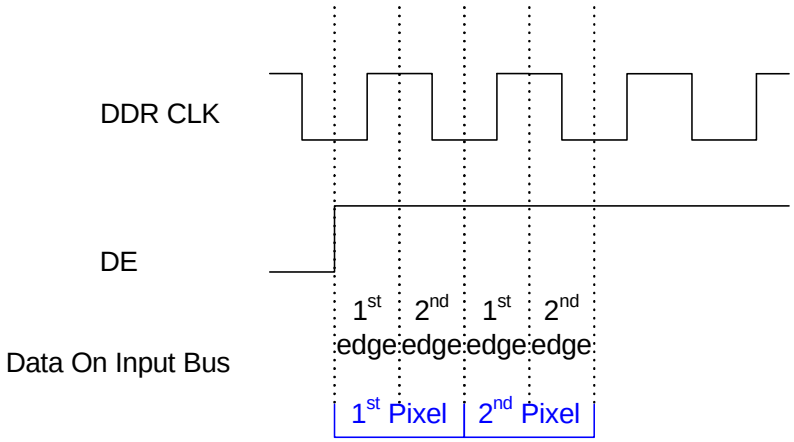
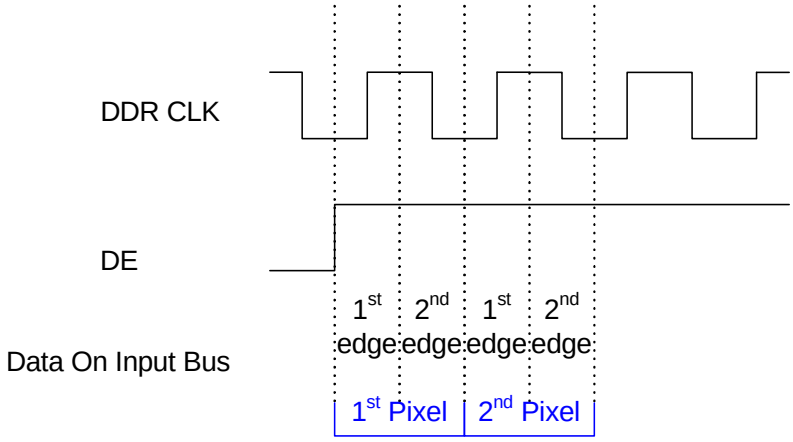


Table 9 YCbCr 4:2:2 (12, 10, or 8 bits) DDR with Separate Syncs; Input ID = 6

Input Format	Data<23:0>																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Style 1																								
YCrCb422 Sep Syncs (DDR) 12 bit			1st pixel						1st edge				Y[7:4]				Cb[3:0]				Y[3:0]			
						2nd edge							Cb[11:4]								Y[11:8]			
			2nd pixel										Y[7:4]				Cr[3:0]				Y[3:0]			
													Cr[11:4]								Y[11:8]			
YCrCb422 Sep Syncs (DDR) 10 bit													Y[5:4]		Cb[3:0]				Y[3:0]					
													Cb[9:4]						Y[9:6]					
													Y[5:4]		Cr[3:0]				Y[3:0]					
													Cr[9:4]						Y[9:6]					
YCrCB 422 Sep. Syncs (DDR) 8 bit													Cb[3:0]				Y[3:0]							
													Cb[7:4]				Y[7:4]							
													Cr[3:0]				Y[3:0]							
													Cr[7:4]				Y[7:4]							
Style 2																								
12 bit													Y[11:0]											
													Cb[11:0]											
													Y[11:0]											
													Cr[11:0]											
10 bit													Y[9:0]											
													Cb[9:0]											
													Y[9:0]											
													Cr[9:0]											
8 bit													Y[7:0]											
													Cb[7:0]											
													Y[7:0]											
													Cr[7:0]											
Style 3																								
12 bit													Cb[11:0]											
													Y[11:0]											
													Cr[11:0]											
													Y[11:0]											
10 bit													Cb[9:0]											
													Y[9:0]											
													Cr[9:0]											
													Y[9:0]											
8 bit													Cb[7:0]											
													Y[7:0]											
													Cr[7:0]											
													Y[7:0]											

An input format of YCbCr 4:2:2 DDR can be selected by setting the input ID (R0x15 [3:1]) to 0b110. The 3 different input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The Data Input Edge is defined in R0x16 [1]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:2:2 word and should be where DE starts. See ► Figure 11 and Figure 12.

Figure 16 DDR DE timing - register 0x16[1] = 0



6.1.3 Audio Data Capture Block

The AD9889B supports multiple audio formats: I2S and SPDIF. The AD9889B supports audio input frequencies of 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz. The MCLK signal input is optional. The I2S audio inputs can support standard I2S, left-justified serial audio or right-justified serial audio. The Audio Data Capture Block captures the audio samples and converts them into audio packets which are sent through the HDMI link (if the AD9889B is set in HDMI mode). Please refer to the AD9889B Programming Guide for more information.

6.1.3.1 *SUPPORTED AUDIO INPUT FORMAT AND IMPLEMENTATION*

AD9889B is capable of receiving audio data for packetization and transmission over the HDMI interface in any of the following formats:

- Inter IC Sound (I2S)
- Sony/Philips Digital Interface (SPDIF)

Table 10 illustrates the many audio input and output options that are available with the AD9889B.

Table 10 Audio input format summary

Audio Select	I2S Format	Data Input Pins	Clock	Encoding	Format	Output Packet Type
R0x0A[4]	R0x0C[1:0]					
0	00	I2S[3:0]	SCLK	Normal	Standard I2S	Audio Sample Packet
0	01	I2S[3:0]	SCLK	Normal	Right Justified	Audio Sample Packet
0	10	I2S[3:0]	SCLK	Normal	Left Justified	Audio Sample Packet
0	11	I2S[3:0]	SCLK	Normal	AES3 Direct	Audio Sample Packet
1	**	SPDIF	MCLK	Bi-Phase Mark	IEC60958 or IEC61937	Audio Sample Packet

6.1.3.2 *I2S AUDIO*

The AD9889B can accommodate from two to eight channels of I2S audio at up to a 192KHz sampling rate. The AD9889B supports standard I2S, left-justified serial audio and right-justified serial audio formats via R0x0C[1:0] and sample word lengths between 16 bits and 24 bits (R0x14[3:0]). See Figure 17 to Figure 20 for format information, For timing information, see ► Figure 3.

If the I2S data changes on the rising clock edge it is recommended that it be latched into the AD9889B on the falling edge. If the I2S data changes on the falling clock edge, it is recommended that it be latched into the AD9889B on the rising edge. This can be specified by programming register R0x0B[6]. 0 = latch on the rising clock edge; 1 = latch on the falling clock edge. See Figure 3 for the timing details.

Figure 17 I2S Standard Audio – Data width 16 to 24 bits per channel

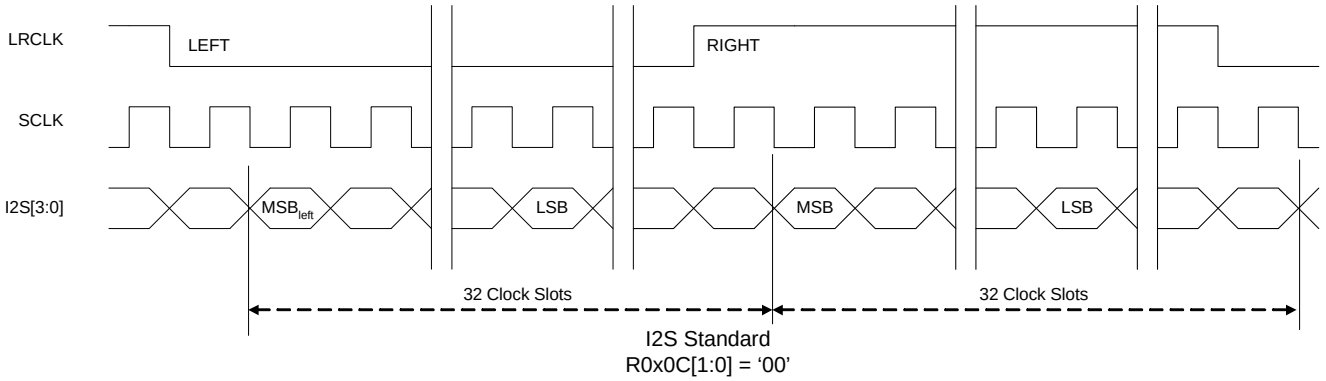
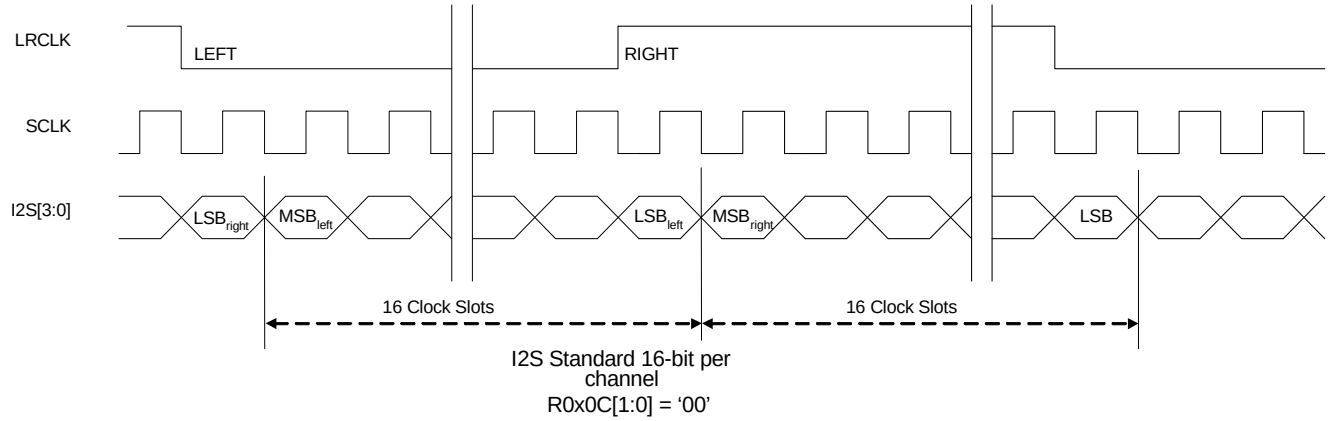
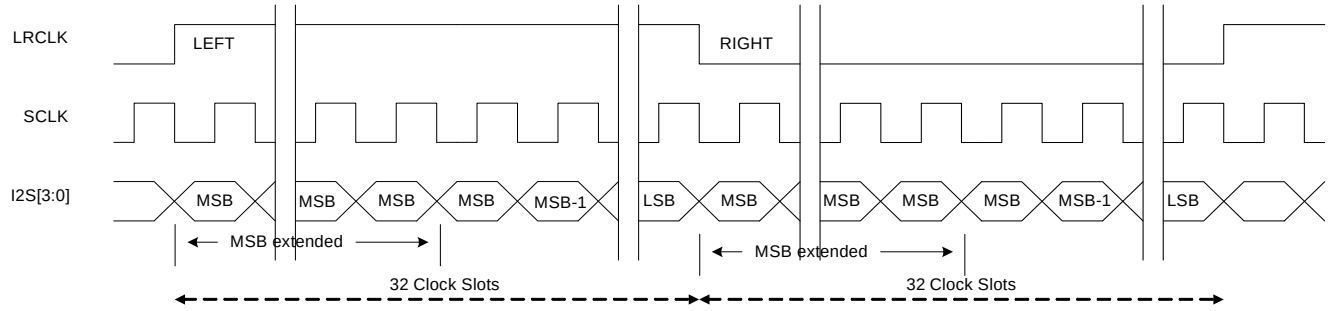


Figure 18 I2S Standard Audio – 16-bit samples only



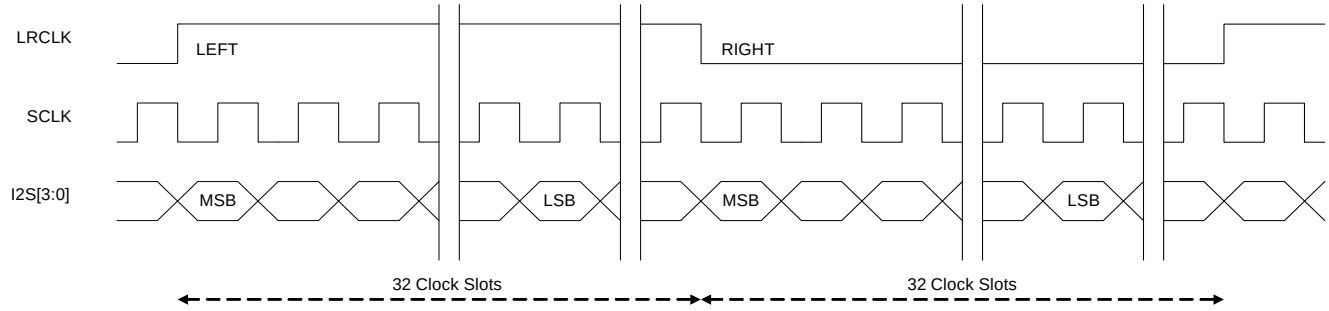
I2S Standard 16-bit per channel
R0x0C[1:0] = '00'

Figure 19 Serial Audio – Right-Justified



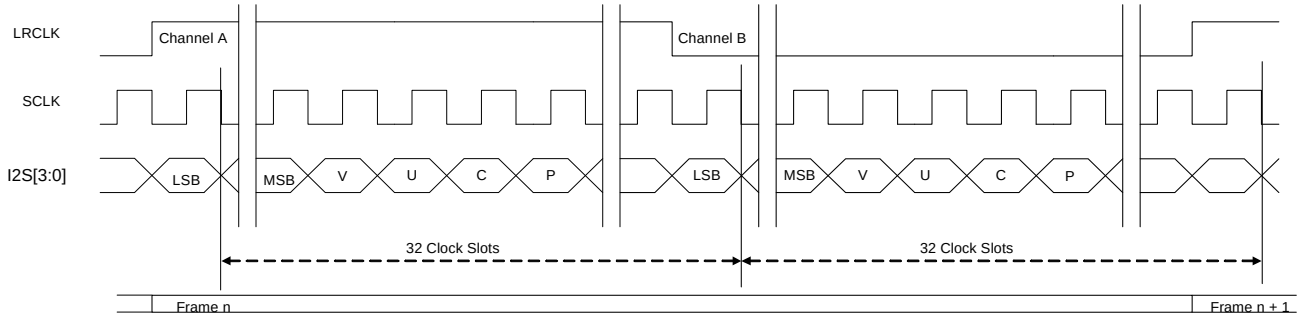
Serial Audio
Right Justified
R0x0C[1:0] = '01'

Figure 20 Serial Audio – Left-Justified



Serial Audio
Left Justified
R0x0C[1:0] = '10'

Figure 21 AES3 Direct Audio

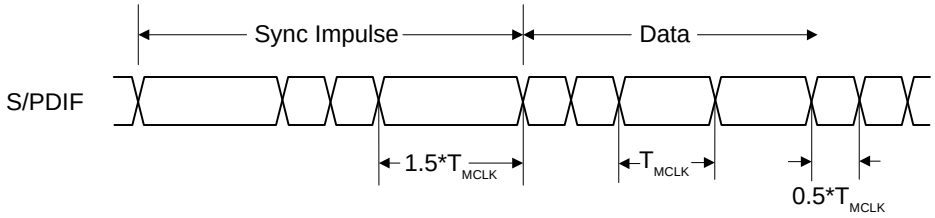


AES3 Direct Audio
R0x0C[1:0] = '11'

6.1.3.3 *SPDIF*

The AD9889B is capable of accepting two-channel linear pulse code modulation (LPCM) and encoded audio up to a 192KHz sampling rate via the SPDIF. SPDIF audio input is selected by setting R0x0A[4] = '1'. The AD9889B is capable of accepting SPDIF with or without an MCLK input. When no MCLK is present the AD9889B generates its own MCLK. For timing information see ► Figure 22.

Figure 22 SPDIF Data Timing



6.1.4 Hot Plug Detect (HPD) pin

The Hot Plug Detect (HPD) pin is an input which detects if a DVI or HDMI sink is connected. If the voltage on HPD is greater than 1.2V, then the AD9889B considers an HDMI/DVI sink is connected. If the voltage is below 1.2V, then the AD9889B considers an HDMI/DVI sink is not connected. The HPD must be connected to the HDMI connector. A 10KΩ pull down resistor to ground is recommended: this ensures that 0V is present on the HPD pin when no sink is connected.

6.1.5 Power Down / I2C Address (PD/AD)

The Power Down / Address (PD/AD) input pin can be connected to GND or supply (through a 2KΩ resistor or a control signal). The device address and power down polarity is set by the state of the PD/AD pin when the AD9889B supplies are applied. For example, if the PD/AD pin is low (when the supplies are turned on) then the device address will be 0x72 and the power down will be active high. If the PD/AD pin is high (when the supplies are turned on), the device address will be 0x7A and the power down will be active low.

6.1.6 Input Voltage Tolerance

The digital inputs (video, audio) on the AD9889B work with 1.8V and 3.3V signal levels. The I2C ports (DDCSDA/DDCSCL and SDA/SCL) work with 1.8V and 3.3V and are tolerant of 5V logic levels

6.2 Output Connections

6.2.1 Output Formats Supported

The AD9889B supports the following output formats:

- 24 bit RGB 4:4:4
- 24 bit YCbCr 4:4:4
- 24 bit YCbCr 4:2:2

6.2.2 TMDS Outputs

The three TMDS output data channels have signals which can run up to 1.62GHz. It is highly recommended to match the length of the traces in order to minimize the following:

- Intra-pair skew (skew between + and -)
- Inter-pair skew (skew between Channels 0, 1, and 2 and Clock)

The traces should also have a 50 Ohm transmission line impedance characteristic (100 Ohms differential). This is very important to avoid any reflections, thus outputting the best Eye Diagram. Also minimize the trace length as much as possible to minimize the resistance path. This is generally done by placing the AD9889B close to the HDMI connector.

6.2.2.1 *ESD Protection*

In order to provide ESD protection to the TMDS differential pairs, DDCSDA, DDCSCL and CEC signals, it is recommended that low capacitance (<0.6pF) varistors are used, such as the Panasonic EZAEG2A device. Please refer to ► Figure 30 for connection of the varistors. The ESD suppressors should be placed as close as possible to the HDMI connector. The differential nets of the TMDS lines should be routed through the pad of the ESD suppressor to minimize the disruption in the differential impedance.

6.2.2.2 *EMI Prevention*

Most applications using the AD9889B should not require EMI filtering. However, if it is necessary to reduce the EMI emissions (predominantly at higher frequencies), we recommend use of common mode chokes placed in the TMDS lines as close to the AD9889B as is possible. Two such options are the Murata DLW21SN670HQ2L (67Ω) or DLW21SN900HQ2 (90Ω).

6.2.3 Display Data Channel (DDC) pins

The Display Data Channel (DDCSCL and DDCSDA) pins need to have the minimum amount of capacitance loading to ensure the best signal integrity. The DDCSCL and DDCSDA capacitance loading must be less than 50pF to meet the HDMI compliance specification. The DDCSCL and DDCSDA must be connected to the HDMI connector and a pull-up resistor to 5V is required. The pull-up resistor must have a value between 1.5KΩ and 2KΩ. The Enhanced Display Identification (EDID) EEPROM on the HDMI/DVI sink is expected to have an address of 0xA0. It is recommended to match the length of the DDCSCL and DDCSDA lines. Please refer to section ► 6.2.2.1 for recommendations for ESD protection.

6.2.4 Interrupt Output (INT)

The AD9889B provides the INT (interrupt) pin in order to enable an interrupt driven system design. The interrupt pin is an open drain output. It should be pulled to a logic high level (such as 1.8V or 3.3V depending on the high logic level of the microcontroller) through a resistor (2KΩ to 5KΩ). It should also be connected to the input of the system's microcontroller. Refer to the ▹*AD9889B Programming Guide* for more information on using the interrupt.

6.3 Video Data Formatting

Following the Input Data Capture are the options for Color Space Conversion (CSC) and for formatting between 4:4:4 and 4:2:2. Taken together these can alter an input stream from: RGB to YCbCr (4:4:4 or 4:2:2), or YCbCr to RGB. Required video control signals such as Hsync, Vsync and Data Enable (DE) can be generated from different input formats and can be adjusted for optimum position

6.3.1 DE, Hsync and Vsync Generation

When transmitting video data across the TMDS interface, it is necessary to have an Hsync, Vsync, and Data Enable (DE) defined for the image. There are three methods for sync input to the AD9889B. See ► Figure 23 for a block diagram of the sync processing capabilities.

Separate Hsync, Vsync, and DE

For this method, all necessary signals are provided so neither Sync generation nor DE generation is required. If desired, the user can adjust the Hsync and Vsync timing relative to DE (refer to Hsync and Vsync adjustment section). Also, the DE timing can be adjusted relative to Hsync and Vsync.

▹ Refer to the *AD9889B Programming Guide* for details on how to adjust the DE and sync timing.

Embedded Syncs (SAV and EAV)

When embedded syncs are provided to the AD9889B Hsync and Vsync need to be generated internally by the AD9889B hardware. Registers 0x30 through 0x34 and 0x17[6:5] contain the settings for Hsync and Vsync generation in the embedded sync decoder section. The AD9889B will use the signal generated by the EAV and SAV as the DE by default, but a new DE can also be generated. Sync adjustment is also available.

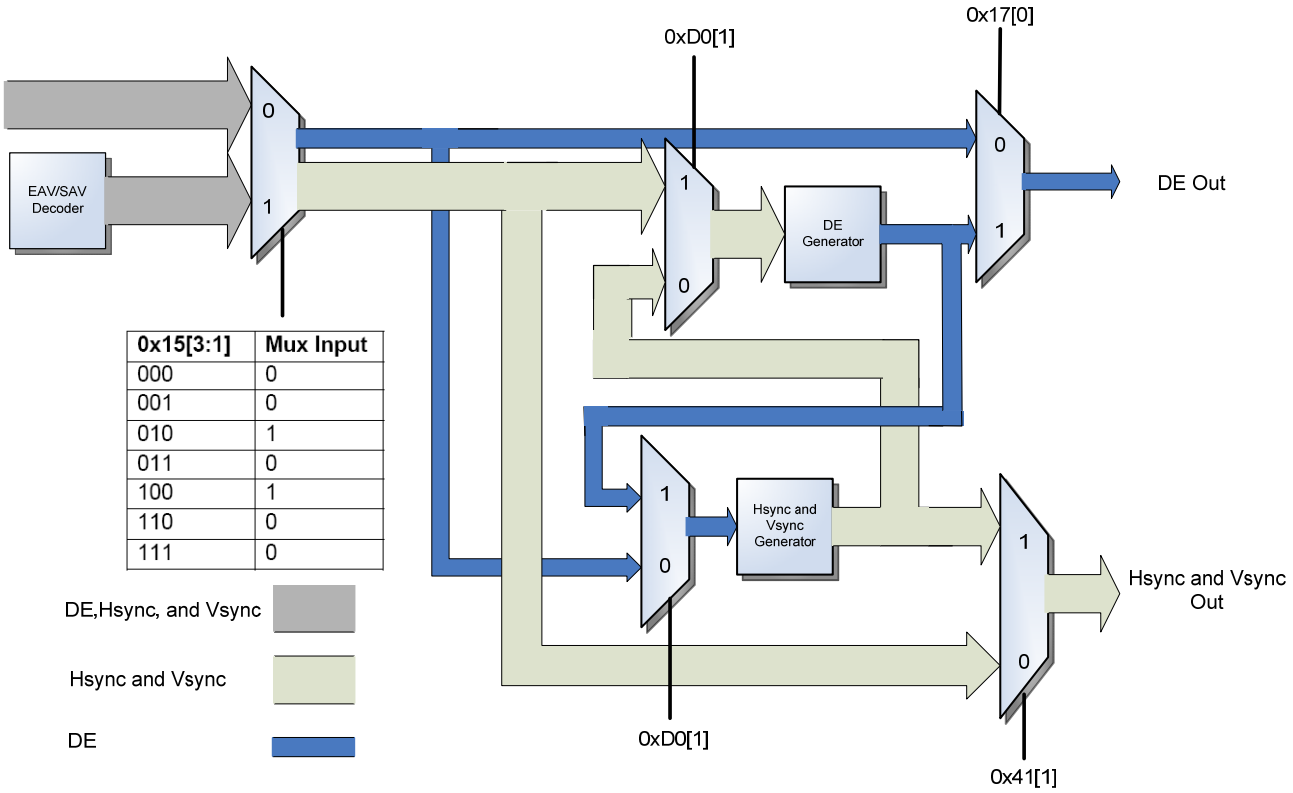
▹ Refer to the *AD9889B Programming Guide* for details on how to program the DE and sync generator when embedded syncs are used.

Separate Hsync and Vsync only

This method requires that a DE be generated. Hsync and Vsync can also be adjusted based on the new DE if desired by enabling the Hsync and Vsync generation and setting the order to DE generation then Hsync Vsync Generation.

▹ Refer to the *AD9889B Programming Guide* for details on how to generate DE based on the incoming sync signals.

Figure 23 Sync Processing Block Diagram



0x15[3:1]	Mux Input
000	0
001	0
010	1
011	0
100	1
110	0
111	0

6.3.2 Color Space Conversion (CSC) Matrix

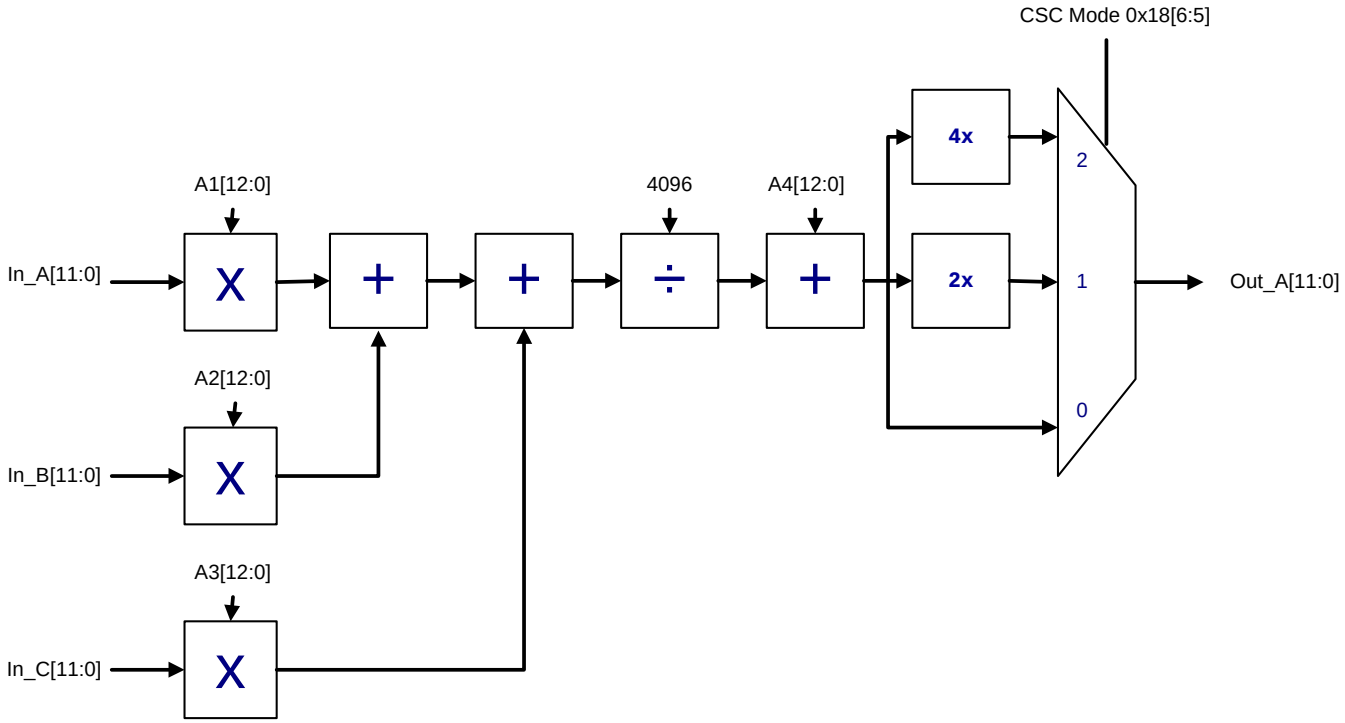
The Color Space Conversion (CSC) matrix in the AD9889B consists of three identical processing channels (see ►Figure 24). In each channel, the three input values (R,G,B or Y,Cr,Cb - see ►Table 11) are multiplied by three separate coefficients. In each CSC channel, the order of input remains the same – Out_A will have the same input (In_A, In_B, In_C) as Out_B and Out_C. The coefficients will be different for each channel. Also included is an offset value for each row of the matrix and a scaling multiple for all values. Each coefficient is 13 bit 2's complement resolution to ensure the signal integrity is maintained. The CSC is designed to run at speeds up to 165Mhz, supporting resolutions up to 1080p at 60Hz and UXGA at 60Hz. With "any-to-any" color space support, formats such as RGB, YUV, YCbCr, and others are supported by the CSC.

▹ Please refer to the *AD9889B Programming Guide* for more information about this block.

Table 11 Channel Assignment for Color Space Converter (CSC)

Input	RGB	YCrCb	Coefficients	Output
In_A	Red	Cr	A1,A2,A3,A4	Out_A
In_B	Green	Y		
In_C	Blue	Cb		
In_A	Red	Cr	B1.B2.B3.B4	Out_B
In_B	Green	Y		
In_C	Blue	Cb		
In_A	Red	Cr	C1,C2,C3,C4	Out_C
In_B	Green	Y		
In_C	Blue	Cb		

Figure 24 Single Channel of CSC (In_A)



6.3.3 4:2:2 to 4:4:4 and 4:4:4 to 4:2:2 Conversion Block

The 4:2:2 to 4:4:4 conversion block can convert 4:2:2 input signals into the 4:4:4 timing format. This is necessary, for instance, if the AD9889B is set in DVI mode and has 4:2:2 format as its video input. The AD9889B is also capable of performing 4:4:4 to 4:2:2 conversions.

▹ Please refer to the *AD9889B Programming Guide* for more information about this block.

6.4 DDC Controller

The AD9889B DDC Controller performs two main functions: to support the system's EDID, and HDCP handling.

- The AD9889B has the ability to read and buffer the sink EDID (one segment of 256 bytes at a time) via the DDC lines. This feature eliminates the requirement for the source controller to interface directly to the sink.

- The AD9889B DDC controller provides the path through which HDCP content protection authentication and communications occur. The AD9889B has internal HDCP key storage (eliminating the need for an external EEPROM) and a built-in micro-controller to handle HDCP transmitter states, including handling down-stream HDCP repeaters. This provides content protection for video which prevents unauthorized digital copying.

▹ Please refer to the *AD9889B Programming Guide* for more information about this block.

6.5 Inter-IC Communications (I2C) Interface

6.5.1 Two-Wire Serial Control Port

The AD9889B registers must be programmed through the SDA and SCL pins using the Inter IC (IIC or I2C) protocol. The SDA/SCL programming address is 0x72 or 0x7A based on whether the PD/AD pin is pulled high (I2C address = 0x7A) or pulled low (I2C address = 0x72). The AD9889B Programming Guide provides the information necessary for programming the transmitter.

Up to two AD9889B devices can be connected to the two-wire serial interface, with a unique address for each device.

▹ The *AD9889B Programming Guide* provides the information necessary for programming the transmitter.

The two-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The AD9889B interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal
- Acknowledge (Ack)

When the serial interface is inactive (SCL and SDA are high), communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a seven-bit slave address (the first seven bits) and a single R/$\overline{W}$ bit (the eighth bit). The R/$\overline{W}$ bit indicates the direction of data transfer: read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the A2 input pin as shown in ► Table 12), the AD9889B acknowledges by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the AD9889B does not acknowledge.

Table 12 Serial Port Addresses

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Hex Addr.
A_6 (MSB)	A_5	A_4	A_3	A_2	A_1	A_0	
0	1	1	1	0	0	1	0x72
0	1	1	1	1	0	1	0x7A

6.5.2 Data Transfer via I2C

For each byte of data read or written, the most significant bit (MSB) is the first bit of the sequence.

If the AD9889B does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9889B during a read sequence, the AD9889B interprets this as end of data. The SDA remains high, so the master can generate a stop signal.

Writing data to specific control registers of the AD9889B requires that the eight-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations, however, it is reset after a STOP command. The base address auto-increments by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address does not increment and remains at its maximum value. Any base address higher than the maximum value does not produce an acknowledge signal.

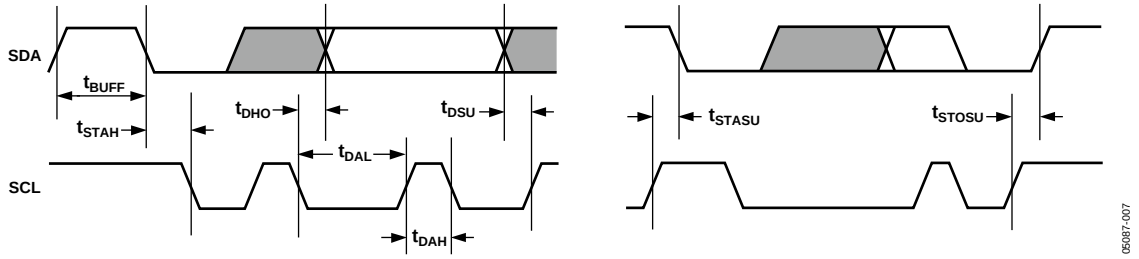
Data are read from the control registers of the AD9889B in a similar manner. Reading requires two data transfer operations:

1. The base address must be written with the R/$\overline{W}$ bit of the slave address byte low to set up a sequential read operation.
2. Reading (the R/$\overline{W}$ bit of the slave address byte high) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the AD9889B, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high. As in the write sequence, a STOP command resets the base address.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read/write) between the slave and master without releasing the serial interface lines.

Figure 25 Serial Port Read/Write Timing



6.5.3 Serial Interface Read/Write Examples

Write to one control register:

- Start signal
- Slave address byte (R/$\overline{W}$ bit = low)
- Base address byte
- Data byte to base address
- Stop signal

Write to four consecutive control registers:

- Start signal
- Slave address byte (R/$\overline{W}$ bit = low)

- Base address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

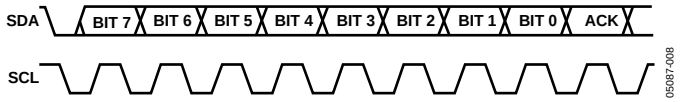
Read from one control register:

- Start signal
- Slave address byte (R/$\overline{W}$ bit = low)
- Base address byte
- Start signal
- Slave address byte (R/$\overline{W}$ bit = high)
- Data byte from base address
- Stop signal

Read from four consecutive control registers:

- Start signal
- Slave address byte (R/$\overline{W}$ bit = low)
- Base address byte
- Start signal
- Slave address byte (R/$\overline{W}$ bit = high)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

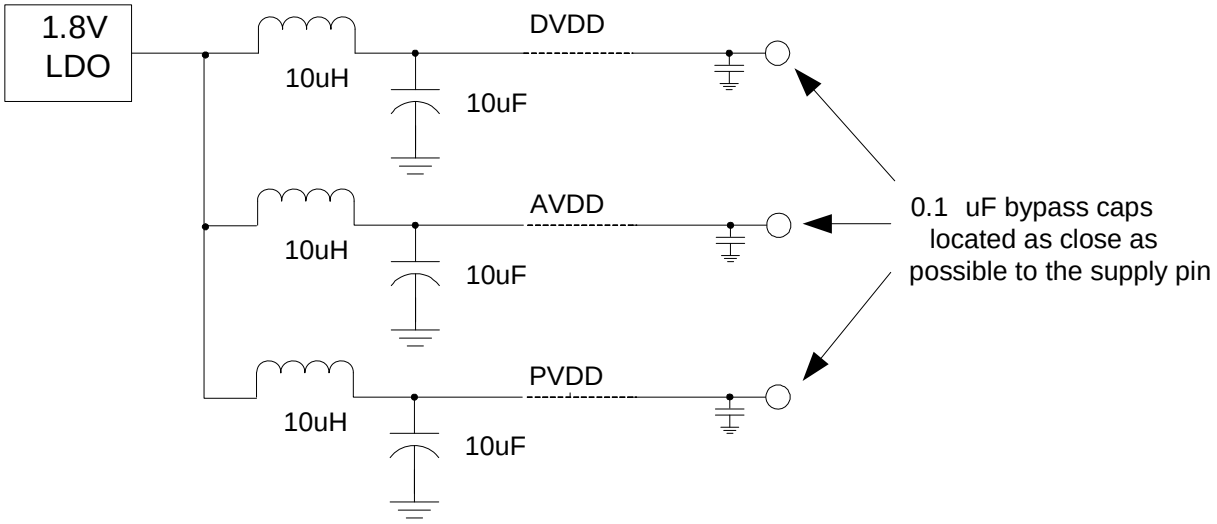
Figure 26 Serial Interface—Typical Byte Transfer



6.6 Power Domains

The AVDD, DVDD and PVDD power domains of the AD9889B operate off of 1.8 volts. It is recommended that the AD9889B has its own designated 1.8V linear regulator and that the AVDD, DVDD and PVDD PCB power domains be segregated using inductors. More detailed recommendations for the PCB can be found in section ► Section 7:.

Figure 27 Power Supply Noise Filter



6.6.1 Power Supply Sequencing

There is no required sequence for turning on or turning off the power domains; all should be fully powered up or down within 1 second of the others.

SECTION 7: PCB LAYOUT RECOMMENDATIONS

7.1 Power Supply Noise Filtering

The DVDD and AVDD power supply domains must remain noise-free for the best operation. The AVDD domain (analog PLL) is more sensitive to noise than the DVDD domain (digital core). Power supply noise has a frequency component that affects performance, and this is specified in Vrms terms. See ► Figure 28 for the maximum allowable noise over frequency. An LC filter on the output of the power supply is recommended to attenuate the noise and should be placed as close to the AD9889B as possible. An effective LC filter for this is a 10 µH inductor and a 10µF capacitor (see► Figure 27). This filter scheme will reduce any noise component over 20KHz to effectively 0. Using the recommended LC filter with realistic load and series resistance yields the transfer curve shown in Figure 29.

Each of the power supply pins of the AD9889B should also have a 0.1uF capacitor connected to the ground plane as shown in ► Figure 27.. The capacitor should be placed as close to the supply pin as possible. Adjacent power pins can share a bypass capacitor. The ground pins of the AD9889B should be connected to the GND plane using vias.

Figure 28 AVDD Max Noise

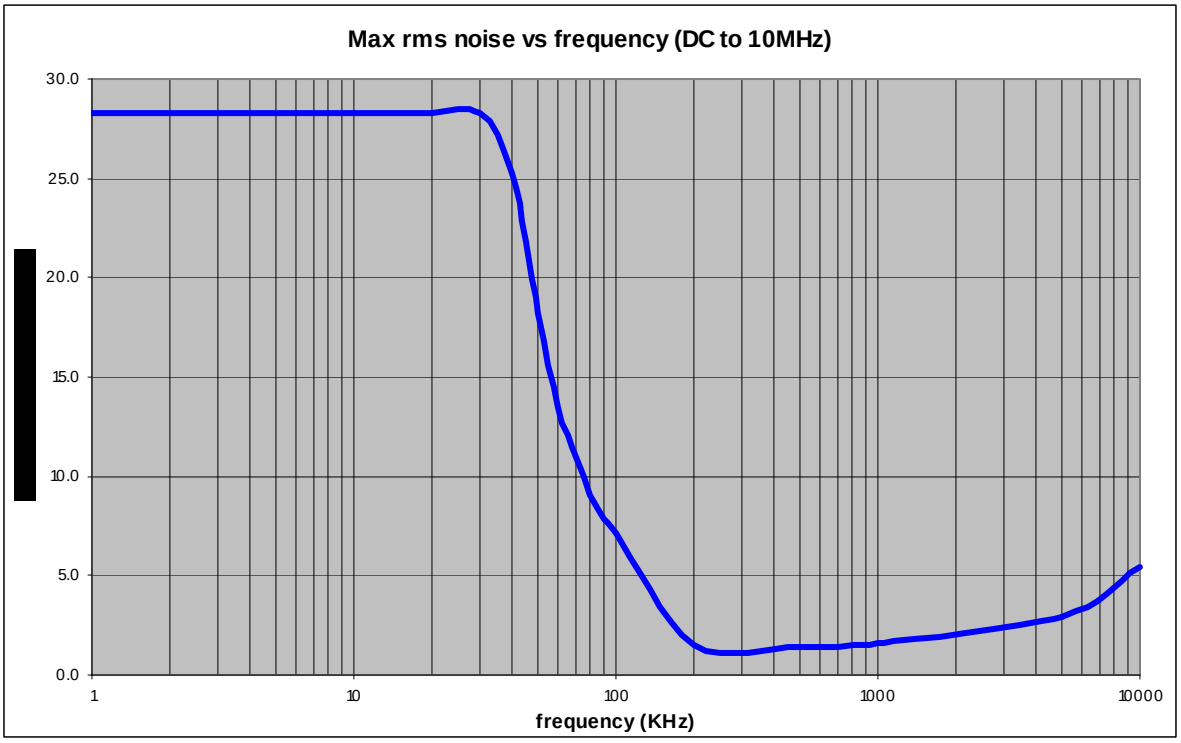
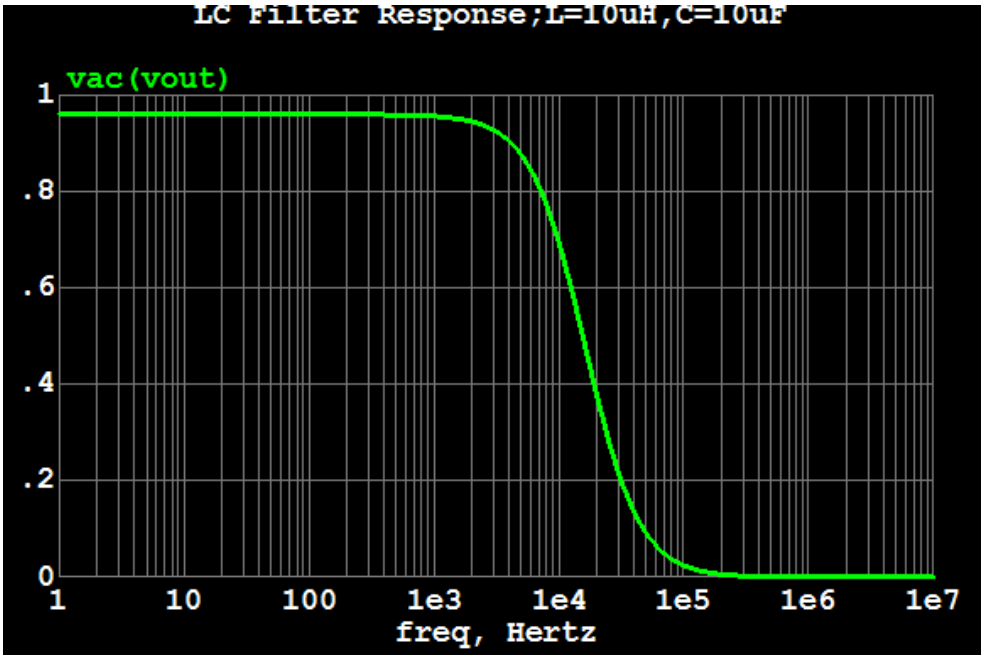


Figure 29 LC Filter Transfer Curve



7.2 Video Clock and Data Inputs

Any noise that that is coupled onto the CLK input trace will add jitter to the system. It is a recommended to control the impedance of the CLK trace. If possible, using a solid ground or supply reference under the trace is a good way to ensure the impedance remains constant over the entire length of the trace. Therefore, minimize the video input data clock (pin 79) trace length and do not run any digital or other high frequency traces near it. Make sure to match the length of the input data signals to optimize data capture especially for Double Data Rate (DDR) input formats.

7.3 Audio Clock and Data Inputs

The length of the input audio data signals should be matched as closely as possible to optimize audio data capture. It is recommended to add series 50Ω resistors (+/-5%) as close as possible to the source of the audio data and clock signals to minimize impedance mismatch.

7.4 SDA and SCL

The SDA and SCL pins should be connected to an I2C Master. A pull-up resistor of 2KΩ (+/-5%) to 1.8V or 3.3V is recommended for each of these signals. See ► Figure 30

7.5 DDCSDA and DDCSCL

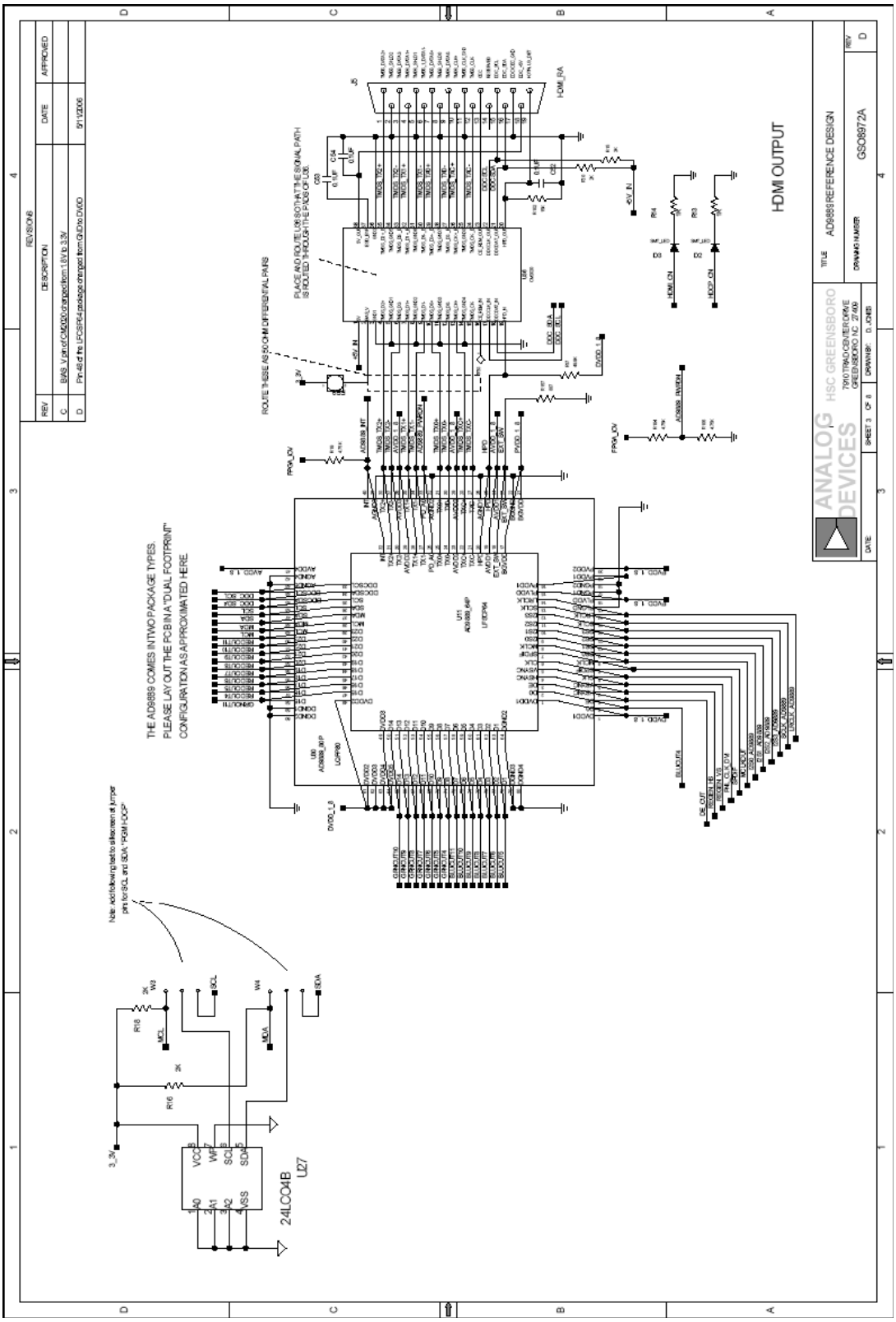
The DDCSDA and DDCSCL pins should be connected to the HDMI connector. A pull-up resistor of 1.5KΩ to 2KΩ (+/-5%) to HDMI +5V is required for each of these signals. See ► Figure 30

7.6 Current Reference Pin: R_EXT

The external reference resistor should be connected between the R_EXT pin and ground with as short a trace as possible. The external reference resistor must have a value of 887 Ohms (+/-1% tolerance). It is strongly recommended to avoid running any high-speed AC or noisy signals next to the R_EXT line or close to it. Specifically it is recommended that no switching signals – such as LRCLK (including vias) be routed close to the R_EXT pin. Low-level TMDS switching noise should have minimal impact on R_EXT.

An example schematic is shown in ► Figure 30. For a complete set of reference schematics and PCB layout example, contact ATV_VideoTX_Apps@analog.com

Figure 30 Example Schematic



SECTION 8: GLOSSARY

480i, 480p, 576i, 576p, 720p, 1080i, 1080p	Common video modes – refer to CEA-861D for more information.
VGA, SVGA, XGA, SXGA, UXGA	Common graphics modes – refer to www.VESA.org for more information.
CSC	Colorspace Convert is used to convert RGB to YCrCb or YCrCb to RGB. Adjustments can be factored in for differing ranges.
CSPBGA	Chip Scale Package Ball Grid Array is one of the package options in which the AD9889B is supplied.
DDC	Display Data Channel is used to communicate between to the source and sink to determine sink capabilities. It is also used as the HDCP key communications channel.
DDR	Double Data Rate clocks capture data on both the rising and falling edge of the clock.
EDID	Enhanced Display Identification is used to store monitor (sink) capabilities in an EEPROM.
HDCP	High-bandwidth Digital Content Protection is a method of protecting content from unauthorized digital copying.
HDMI	High Definition Multimedia Interface is composed of three TMDS differential data channels and one differential clock channel. It is defined to include video streams up to 3.7Gbps as well as audio.
I2C	Inter-IC Communications is a Philips two-wire serial bus for low-speed (up to 400kHz) data.
I2S	Inter-IC Sound is a serial Philips bus designed specifically for audio.
LFCSP	Lead Frame Chip Scale Package is the type of package in which the AD9889B is supplied.
LQFP	Low-profile Quad Flatpack Package is one of the package options in which the AD9889B is supplied.
LPCM	Linear Pulse-Code Modulation is a method of encoding audio samples.
NDA	Non-Disclosure Agreement is used to assure confidentiality of intellectual property.
RGB	Red Green Blue is the standard definition for three-color graphics and video.
TMDS	Transition Minimized Differential Signaling is the format used by the three data channels in HDMI. This encodes 8 bits into 10 and serializes them.
YCrCb	This is a common color format for video where the 'Y' component is luminance and the Cr and Cb signals are color difference signals. 4:4:4 defines a Y, Cr, and Cb for each pixel; 4:2:2 defines a Y for each pixel and a sharing of Cr and Cb between 2 sequential pixels. In this manner, compression of 33% is possible.