

12-Bit + Sign, 5Msps Differential Input ADC with Wide Input Common Mode Range

FEATURES

- 5Msps Throughput Rate
- $\pm 0.25\text{LSB INL (Typ)}$, $\pm 1\text{LSB INL Guaranteed}$
- Guaranteed 12-Bit, No Missing Codes
- $8\text{V}_{\text{P-P}}$ Differential Inputs with Wide Input Common Mode Range
- 73dB SNR (Typ) at $f_{\text{IN}} = 2.2\text{MHz}$
- -85dB THD (Typ) at $f_{\text{IN}} = 2.2\text{MHz}$
- Guaranteed Operation -40°C to 125°C
- Single 3.3V or 5V Supply
- Low Drift ($20\text{ppm}/^{\circ}\text{C Max}$) 2.048V or 4.096V Internal Reference with 1.25V External Reference Input
- 1.8V to 2.5V I/O Voltages
- CMOS or LVDS SPI-Compatible Serial I/O
- Power Dissipation 50mW at $V_{\text{DD}} = 5\text{V}$ (Typ)
- Small 16-Lead (4mm \times 5mm) MSOP Package

APPLICATIONS

- High Speed Data Acquisition Systems
- Communications
- Remote Data Acquisition
- Imaging
- Optical Networking
- Automotive
- Multiphase Motor Control

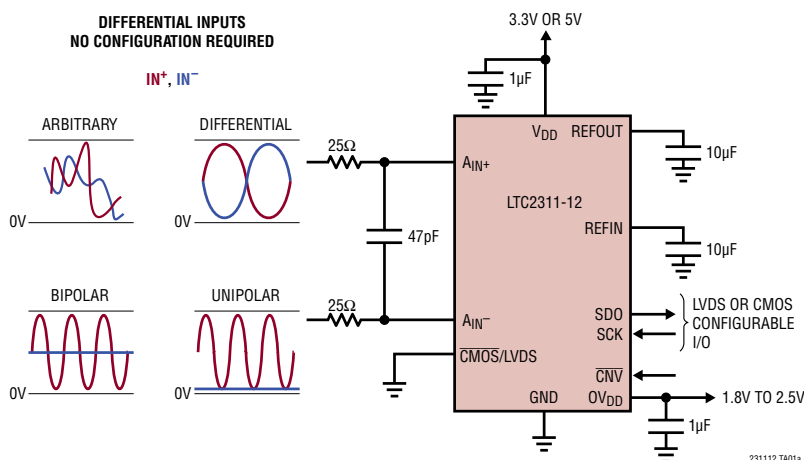
DESCRIPTION

The **LTC[®]2311-12** is a low noise, high speed 12-bit + sign successive approximation register (SAR) ADC with differential inputs and wide input common mode range. Operating from a single 3.3V or 5V supply, the LTC2311-12 has an $8\text{V}_{\text{P-P}}$ differential input range, making it ideal for applications which require a wide dynamic range with high common mode rejection. The LTC2311-12 achieves $\pm 0.25\text{LSB INL}$ typical, no missing codes at 12 bits and 73dB SNR typical.

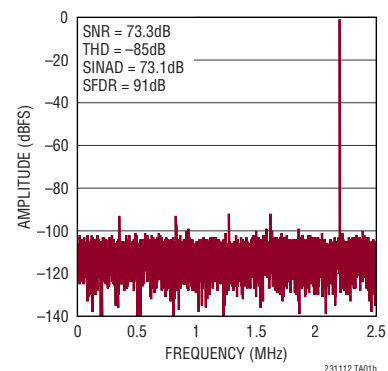
The LTC2311-12 has an onboard low drift ($20\text{ppm}/^{\circ}\text{C max}$) 2.048V or 4.096V temperature compensated reference and provides an external 1.25V buffered reference input. The LTC2311-12 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 5Msps throughput with one-cycle latency makes the LTC2311-12 ideally suited for a wide variety of high speed applications. The LTC2311-12 dissipates only 50mW with a 5V supply and offers nap and sleep modes to reduce the power consumption for further power savings during inactive periods.

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TYPICAL APPLICATION



16k Point FFT $f_{\text{SAMPL}} = 5\text{Msps}$, $f_{\text{IN}} = 2.2\text{MHz}$



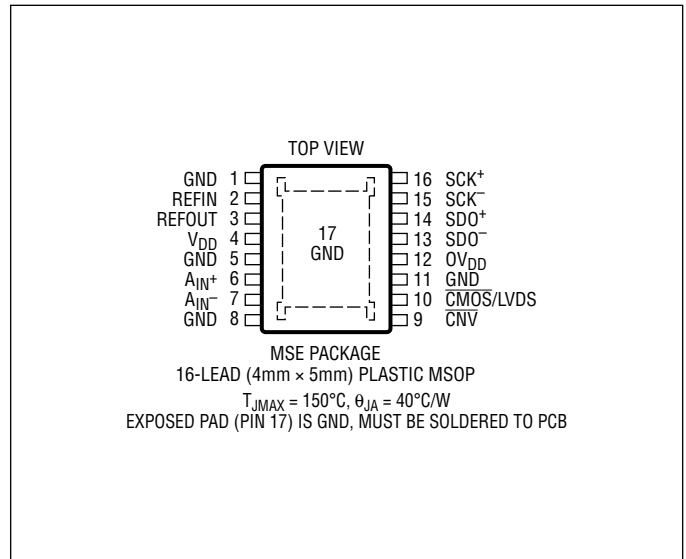
LTC2311-12

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD})	6V
Supply Voltage (OV_{DD})	3V
Analog Input Voltage	
A_{IN+} , A_{IN-} (Note 3)	-0.3V to ($V_{DD} + 0.3V$)
REFIN, REFOUT	-0.3V to ($V_{DD} + 0.3V$)
\overline{CNV} (Note 15)	-0.3V to ($V_{DD} + 0.3V$)
Digital Input Voltage	
(Note 3)	($GND - 0.3V$) to ($OV_{DD} + 0.3V$)
Digital Output Voltage	
(Note 3)	($GND - 0.3V$) to ($OV_{DD} + 0.3V$)
Power Dissipation	200mW
Operating Temperature Range	
LTC2311C	0°C to 70°C
LTC2311I	-40°C to 85°C
LTC2311H	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

<http://www.linear.com/product/LTC2311-12#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2311CMSE-12#PBF	LTC2311CMSE-12#TRPBF	231112	16-Lead Plastic MSOP	0°C to 70°C
LTC2311IMSE-12#PBF	LTC2311IMSE-12#TRPBF	231112	16-Lead Plastic MSOP	-40°C to 85°C
LTC2311HMSE-12#PBF	LTC2311HMSE-12#TRPBF	231112	16-Lead Plastic MSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 4).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN+}	Absolute Input Range (A_{IN+})	(Note 5) ●	0		V_{DD}	V
V_{IN-}	Absolute Input Range (A_{IN-})	(Note 5) ●	0		V_{DD}	V
$V_{IN+} - V_{IN-}$	Input Differential Voltage Range	$V_{IN} = V_{IN+} - V_{IN-}$ ●	-REFOUT		REFOUT	V
V_{CM}	Common Mode Input Range	$V_{IN} = (V_{IN+} + V_{IN-})/2$ ●	0		V_{DD}	V
I_{IN}	Analog Input DC Leakage Current	●	-1		1	μA
C_{IN}	Analog Input Capacitance			10		pF
CMRR	Input Common Mode Rejection Ratio	$f_{IN} = 2.2\text{MHz}$		85		dB
V_{IHCNV}	\overline{CNV} High Level Input Voltage	●	1.3			V
V_{ILCNV}	\overline{CNV} Low Level Input Voltage	●			0.3	V
V_{INCNV}	\overline{CNV} Input Current	$V_{IN} = 0V$ to V_{DD} ●	-10		10	μA

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CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	12			Bits
	No Missing Codes		●	12			Bits
	Transition Noise				0.3		LSB_{RMS}
INL	Integral Linearity Error	(Note 6)	●	-1	± 0.25	1	LSB
DNL	Differential Linearity Error		●	-0.99	± 0.2	0.99	LSB
BZE	Bipolar Zero-Scale Error	(Note 7)	●	-2	0	2	LSB
	Bipolar Zero-Scale Error Drift				0.002		$\text{LSB}/^\circ\text{C}$
FSE	Bipolar Full-Scale Error	$V_{\text{REFOUT}} = 4.096\text{V}$ (REFIN Grounded) (Note 7)	●	-4	± 1	4	LSB
	Bipolar Full-Scale Error Drift	$V_{\text{REFOUT}} = 4.096\text{V}$ (REFIN Grounded)			15		$\text{ppm}/^\circ\text{C}$

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $A_{\text{IN}} = -1\text{dBFS}$ (Notes 4, 8).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	$f_{\text{IN}} = 2.2\text{MHz}$, $V_{\text{REFOUT}} = 4.096\text{V}$, Internal Reference $f_{\text{IN}} = 2.2\text{MHz}$, $V_{\text{REFOUT}} = 5\text{V}$, External Reference	●	70.5	73 73.2		dB dB
SNR	Signal-to-Noise Ratio	$f_{\text{IN}} = 2.2\text{MHz}$, $V_{\text{REFOUT}} = 4.096\text{V}$, Internal Reference $f_{\text{IN}} = 2.2\text{MHz}$, $V_{\text{REFOUT}} = 5\text{V}$, External Reference	●	71	73.3 73.5		dB dB
THD	Total Harmonic Distortion	$f_{\text{IN}} = 2.2\text{MHz}$, $V_{\text{REFOUT}} = 4.096\text{V}$, Internal Reference $f_{\text{IN}} = 2.2\text{MHz}$, $V_{\text{REFOUT}} = 5\text{V}$, External Reference	●		-85 -85	-79	dB dB
SFDR	Spurious Free Dynamic Range	$f_{\text{IN}} = 2.2\text{MHz}$, $V_{\text{REFOUT}} = 4.096\text{V}$, Internal Reference $f_{\text{IN}} = 2.2\text{MHz}$, $V_{\text{REFOUT}} = 5\text{V}$, External Reference	●	79	90 90		dB dB
	-3dB Input Linear Bandwidth	$\text{SNR} - \text{SINAD} \geq 3\text{dB}$			10		MHz
	Aperture Delay				500		ps
	Aperture Jitter				1		ps_{RMS}
	Transient Response	Full-Scale Step			3		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFOUT}	REFOUT Output Voltage	$4.75\text{V} < V_{\text{DD}} < 5.25\text{V}$	●	4.082	4.096	4.110	V
		$3.13\text{V} < V_{\text{DD}} < 3.47\text{V}$	●	2.042	2.048	2.054	V
	REFOUT Input Voltage	$4.75\text{V} < V_{\text{DD}} < 5.25\text{V}$, REFIN = 0V (Note 5)	●	0.5		V_{DD}	V
		$3.13\text{V} < V_{\text{DD}} < 3.47\text{V}$, REFIN = 0V (Note 5)	●	0.5		V_{DD}	V
	REFOUT Temperature Coefficient	(Note 14)	●		3	20	$\text{ppm}/^\circ\text{C}$
	REFOUT Short-Circuit Current	$V_{\text{DD}} = 5.25\text{V}$, Forcing Output to GND	●			30	mA
	REFOUT Line Regulation	$V_{\text{DD}} = 4.75\text{V}$ to 5.25V			0.3		mV/V
	REFOUT Load Regulation	$I_{\text{REFOUT}} < 2\text{mA}$			0.5		mV/mA
	REFOUT Input Resistance (External Reference Mode)	REFIN = 0V			60		k Ω
I_{REFOUT}	REFOUT Input Current (External Reference Mode)	REFIN = 0V, REFOUT = 4.096V (Note 10)			700		μA

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFIN}	REFIN Output Voltage	$3.13\text{V} < V_{\text{DD}} < 3.47\text{V}$ $4.75\text{V} < V_{\text{DD}} < 5.25\text{V}$	● ●	1.245 1.245	1.25 1.25	1.255 1.255	V V
	REFIN Input Voltage	$3.13\text{V} < V_{\text{DD}} < 3.47\text{V}$ (Note 5) $4.75\text{V} < V_{\text{DD}} < 5.25\text{V}$ (Note 5)	● ●	1 1		1.85 1.45	V V
	REFIN Short-Circuit Current	$V_{\text{DD}} = 5.25\text{V}$, Forcing Output to GND	●			250	μA
$V_{\text{IL}} (V_{\text{REFIN}})$	REFIN Low Level Input Voltage (External Reference Mode)	$3.13\text{V} < V_{\text{DD}} < 3.47\text{V}$	●			0.5	V
		$4.75\text{V} < V_{\text{DD}} < 5.25\text{V}$	●			0.5	V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS Digital Inputs and Outputs							
V_{IH}	High Level Input Voltage		●	$0.8 \cdot OV_{\text{DD}}$			V
V_{IL}	Low Level Input Voltage		●			$0.2 \cdot OV_{\text{DD}}$	V
I_{IN}	Digital Input Current	$V_{\text{IN}} = 0\text{V}$ to OV_{DD}	●	-10		10	μA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	$I_{\text{O}} = -500\mu\text{A}$	●	$OV_{\text{DD}} - 0.2$			V
V_{OL}	Low Level Output Voltage	$I_{\text{O}} = 500\mu\text{A}$	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	$V_{\text{OUT}} = 0\text{V}$ to OV_{DD}	●	-10		10	μA
I_{SOURCE}	Output Source Current	$V_{\text{OUT}} = 0\text{V}$			-10		mA
I_{SINK}	Output Sink Current	$V_{\text{OUT}} = OV_{\text{DD}}$			10		mA
LVDS Digital Inputs and Outputs							
V_{ID}	LVDS Differential Input Voltage	100Ω Differential Termination, $OV_{\text{DD}} = 2.5\text{V}$	●	240		600	mV
V_{IS}	LVDS Common Mode Input Voltage	100Ω Differential Termination, $OV_{\text{DD}} = 2.5\text{V}$	●	1		1.45	V
V_{OD}	LVDS Differential Output Voltage	100Ω Differential Load, LVDS Mode, $OV_{\text{DD}} = 2.5\text{V}$	●	100	225	300	mV
V_{OS}	LVDS Common Mode Output Voltage	100Ω Differential Load, LVDS Mode, $OV_{\text{DD}} = 2.5\text{V}$	●	0.85	1.2	1.4	V
$V_{\text{OD_LP}}$	Low Power LVDS Differential Output Voltage	100Ω Differential Load, Low Power, LVDS Mode, $OV_{\text{DD}} = 2.5\text{V}$	●	50	125	200	mV
$V_{\text{OS_LP}}$	Low Power LVDS Common Mode Output Voltage	100Ω Differential Load, Low Power, LVDS Mode, $OV_{\text{DD}} = 2.5\text{V}$	●	0.9	1.2	1.4	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	5V Operation	●	4.75		5.25	V
		3.3V Operation	●	3.13		3.47	V
OV_{DD}	Supply Voltage		●	1.71		2.63	V
I_{VDD}	Supply Current	5Msps Sample Rate ($A_{IN+} = A_{IN-} = 0V$)	●		8.8	12	mA
I_{NAP}	Nap Mode Current	Conversion Done (I_{VDD})	●		2.4	3.5	mA
I_{SLEEP}	Sleep Mode Current	$V_{DD} = 3.3V$, Sleep Mode ($I_{VDD} + I_{OVDD}$)	●		0.1	10	μA

CMOS I/O Mode

I_{OVDD}	Supply Current	5Msps Sample Rate ($C_L = 5pF$)	●		1.1	1.5	mA
$P_{D_3.3V}$	Power Dissipation	$V_{DD} = 3.3V$ 5Msps Sample Rate ($A_{IN+} = A_{IN-} = 0V$)			27		mW
	Nap Mode	$V_{DD} = 3.3V$ Conversion Done ($I_{VDD} + I_{OVDD}$)			7.5		mW
	Sleep Mode	$V_{DD} = 3.3V$ Sleep Mode ($I_{VDD} + I_{OVDD}$)			0.3		μW
P_{D_5V}	Power Dissipation	$V_{DD} = 5V$ 5Msps Sample Rate ($A_{IN+} = A_{IN-} = 0V$)	●		50	65	mW
	Nap Mode	$V_{DD} = 5V$ Conversion Done ($I_{VDD} + I_{OVDD}$)	●		12	18	mW
	Sleep Mode	$V_{DD} = 5V$ Sleep Mode ($I_{VDD} + I_{OVDD}$)	●		0.5	30	μW

LVDS I/O Mode

I_{OVDD}	Supply Current	5Msps Sample Rate ($R_L = 100\Omega$)	●		2.5	3.5	mA
$P_{D_3.3V}$	Power Dissipation	$V_{DD} = 3.3V$ 5Msps Sample Rate ($A_{IN+} = A_{IN-} = 0V$)			33		mW
	Nap Mode	$V_{DD} = 3.3V$ Conversion Done ($I_{VDD} + I_{OVDD}$)			14		mW
	Sleep Mode	$V_{DD} = 3.3V$ Sleep Mode ($I_{VDD} + I_{OVDD}$)			0.3		μW
P_{D_5V}	Power Dissipation	$V_{DD} = 5V$ 5Msps Sample Rate ($A_{IN+} = A_{IN-} = 0V$)	●		58	65	mW
	Nap Mode	$V_{DD} = 5V$ Conversion Done ($I_{VDD} + I_{OVDD}$)	●		18	25	mW
	Sleep Mode	$V_{DD} = 5V$ Sleep Mode ($I_{VDD} + I_{OVDD}$)	●		0.5	20	μW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS, LVDS I/O Modes							
f_{SMPL}	Maximum Sampling Frequency		●			5	Msps
t_{CYC}	Time Between Conversions	(Note 11)	●	200		1000000	ns
t_{ACQ}	Acquisition Time	(Note 11)	●	38.1			ns
t_{CONV}	Conversion Time		●	161.9			ns
t_{CNVH}	\overline{CNV} High Time		●	25			ns
$t_{DCNVSKL}$	SCK Quiet Time from $\overline{CNV} \downarrow$	(Note 11)	●	10			ns
$t_{DSCKLCNVH}$	SCK Delay Time to $\overline{CNV} \uparrow$	(Note 11)	●	20			ns
t_{SCK}	SCK Period	(Notes 12, 13)	●	9.4			ns
t_{SCKH}	SCK High Time		●	4			ns
t_{SCKL}	SCK Low Time		●	4			ns

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 4).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{DSCKSDOV}	SDO Data Valid Delay from $\text{SCK}\downarrow$	$C_L = 5\text{pF}$ (Note 11) ●		4	7.4	ns
t_{HSDO}	SDO Data Remains Valid Delay from $\text{SCK}\downarrow$	$C_L = 5\text{pF}$ (Note 11) ●	2			ns
t_{DCNVSDOV}	SDO Data Valid Delay from $\overline{\text{CNV}}\downarrow$	$C_L = 5\text{pF}$ (Note 11) ●		2.5	5	ns
t_{DCNVSDOZ}	Bus Relinquish Time After $\overline{\text{CNV}}\uparrow$	(Note 11) ●			5	ns
t_{WAKE}	REFOUT Wake-Up Time	$C_{\text{REFOUT}} = 10\mu\text{F}$		10		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground, or above V_{DD} or OV_{DD} , they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground, or above V_{DD} or OV_{DD} , without latch-up.

Note 4: $V_{\text{DD}} = 5\text{V}$, $\text{OV}_{\text{DD}} = 2.5\text{V}$, $\text{REFOUT} = 4.096\text{V}$, $f_{\text{SAMPL}} = 5\text{MHz}$.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero error is the offset voltage measured from -0.5LSB when the output code flickers between 0 0000 0000 0000 and 1 1111 1111 1111. Full-scale bipolar error is the worst-case of $-\text{FS}$ or $+\text{FS}$

untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 8: All specifications in dB are referred to a full-scale $\pm 4.096\text{V}$ input with $\text{REFOUT} = 4.096\text{V}$.

Note 9: When REFOUT is overdriven, the internal reference buffer must be turned off by setting $\text{REFIN} = 0\text{V}$.

Note 10: $f_{\text{SAMPL}} = 5\text{MHz}$, I_{REFOUT} varies proportionally with sample rate.

Note 11: Guaranteed by design, not subject to test.

Note 12: Parameter tested and guaranteed at $\text{OV}_{\text{DD}} = 1.71\text{V}$ and $\text{OV}_{\text{DD}} = 2.5\text{V}$.

Note 13: t_{SCK} of 9.4ns minimum allows a shift clock frequency up to 105MHz for falling edge capture.

Note 14: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 15: $\overline{\text{CNV}}$ is driven from a low jitter digital source, typically at OV_{DD} logic levels. This input pin has a TTL style input that will draw a small amount of current.

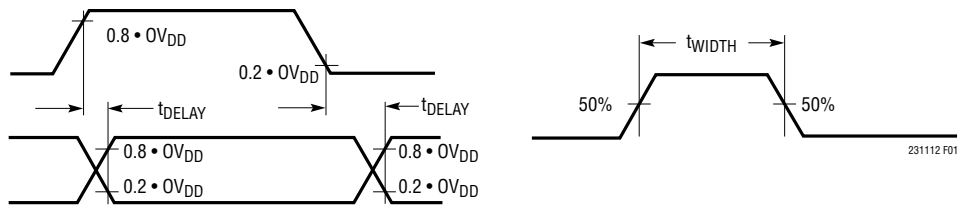
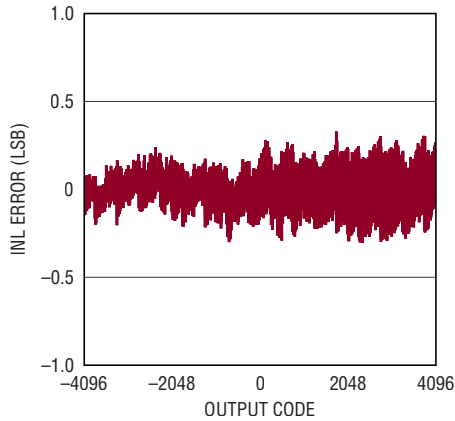
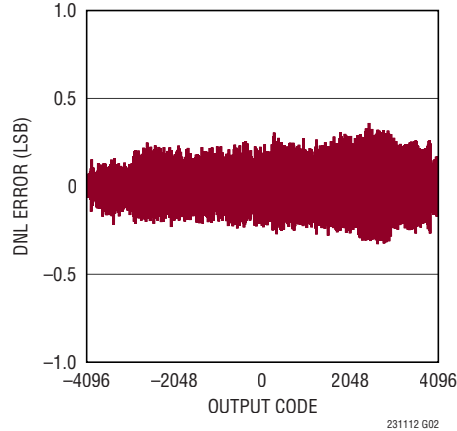
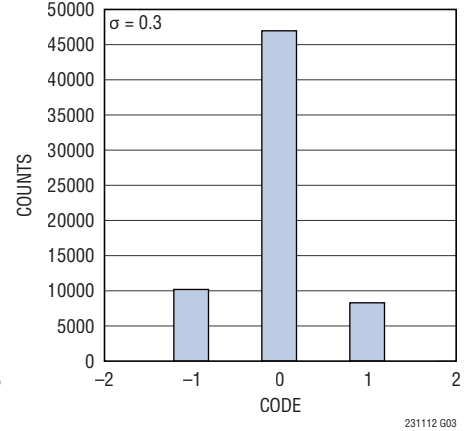
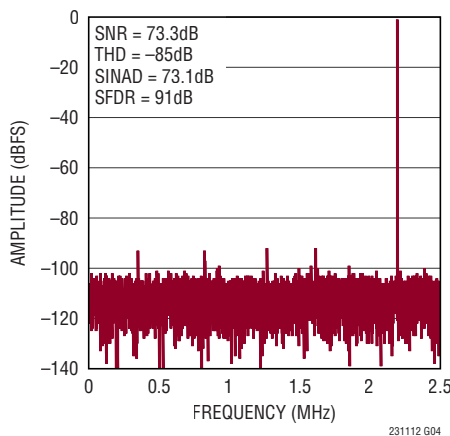
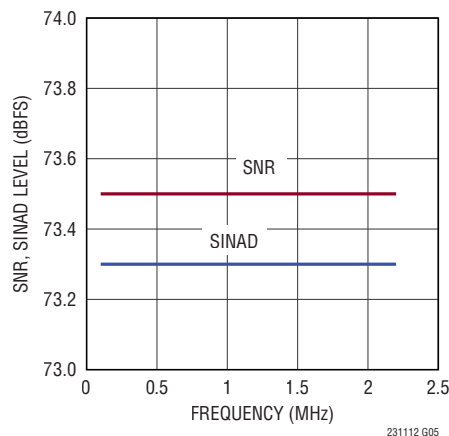
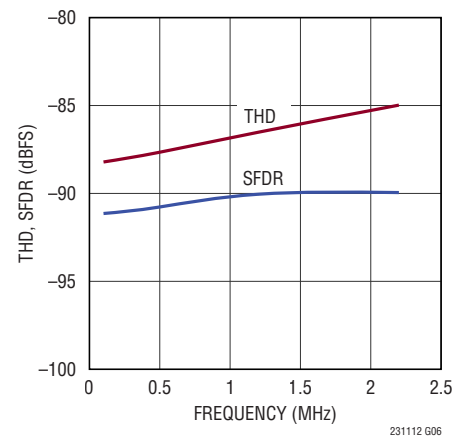
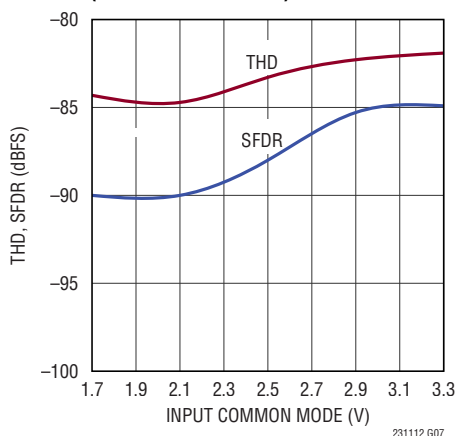
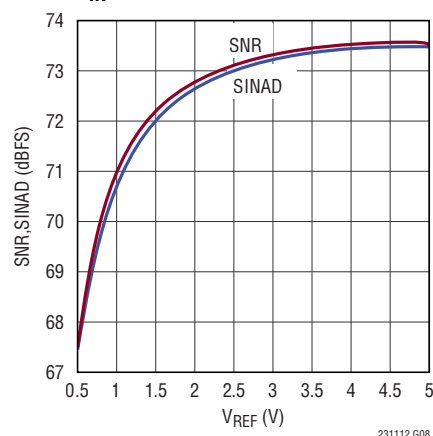
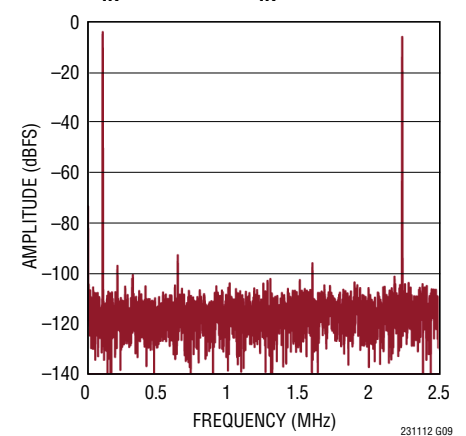


Figure 1. Voltage Levels for Timing Specifications

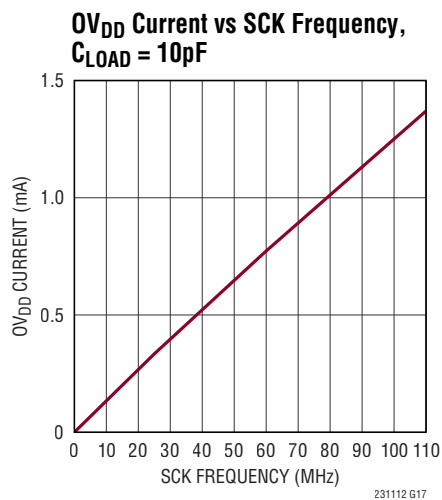
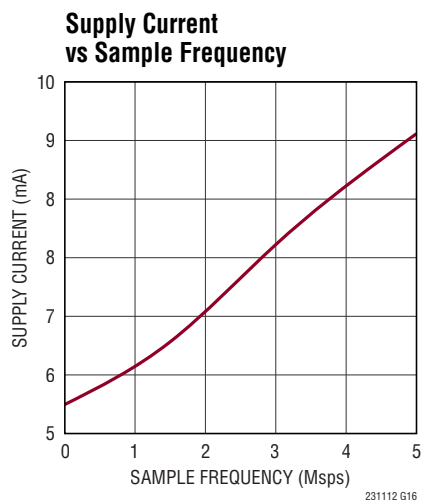
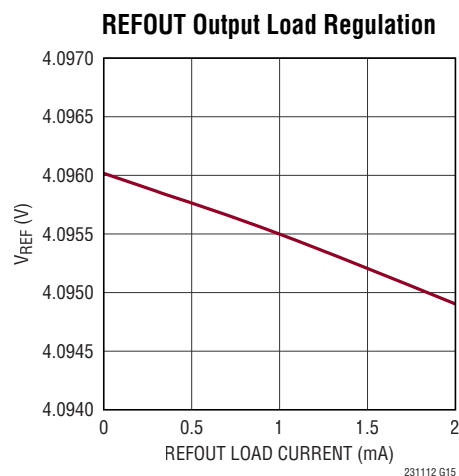
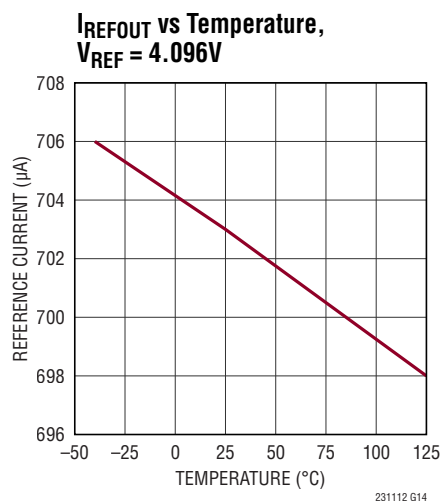
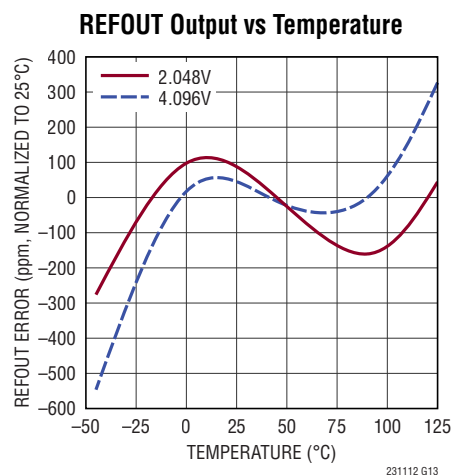
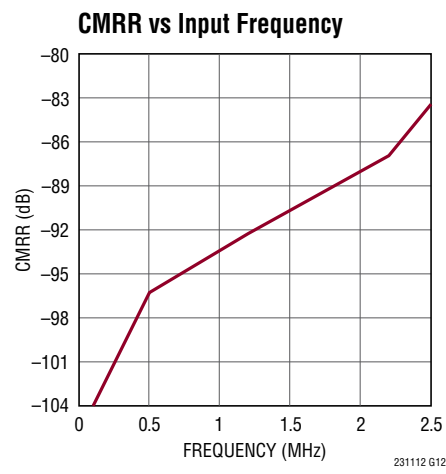
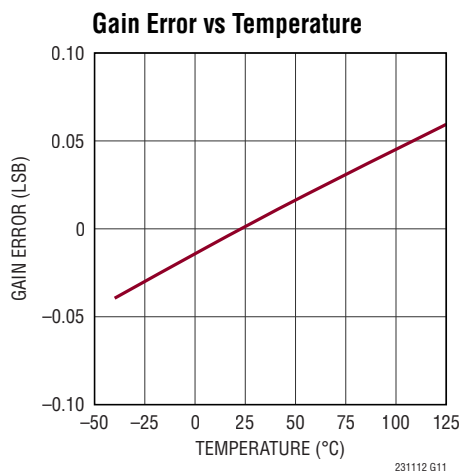
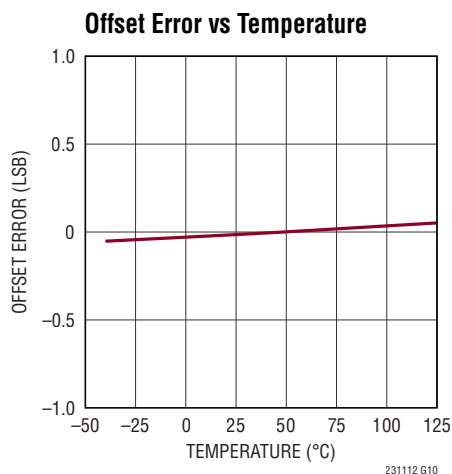
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $0V_{DD} = 2.5\text{V}$, $REF_{OUT} = 4.096\text{V}$, $f_{SAMPL} = 5\text{Mps}$, unless otherwise noted.

Integral Nonlinearity vs Output Code**Differential Nonlinearity vs Output Code****DC Histogram for 64k Samples****16k Point FFT, $f_{SAMPL} = 5\text{Mps}$, $f_{IN} = 2.2\text{MHz}$** **SNR, SINAD vs Input Frequency (100kHz to 2.2MHz)****THD, SFDR Input Frequency (100kHz to 2.2MHz)****THD, SFDR vs Input Common Mode (100kHz to 2.2MHz)****SNR, SINAD vs Reference Voltage, $f_{IN} = 500\text{kHz}$** **8k Point FFT, IMD, $f_{SAMPL} = 5\text{Mps}$, $A_{IN}^+ = 100\text{kHz}$, $A_{IN}^- = 2.2\text{MHz}$** 

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $0V_{DD} = 2.5\text{V}$, $REF_{OUT} = 4.096\text{V}$, $f_{SAMPL} = 5\text{Msps}$, unless otherwise noted.



PIN FUNCTIONS

GND (Pins 1, 5, 8, 11): Ground. These pins and the exposed pad (Pin 17) must be tied directly to a solid ground plane.

REFIN (Pin 2): Reference Buffer 1.25V Input/Output. An onboard buffer nominally outputs 1.25V to this pin. This pin should be decoupled closely to the pin (no vias) with a 10 μ F (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be overdriven with an external reference. The REFIN pin, when pulled to GND disables the REFOUT pin buffer allowing an external reference to drive REFOUT directly.

REFOUT (Pin 3): Reference Buffer Output. An onboard buffer nominally outputs 4.096V to this pin. This pin should be decoupled closely to the pin (no vias) with a 10 μ F (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFIN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to V_{DD} .

V_{DD} (Pin 4): Power Supply. Bypass V_{DD} to GND with a 1 μ F ceramic capacitor close to the V_{DD} pin.

A_{IN}^+ , A_{IN}^- (Pins 6, 7): Analog Differential Input Pins. Full-scale range (A_{IN}^+ to A_{IN}^-) is \pm REFOUT voltage. These pins can be driven from V_{DD} to GND.

\overline{CNV} (Pin 9): Convert Input. This pin, when high, defines the sampling phase. When this pin is driven low, the conversion phase is initiated and output data is clocked out. This input pin is a TTL style input typically driven at OV_{DD} levels with a low jitter pulse, but it is bound to V_{DD} levels. This pin is unaffected by the $\overline{CMOS}/LVDS$ pin.

$\overline{CMOS}/LVDS$ (Pin 10): I/O mode select. Ground this pin to enable CMOS mode, tie to OV_{DD} to enable LVDS mode. Float this pin to enable low power LVDS mode.

OV_{DD} (Pin 12): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 2.5V. This supply is nominally set to the same supply as the host interface (CMOS: 1.8V or 2.5V, LVDS: 2.5V). Bypass OV_{DD} to GND with a 1 μ F ceramic capacitor close to the OV_{DD} pin.

Exposed Pad (Pin 17): Ground. Solder this pad to ground.

CMOS I/O Mode

SDO^+ (Pin 14): Serial Data Output. The conversion result is shifted MSB first on each falling edge of SCK. The result is output on SDO^+ . The logic level is determined by OV_{DD} . Do not connect SDO^- . (Pin 13)

SCK^+ (Pin 16): Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins. Drive SCK^+ with a single-ended clock. The logic level is determined by OV_{DD} . Do not connect SCK^- . (Pin 15)

LVDS I/O Mode

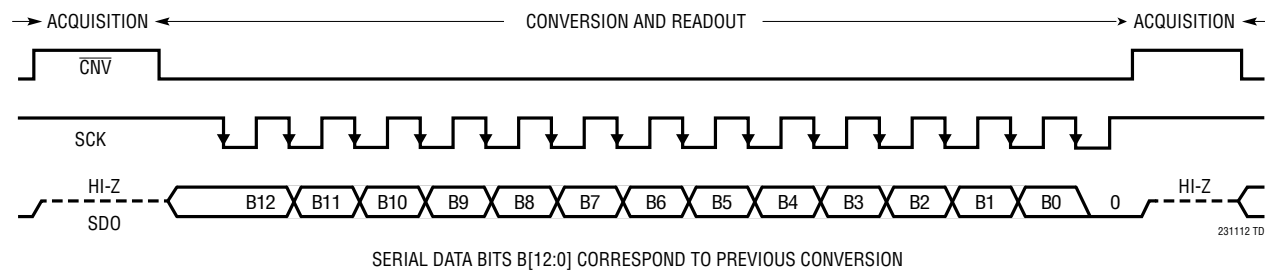
SDO^+ , SDO^- (Pins 14, 13): Serial Data Output. The conversion result is shifted MSB first on each falling edge of SCK. The result is output differentially on SDO^+ and SDO^- . These pins must be differentially terminated by an external 100 Ω resistor at the receiver (FPGA).

SCK^+ , SCK^- (Pins 16, 15): Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins. Drive SCK^+ and SCK^- with a differential clock. These pins must be differentially terminated by an external 100 Ω resistor at the receiver (ADC).

Block diagram of the AD7124 24-bit SAR ADC. The diagram shows the internal components and their connections to the package pins. Key components include a 13-bit SAR ADC, a timing control logic, LVDS/CMOS tri-state serial output, and LVDS/CMOS receivers. Power and ground connections are shown at the top and bottom. The diagram is labeled "231112 BDa" at the bottom right.

TIMING DIAGRAM

CMOS, LVDS I/O Modes



APPLICATIONS INFORMATION

OVERVIEW

The LTC2311-12 is a low noise, high speed 12-bit + sign successive approximation register (SAR) ADC with differential inputs and a wide input common mode range. Operating from a single 3.3V or 5V supply, the LTC2311-12 has an 8V_{P-P} differential input range, making it ideal for applications which require a wide dynamic range. The LTC2311-12 achieves $\pm 0.25\text{LSB}$ INL typical, no missing codes at 12 bits and 73dB SNR typical.

The LTC2311-12 has an onboard reference buffer and low drift (20ppm/°C max) 4.096V temperature-compensated reference. The LTC2311-12 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 5Msps throughput with one-cycle latency makes the LTC2311-12 ideally suited for a wide variety of high speed applications. The LTC2311-12 dissipates only 50mW operating at a 5V supply. Nap and sleep modes are also provided to reduce the power consumption of the LTC2311-12 during inactive periods for further power savings.

CONVERTER OPERATION

The LTC2311-12 operates in two phases. During the acquisition phase, the sample capacitor is connected to the analog input pins A_{IN+} and A_{IN-} to sample the differential analog input voltage, as shown in Figure 3. A falling edge on the $\overline{\text{CNV}}$ pin initiates a conversion. During the conversion phase, the 13-bit CDAC is sequenced through a successive approximation algorithm for each input SCK pulse, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g., $V_{\text{REFOUT}}/2$, $V_{\text{REFOUT}}/4$... $V_{\text{REFOUT}}/8192$) using a differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 13-bit digital output code for serial transfer. The MSB of the 13-bit two's complement output indicates the sign of the differential analog input voltage.

TRANSFER FUNCTION

The LTC2311-12 transfer function provides 13 bits of resolution across the full span of $2 \bullet \text{REFOUT}$, as shown in Figure 2. If the analog input spans less than this full-scale, such as in the case of pseudo-differential drive, the

ADC provides 12 bits of resolution across this reduced span, with the additional benefit of digitizing over and underrange conditions, as shown in Table 1.

The LTC2311-12 digitizes the full-scale voltage of $2 \bullet \text{REFOUT}$ into 2^{13} levels, resulting in an LSB size of 1mV with $\text{REFOUT} = 4.096\text{V}$. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format. When driven by fully differential inputs, the transfer function spans 2^{13} codes. When driven by pseudo differential inputs, the transfer function spans 2^{12} codes.

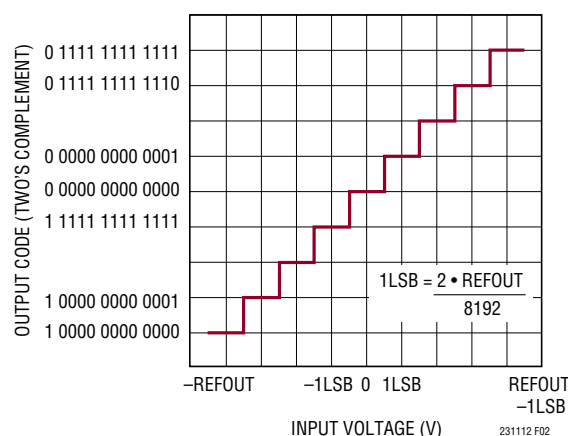


Figure 2. LTC2311-12 Transfer Function

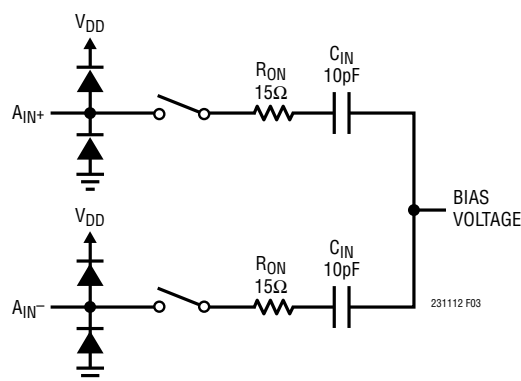


Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2311-12

APPLICATIONS INFORMATION

Table 1: Code Ranges for the Analog Input Operational Modes

MODE	SPAN ($V_{IN+} - V_{IN-}$)	MIN CODE	MAX CODE
Fully Differential	–REFOUT to +REFOUT	1 0000 0000 0000	0 1111 1111 1111
Pseudo-Differential Bipolar	–REFOUT/2 to +REFOUT/2	11 000 0000 0000	00 111 1111 1111
Pseudo-Differential Unipolar	0 to REFOUT	0 0000 0000 0000	0 1111 1111 1111

Analog Input

The differential inputs of the LTC2311-12 provide great flexibility to convert a wide variety of analog signals with no configuration required. The LTC2311-12 digitizes the difference voltage between the A_{IN+} and A_{IN-} pins while supporting a wide common mode input range. The analog input signals can have an arbitrary relationship to each other, provided that they remain between V_{DD} and GND. The LTC2311-12 can also digitize more limited classes of analog input signals such as pseudo-differential unipolar/bipolar and fully differential with no configuration required.

The analog inputs of the LTC2311-12 can be modeled by the equivalent circuit shown in Figure 3. The back-to-back diodes at the inputs form clamps that provide ESD protection. In the acquisition phase, 10pF (C_{IN}) from the sampling capacitor in series with approximately 15 Ω (R_{ON}) from the on-resistance of the sampling switch is connected to the input. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC sampler. The inputs of the ADC core draw a small current spike while charging the C_{IN} capacitors during acquisition.

Single-Ended Signals

Single-ended signals can be directly digitized by the LTC2311-12. These signals should be sensed pseudo-differentially for improved common mode rejection. By connecting the reference signal (e.g., ground sense) of the main analog signal to the other A_{IN} pin, any noise or disturbance common to the two signals will be rejected by the high CMRR of the ADC. The LTC2311-12 flexibility handles both pseudo-differential unipolar and bipolar sig-

nals, with no configuration required. The wide common mode input range relaxes the accuracy requirements of any signal conditioning circuits prior to the analog inputs.

Pseudo-Differential Bipolar Input Range

The pseudo-differential bipolar configuration represents driving one of the analog inputs at a fixed voltage, typically $V_{REF}/2$, and applying a signal to the other A_{IN} pin. In this case the analog input swings symmetrically around the fixed input yielding bipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 4, and the corresponding transfer function in Figure 5. The fixed analog input pin need not be set at $V_{REF}/2$, but at some point within the V_{DD} rails allowing the alternate input to swing symmetrically around this voltage. If the input signal ($A_{IN+} - A_{IN-}$) swings beyond $\pm\text{REFOUT}/2$, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

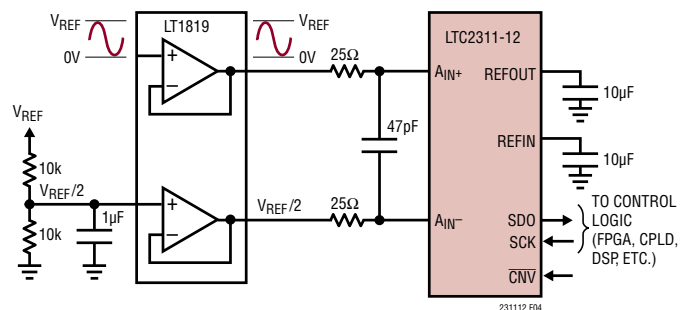


Figure 4. Pseudo-Differential Bipolar Application Circuit

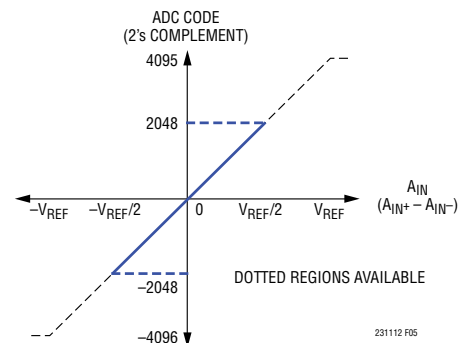


Figure 5. Pseudo-Differential Bipolar Transfer Function

APPLICATIONS INFORMATION

Pseudo-Differential Unipolar Input Range

The pseudo-differential unipolar configuration represents driving one of the analog inputs at ground and applying a signal to the other A_{IN} pin. In this case, the analog input swings between ground and V_{REF} yielding unipolar two's

complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 6, and the corresponding transfer function in Figure 7. If the input signal ($A_{IN+} - A_{IN-}$) swings negative, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

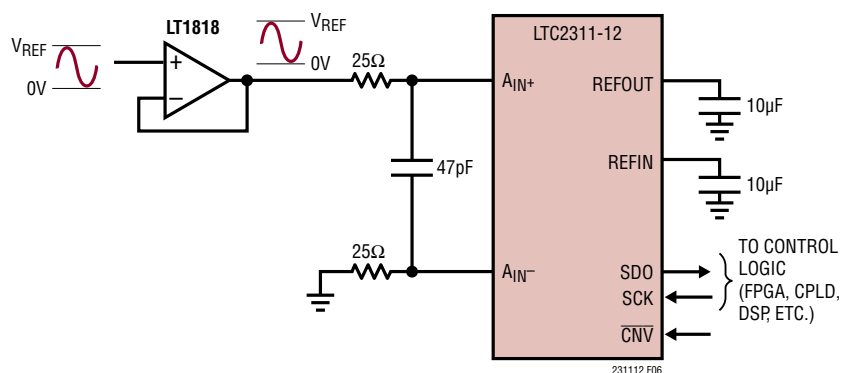


Figure 6. Pseudo-Differential Unipolar Application Circuit

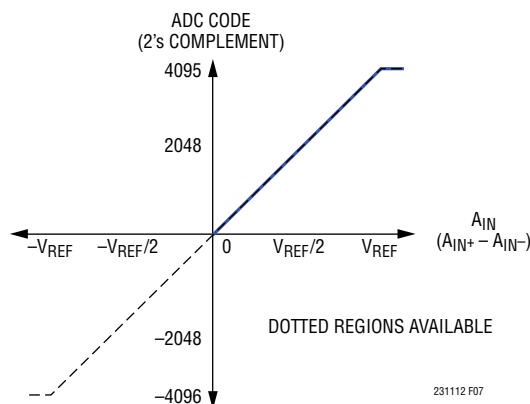


Figure 7. Pseudo-Differential Unipolar Transfer Function

APPLICATIONS INFORMATION

Single-Ended-to-Differential Conversion

While single-ended signals can be directly digitized as previously discussed, single-ended to differential conversion circuits may also be used when higher dynamic range is desired. By producing a differential signal at the inputs of the LTC2311-12, the signal swing presented to the ADC is maximized, thus increasing the achievable SNR.

The LT[®]1819 high speed dual operational amplifier is recommended for performing single-ended-to-differential conversions, as shown in Figure 8. In this case, the first amplifier is configured as a unity-gain buffer and the single-ended input signal directly drives the high impedance input of this amplifier.

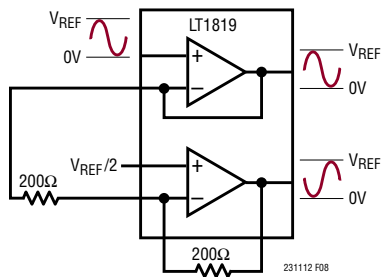


Figure 8. Single-Ended to Differential Driver

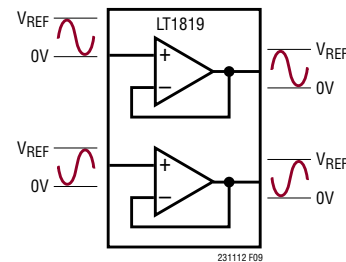


Figure 9. LT1819 Buffering a Fully-Differential Signal Source

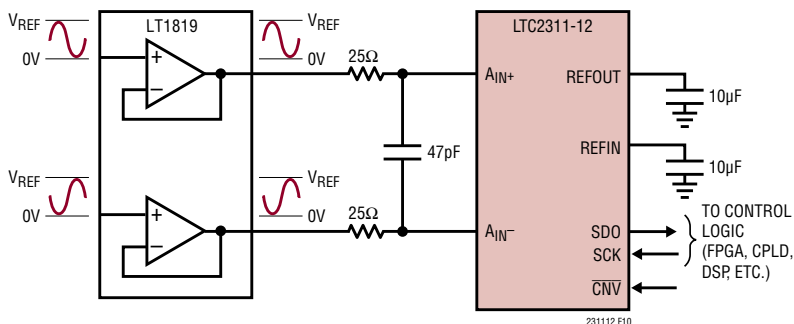


Figure 10. Fully-Differential Application Circuit

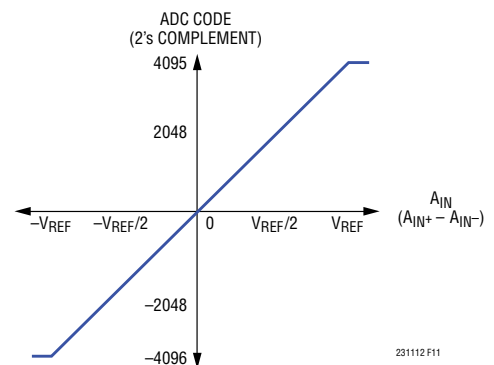


Figure 11. Fully-Differential Transfer Function

APPLICATIONS INFORMATION

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2311-12 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC inputs, because the ADC inputs draw a current spike at the start of the acquisition phase.

For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2311-12. The amplifier provides low output impedance to minimize gain error and allow for fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs, which draw a small current spike during acquisition.

Input Filtering

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with a low bandwidth filter to minimize noise. The simple 1-pole RC lowpass filter shown in Figure 12 is sufficient for many applications.

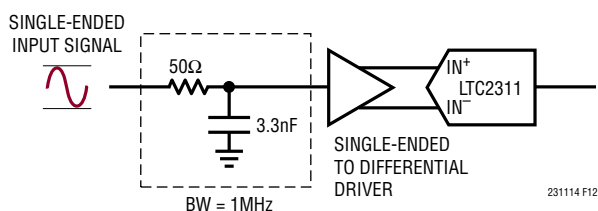


Figure 12. Input Signal Chain

Sampling switch on-resistance (R_{ON}) and the sample capacitor (C_{IN}) form a second lowpass filter that limits the input bandwidth to the ADC core to 110MHz. A buffer amplifier with a low noise density must be selected to minimize the degradation of the SNR over this bandwidth.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

ADC REFERENCE

Internal Reference

The LTC2311-12 has an on-chip, low noise, low drift (20ppm/°C max), temperature compensated bandgap reference that is internally buffered and is available at REFIN (Pin 2). The internal reference buffer gains the REFIN pin voltage (1.25V) to REFOUT (pin 3) and is 4.096V for a 5V supply and 2.048V for a 3.3V supply. Bypass REFOUT to GND with a 10μF (X5R, 0805 size) ceramic capacitor. The 10μF capacitor should be soldered as close as possible to the REFOUT pin to minimize wiring inductance. The REFIN pin produces a 1.25V precision reference which should also be bypassed with a 10μF (X5R, 0805 size) ceramic capacitor. The REFIN pin may be overdriven with an external precision reference as shown in Figure 13a.

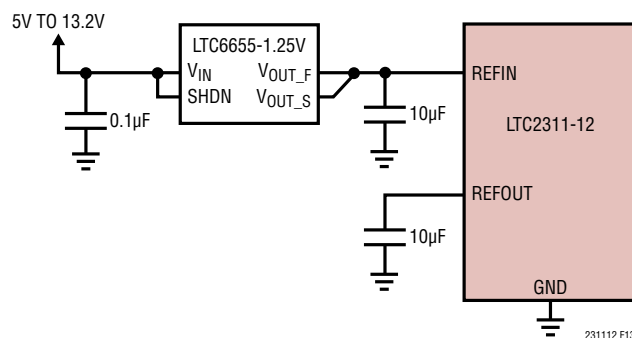


Figure 13a. LTC2311-12 with an External REFIN Voltage

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Table 1. Internal Reference with Internal Buffer

V _{DD}	REFIN	REFOUT	FULLY DIFFERENTIAL INPUT RANGE	UNIPOLAR INPUT RANGE	BIPOLAR INPUT RANGE
5V	1.25V	4.096V	±4.096V	0V to 4.096V	±2.048V
3.3V	1.25V	2.048V	±2.048V	0V to 2.048V	±1.024V

Table 2. External Reference with Internal Buffer

V _{DD}	REFIN (OVER-DRIVEN)	REFOUT	FULLY DIFFERENTIAL INPUT RANGE	UNIPOLAR INPUT RANGE	BIPOLAR INPUT RANGE
5V	1V	3.3V	±3.3V	0V to 3.3V	±1.65V
	1.25V	4.096V	±4.096V	0V to 4.096V	±2.048V
	1.45V	4.7V	±4.7V	0V to 4.7V	±2.35V
3.3V	1V	1.65V	±1.65V	0V to 1.65V	±0.825V
	1.25V	2.048V	±2.048V	0V to 2.048V	±1.024V
	1.85V	3V	±3V	0V to 3V	±1.5V

Table 3. External Reference Unbuffered

V _{DD}	REFIN	REFOUT	FULLY DIFFERENTIAL INPUT RANGE	UNIPOLAR INPUT RANGE	BIPOLAR INPUT RANGE
5V	0V	0.5V	±0.5V	0V to 0.5V	±0.25V
	0V	5V	±5V	0V to 5V	±2.5V
3.3V	0V	0.5V	±0.5V	0V to 0.5V	±0.25V
	0V	3.3V	±3.3V	0V to 3.3V	±1.65V

External Reference

The internal reference buffer can also be overdriven from 1.25V to 5V with an external reference at REFOUT as shown in Figure 13b. In this configuration, REFIN must be grounded to disable the internal reference buffer. A 55kΩ internal resistance loads the REFOUT pin when the reference buffer is disabled. To maximize the input signal swing and corresponding SNR, the LTC6655-5 is recommended when overdriving REFOUT. The LTC6655-5 offers the same small size, accuracy, drift and extended temperature range as the LTC6655-4.096. By using a 5V reference, a higher SNR can be achieved. We recommend bypassing the LTC6655-5 with a 10μF ceramic capacitor (X5R, 0805 size) as close as possible to the REFOUT pin.

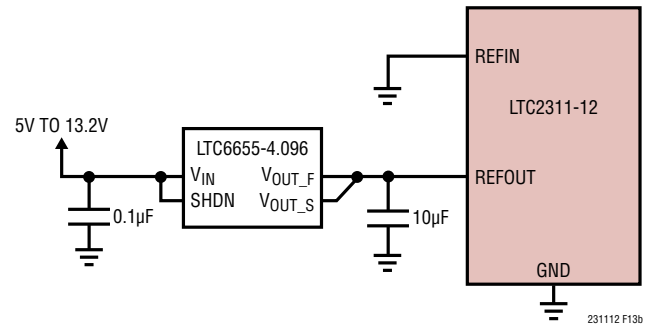


Figure 13b. LTC2311-12 with an External REFOUT Voltage

Internal Reference Buffer Transient Response

The REFOUT pin of the LTC2311-12 draws charge (Q_{CONV}) from the external bypass capacitors during each conversion cycle. If the internal reference buffer is overdriven, the external reference must provide all of this charge with a DC current equivalent to $I_{REFOUT} = Q_{CONV}/t_{CYC}$. Thus, the DC current draw of REFOUT depends on the sampling rate and output code. In applications where a burst of samples is taken after idling for long periods, as shown in Figure 14, I_{REFOUT} quickly goes from approximately ~75μA to a maximum of 700μA for REFOUT = 5V at 5Msps. This step in DC current draw triggers a transient response in the external reference that must be considered since any deviation in the voltage at REFOUT will affect the accuracy of the output code. Due to the one-cycle conversion latency, the first conversion result at the beginning of a burst sampling period will be invalid. If an external reference is used to buffer/drive the REFOUT pin, the fast settling LTC6655 reference is recommended.

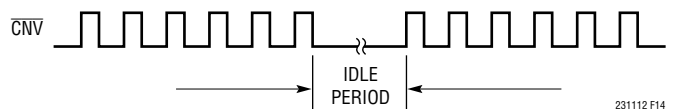


Figure 14. \overline{CNV} Waveform Showing Burst Sampling

APPLICATIONS INFORMATION

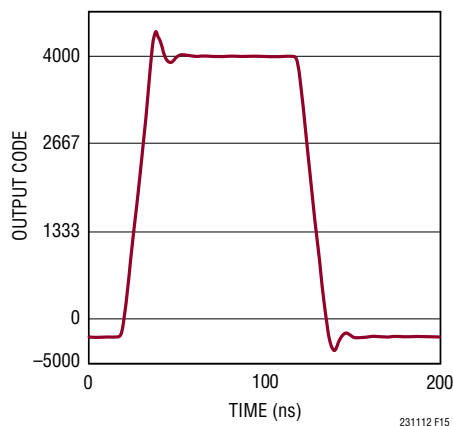


Figure 15. Transient Response of the LTC2311-12

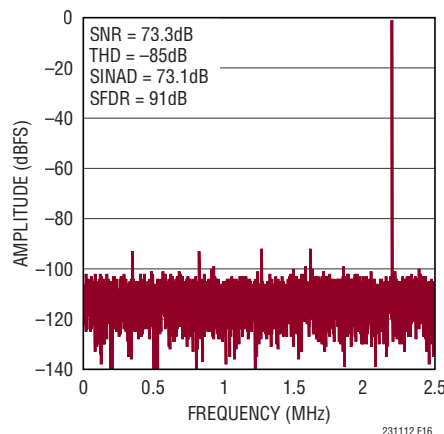


Figure 16. 16k Point FFT of the LTC2311-12

DYNAMIC PERFORMANCE

Fast Fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2311-12 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is bandlimited to frequencies from above DC and below half the sampling frequency. Figure 16 shows that the LTC2311-12 achieves a typical SINAD of 73dB at a 5MHz sampling rate with a 2.2MHz input.

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 16 shows that the LTC2311-12 achieves a typical SNR of greater than 73dB at a 5MHz sampling rate with a 2.2MHz input.

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{\text{SAMPL}}/2$). THD is expressed as:

$$\text{THD} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics. The THD specifications for the LTC2311-12 consider the first seven harmonics (i.e. $N=7$). Figure 16 shows that the LTC2311-12 achieves a typical THD of -85dB at a 5MHz sampling rate with a 2.2MHz input.

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POWER CONSIDERATIONS

The LTC2311-12 requires two power supplies: the 5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2311-12 to communicate with any digital logic operating between 1.8V and 2.5V. When using LVDS I/O, the OV_{DD} supply must be set to 2.5V.

Power Supply Sequencing

The LTC2311-12 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2311-12 has a power-on-reset (POR) circuit that will reset the LTC2311-12 at initial power-up or whenever the power supply voltage drops below 2V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 10ms after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

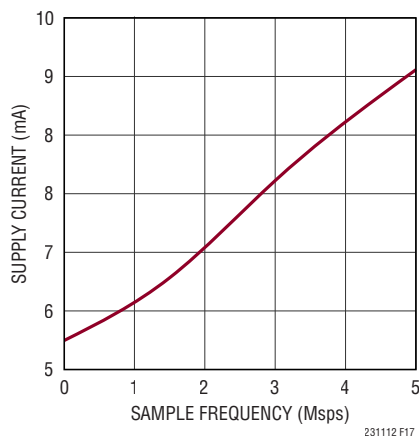


Figure 17. Power Supply Current of the LTC2311-12 Versus Sampling Rate

TIMING AND CONTROL

\overline{CNV} Timing

The LTC2311-12 sampling and conversion is controlled by \overline{CNV} . A rising edge on \overline{CNV} will start sampling and the falling edge starts the conversion and readout process. The conversion process is timed by the SCK input clock. For optimum performance, \overline{CNV} should be driven by a clean low jitter signal. The Typical Application at the back of the data sheet illustrates a recommended implementation to reduce the relatively large jitter from an FPGA \overline{CNV} pulse source. Note the low jitter input clock times the falling edge of the \overline{CNV} signal. The rising edge jitter of \overline{CNV} is much less critical to performance. The typical pulse width of the \overline{CNV} signal is 38.1ns at a 5MSPS conversion rate.

SCK Serial Data Clock Input

The falling edge of this clock shifts the conversion result MSB first onto the SDO pins. A 105MHz external clock must be applied at the SCK pin to achieve 5MSPS throughput.

Nap/Sleep Modes

Nap mode is a method to save power without sacrificing power-up delays for subsequent conversions. Sleep mode has substantial power savings, but a power-up delay is incurred to allow the reference and power systems to become valid. To enter nap mode on the LTC2311-12, the SCK signal must be held high or low and a series of two \overline{CNV} pulses must be applied. This is the case for both CMOS and LVDS modes. The second rising edge of \overline{CNV} initiates the nap state. The nap state will persist until either a single rising edge of SCK is applied, or further \overline{CNV} pulses are applied. The SCK rising edge will put the LTC2311-12 back into the operational (full-power) state. When in nap

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mode, two additional pulses will put the LTC2311-12 in sleep mode. When configured for CMOS I/O operation, a single rising edge of SCK can return the LTC2311-12 into operational mode. A 10ms delay is necessary after exiting sleep mode to allow the reference buffer to recharge the external filter capacitor. In LVDS mode, exit sleep mode by supplying a fifth $\overline{\text{CNV}}$ pulse. The fifth pulse will return the LTC2311-12 to operational mode, and further SCK pulses will keep the part from re-entering nap and sleep modes. The fifth SCK pulse also works in CMOS mode as a method to exit sleep. In the absence of SCK pulses, repetitive $\overline{\text{CNV}}$ pulses will cycle the LTC2311-12 between operational, nap and sleep modes indefinitely.

Refer to the timing diagrams in Figure 18, Figure 19, Figure 20 and Figure 21 for more detailed timing information about sleep and nap modes.

DIGITAL INTERFACE

The LTC2311-12 features a serial digital interface that is simple and straightforward to use. The flexible OV_{DD} supply allows the LTC2311-12 to communicate with any digital logic operating between 1.8V and 2.5V. A 105MHz external clock must be applied at the SCK pin to achieve 5MSPS throughput.

In addition to a standard CMOS SPI interface, the LTC2311-12 provides an optional LVDS SPI interface to support low noise digital design. The $\overline{\text{CNV}}$ /LVDS pin is used to select the digital interface mode.

The falling edge of SCK outputs the conversion result MSB first on the SDO pins. In CMOS mode, use the SDO⁺ pin as the serial data output and the SCK⁺ pin as the serial clock input. Do not connect the SDO⁻ and SCK⁻ pins as they have internal pull-downs to GND.

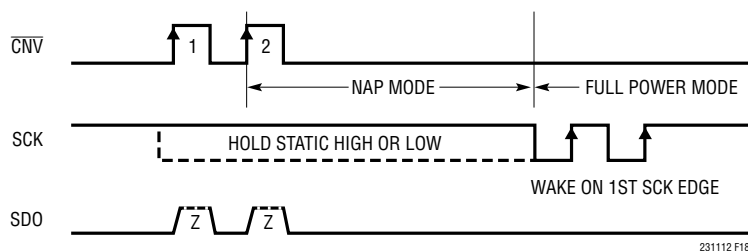


Figure 18. CMOS and LVDS Mode NAP and WAKE Using SCK

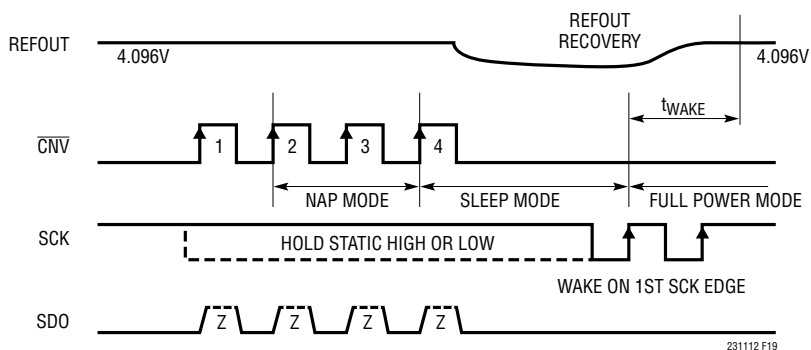


Figure 19. CMOS Mode SLEEP and WAKE Using SCK

APPLICATIONS INFORMATION

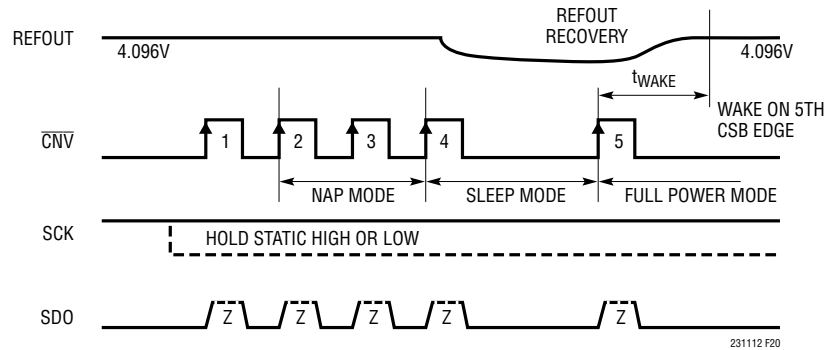
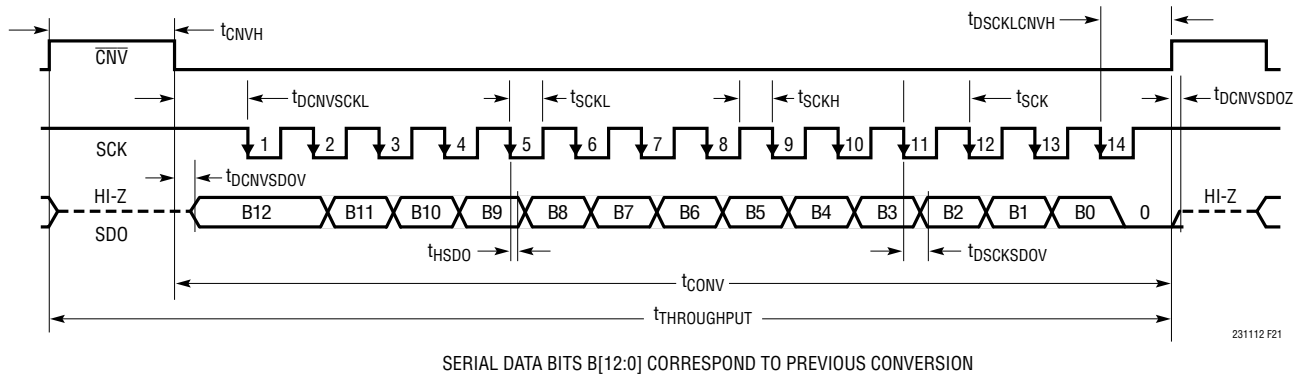
Figure 20. LVDS and CMOS Mode SLEEP and WAKE Using $\overline{\text{CNV}}$ 

Figure 21. LTC2311-12 Timing Diagram, CMOS, LVDS I/O Modes

APPLICATIONS INFORMATION

In LVDS mode, use the SDO⁺/SDO⁻ pins as a differential output. These pins must be differentially terminated by an external 100Ω resistor at the receiver (FPGA). The SCK⁺/SCK⁻ pins are a differential input and must be terminated differentially by an external 100Ω resistor at the receiver (ADC), see Figure 22.

BOARD LAYOUT

To obtain the best performance from the LTC2311-12, a four layer printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals adjacent to analog signals or underneath the ADC.

A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground.

Reference Design

For a detailed look at the reference design for this converter, including schematics and PCB layout, please refer to the [DC2425](#), the evaluation kit for the LTC2311-12.

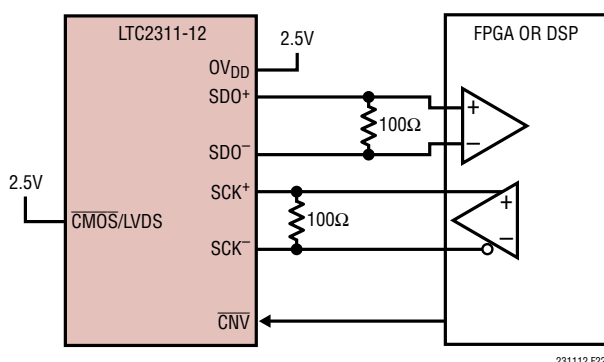
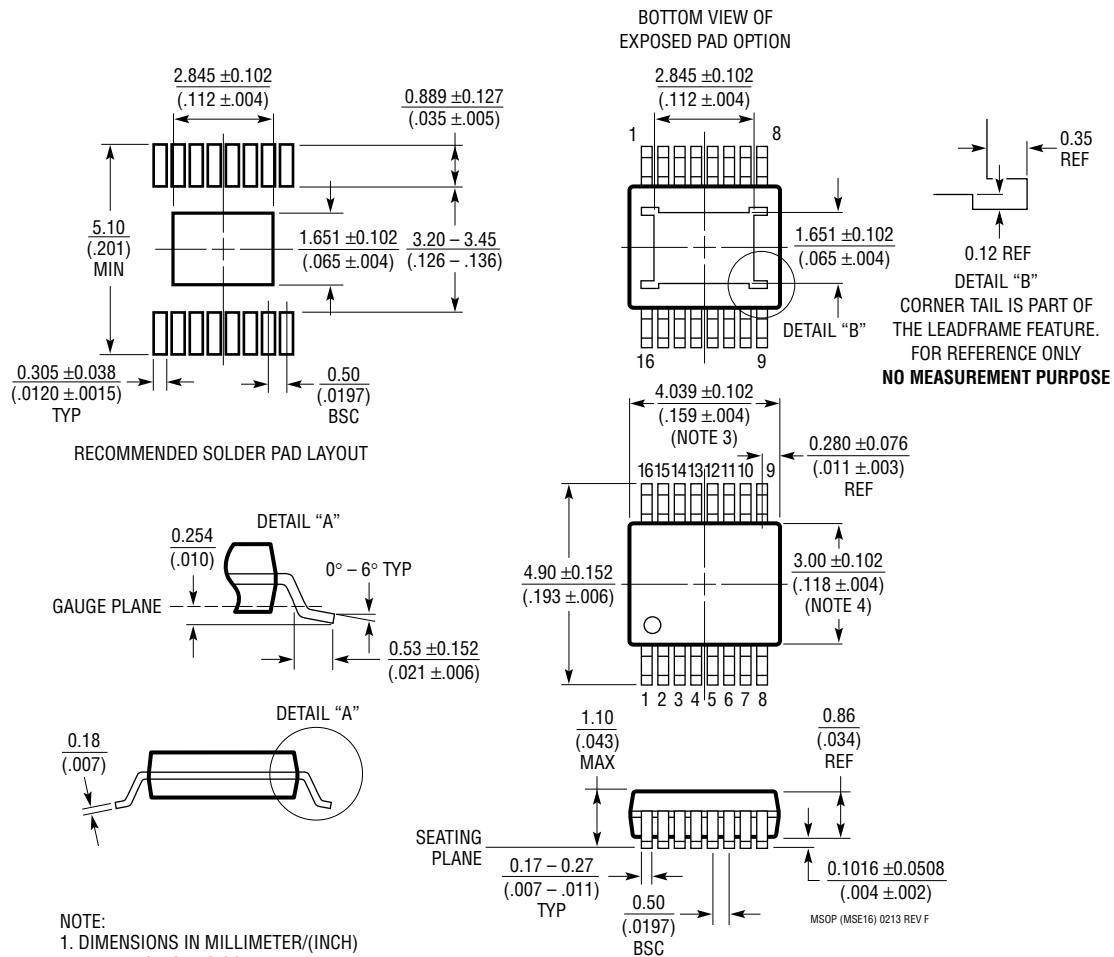


Figure 22. LTC2311-12 Using the LVDS Interface

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC2311-12#packaging> for the most recent package drawings.

MSE Package 16-Lead Plastic MSOP, Exposed Die Pad (Reference LTC DWG # 05-08-1667 Rev F)



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