

TUSHAR
SHRIJAYAN
3/4/2022

COEN 21 - HW #7

6.3

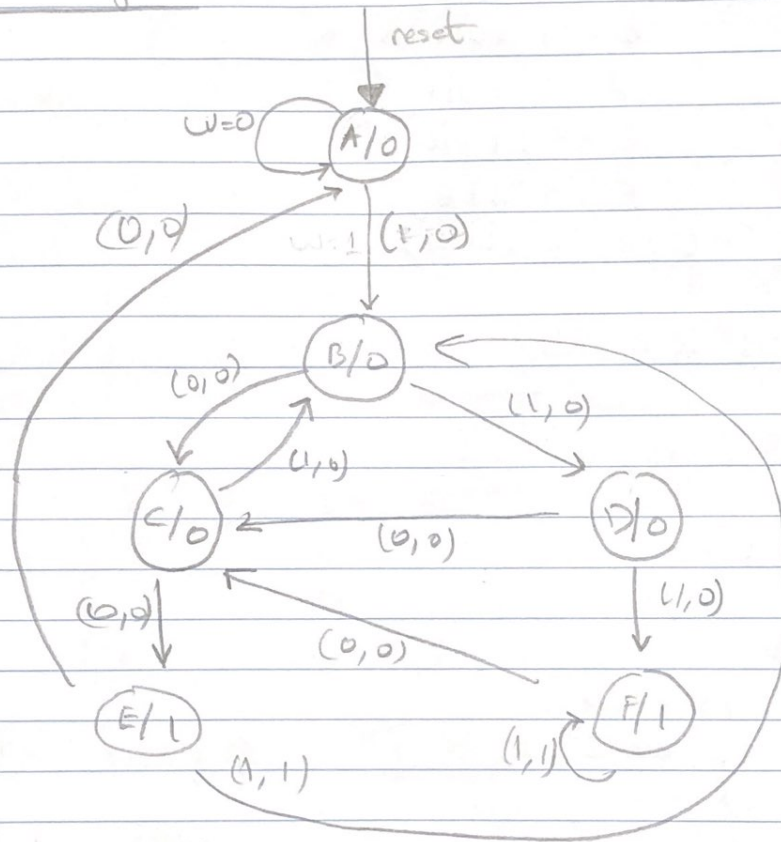
input: w

output: z

$z = 1$, $w = 1001, 1111$, otherwise $z = 0$

MEMORY FSM is required
→ output dependent

State Diagram



6.4

Verilog Code

6.9

input: w_1, w_2 output: z if $w_1 = w_2$ / $z = 1$ else $z = 0$

0123456789101112
 $U_1 = 0110111000110$
 $w_2 = 1110101000111$
 $z = 0000100001110$

\uparrow $\uparrow \uparrow \uparrow$

(mealy FSM)

Let $X = w_1 \oplus w_2$ State Table

	Present State		Input	Next State		Output
	y_1	y_0		Y_1	Y_0	
A:	0	0	0	0	1	0
	0	0	1	0	0	0
B:	0	1	0	1	0	0
	0	1	1	0	0	0
C:	1	0	0	1	1	0
	1	0	1	0	0	0
D:	1	1	0	0	1	1
	1	1	1	0	0	0

KMAP MINIMIZATION

y_1	y_0		x	
	0	1	0	1
0	0	0	0	0
1	0	0	0	1

$$Y_1 = \bar{x}y_0 + \bar{x}y_1$$

y_1	y_0		x	
	0	1	0	1
0	1	0	0	0
1	1	0	0	1

$$Y_0 = \bar{x}y_0 + y_1\bar{x}$$

y_1	y_0		x	
	0	1	0	1
0	0	0	0	0
1	0	0	0	1

$$z = x y_1 y_0$$

Circuit Diagram

