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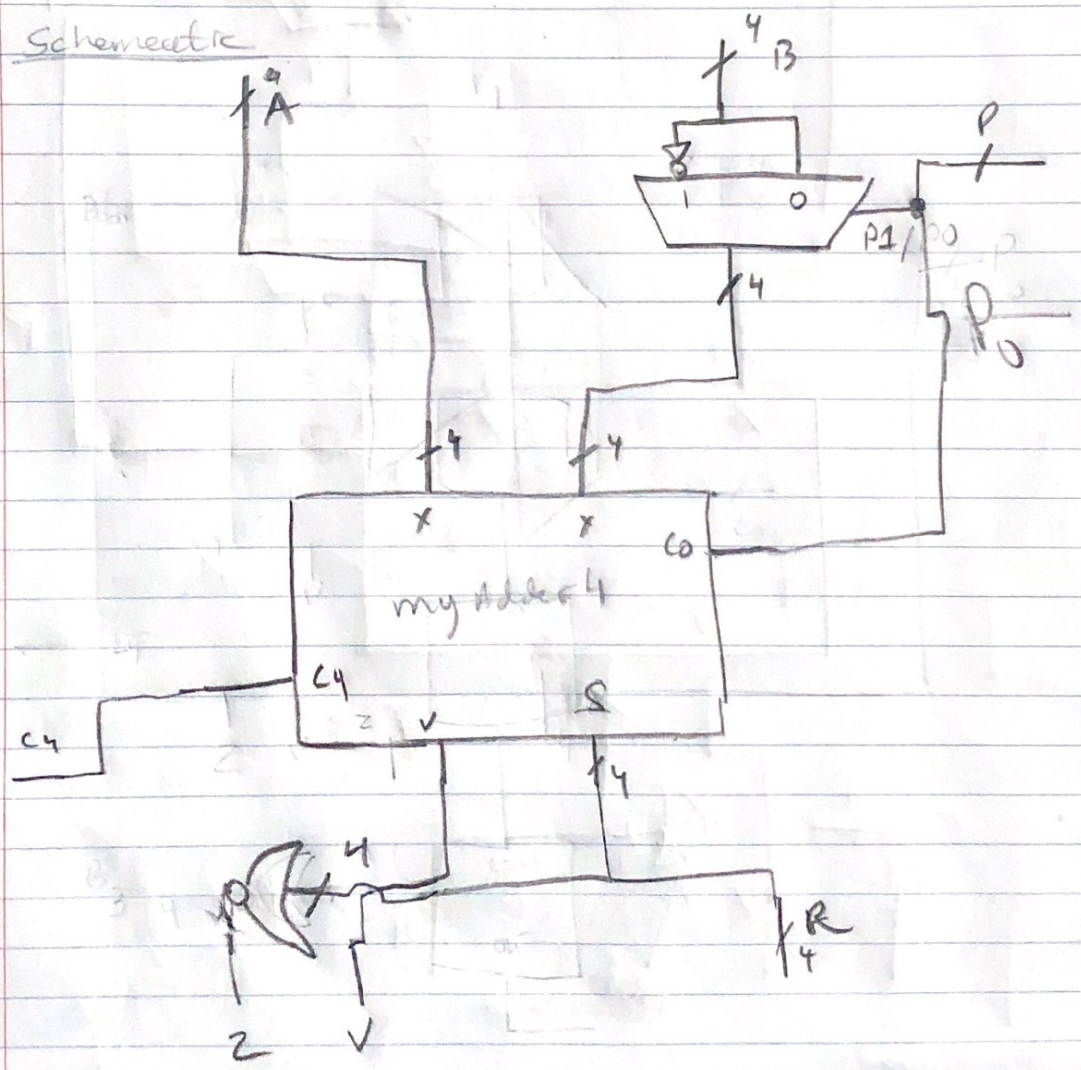
LAB #16: minicalc w/ small 4-bit arithmetic logic unit

1.

op-select input	Adder 4-bit X inputs	Adder 4-bit Y inputs	Adder Carry in	Operation	Name
p3 p2 p1 p0	a3 a2 a1 a0	b3 b2 b1 b0			
0 0 0 0	a3 a2 a1 a0	b3 b2 b1 b0	0	R = A+B	Add
0 0 0 1	a3 a2 a1 a0	b3 b2 b1 b0	1	R = A+B+1	Add and increment
0 0 1 0	a3 a2 a1 a0	$\overline{b3}$ $\overline{b2}$ $\overline{b1}$ $\overline{b0}$	0	R = A-B-1	Subtract & decrement
0 0 1 1	a3 a2 a1 a0	$\overline{b3}$ $\overline{b2}$ $\overline{b1}$ $\overline{b0}$	1	R = A-B	Subtract

2. → 4-bit adder symbol / → 2:1 MUX

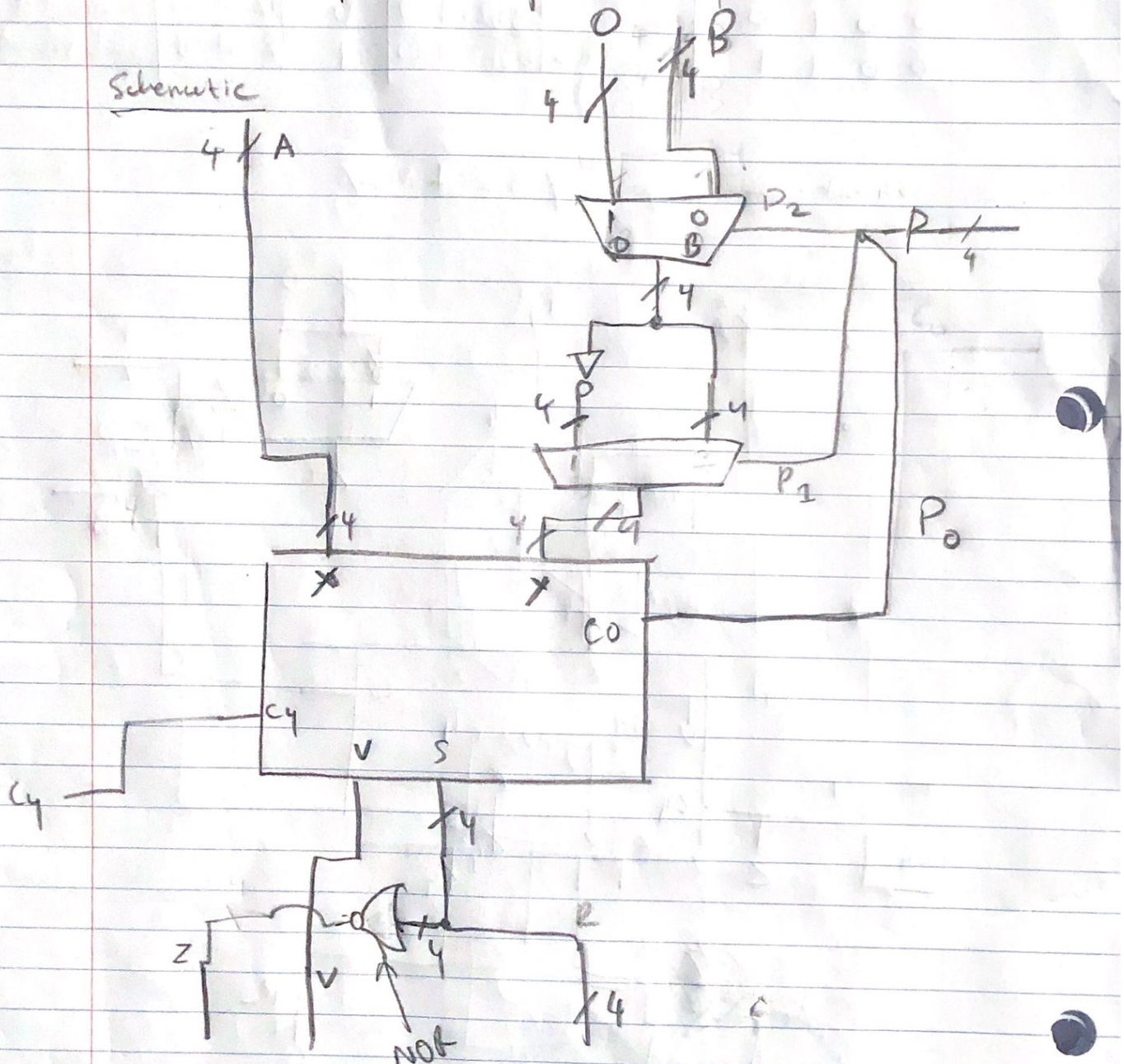
Schematic



3.

p3	p2	p1	p0	R control	OPERATION	Y value	error
0	1	0	0	R = A	transfer A	0000	0
0	1	0	1	R = A + 1	increment A	0001	1
0	1	1	0	R = A - 1	decrement A	1111	0
0	1	1	1	R = A	Duplicate	1111	1

Schematic



4.
```
module myALA4 (P, A, B, CO, R, C4, V, Z);

    input CO;
    input [3:0] A, B, P;
    output [3:0] R;
    output C4, V, Z;

    reg [3:0] Y;

    always @(*)
    begin
        case( P[2:1] )
            2'b00 : Y = B;
            2'b01 : Y = ~B;
            2'b10 : Y = 4'b0000;
            2'b11 : Y = 4'1111;
        endcase
    end

    myadder 4(P[0], A, Y, V, C4, R);

    assign Z = ~(R[0] | R[1] | R[2] | R[3]);
endmodule
```

5.

P0 controls the carry input to 4-bit ALU.

P1 selets operation of subtracting / adding B.

P2 selects the operation to increment/decrement/transfer A.

6. TEST PLAN
   → test P_0 carry input
   → test P1 operation select 0/1
   → test P2 operation select 0/1