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Lab 4 Report

Introduction

In this lab, we will be implementing a binary adder that takes in 2 two-bit integers and outputs a three-bit integer. We will use multiplexers to complete our design and will use Verilog and schematic design to implement the block diagrams. The three outputs, S2, S1, and S0, will represent the digits of the sum.

We derived the behavior of the binary adder into a truth table, and created the K-maps from it. Then listed the equations when we use A1 input as a select line for 3 multiplexers to determine the outputs S2, S1, and S0.

[Rest of Report Continued on next page]

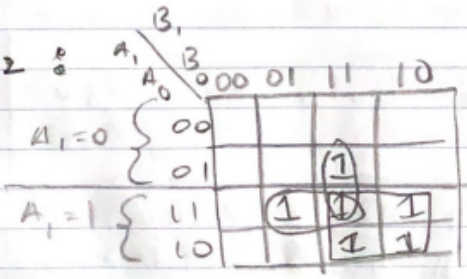
KMAPS & Logic Expressions

PART 2 – Create schematic Options for circuit outputs

a) using A1 for select bit

b) Kmaps → S_2 :

i)

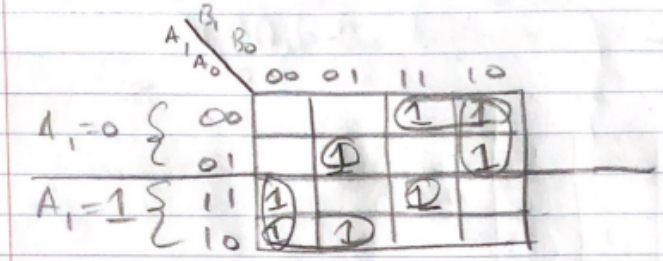


expression

$A_1B_1 + A_0\bar{B}_1\bar{B}_0 + \bar{A}_1A_0\bar{B}_0$

i) continued

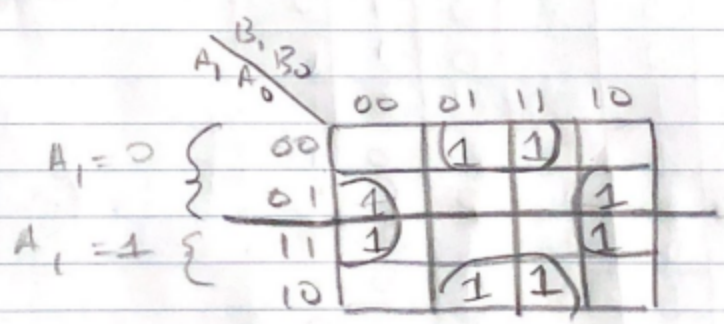
S_1 Kmap



expression: $A_1\bar{B}_1\bar{B}_0 + A_1A_0\bar{B}_1 + \bar{A}_1A_0\bar{B}_1\bar{B}_0 + A_1\bar{A}_0\bar{B}_1\bar{B}_0$

$+ \bar{A}_1\bar{A}_0B_1 + \bar{A}_1B_1\bar{B}_0$

S_0 Kmap



$$S_0 = \bar{A}_0 B_0 + A_0 \bar{B}_0$$

From K-maps → Shannon Expansion

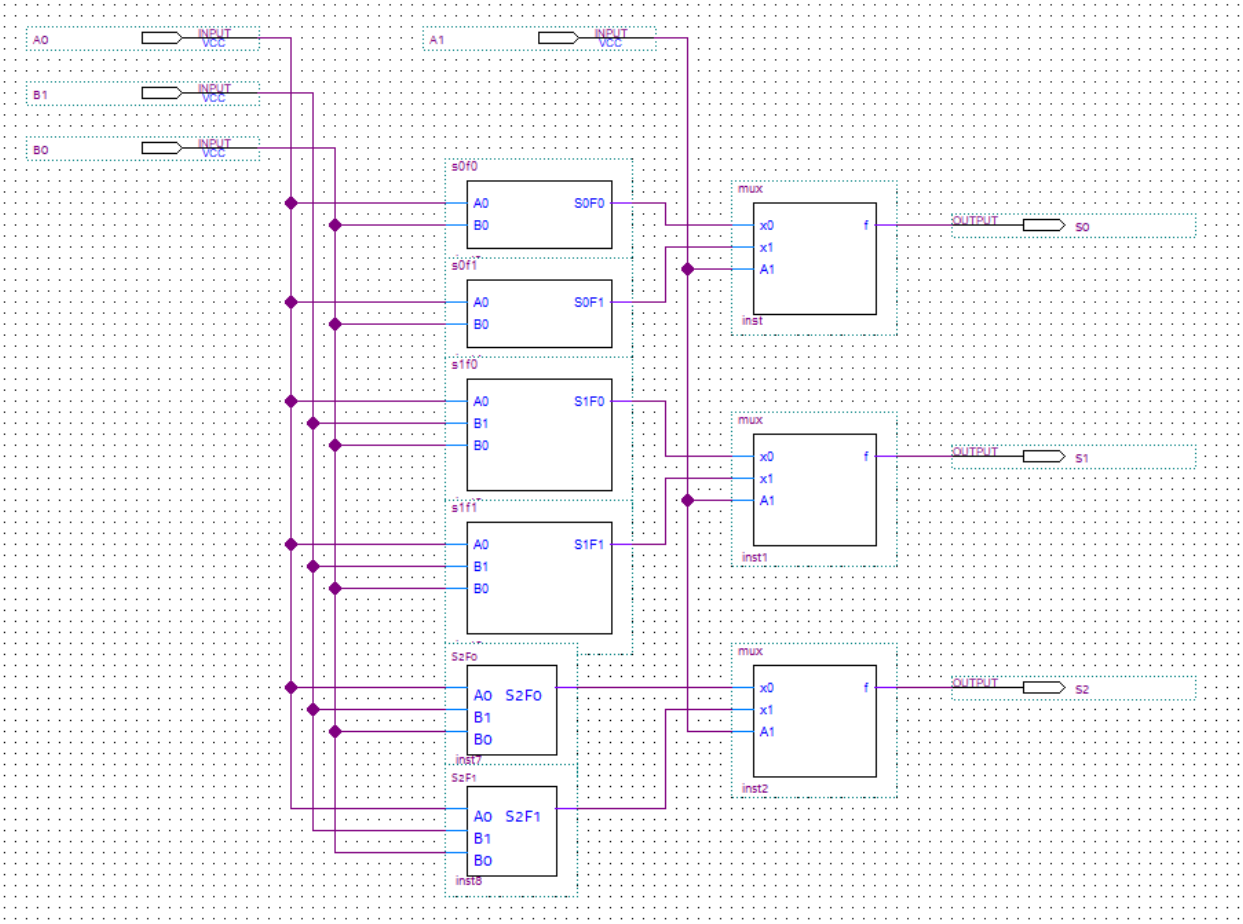
$S_0 F_0 = \bar{A}_0 B_0 + A_0 \bar{B}_0 = A_0 \oplus B_0$ | $S_2 F_0 = A_0 B_1 B_0$

$S_0 F_1 = \bar{A}_0 B_0 + A_0 \bar{B}_0 = A_0 \oplus B_0$ | $S_2 F_1 = B1 + A0 B0$

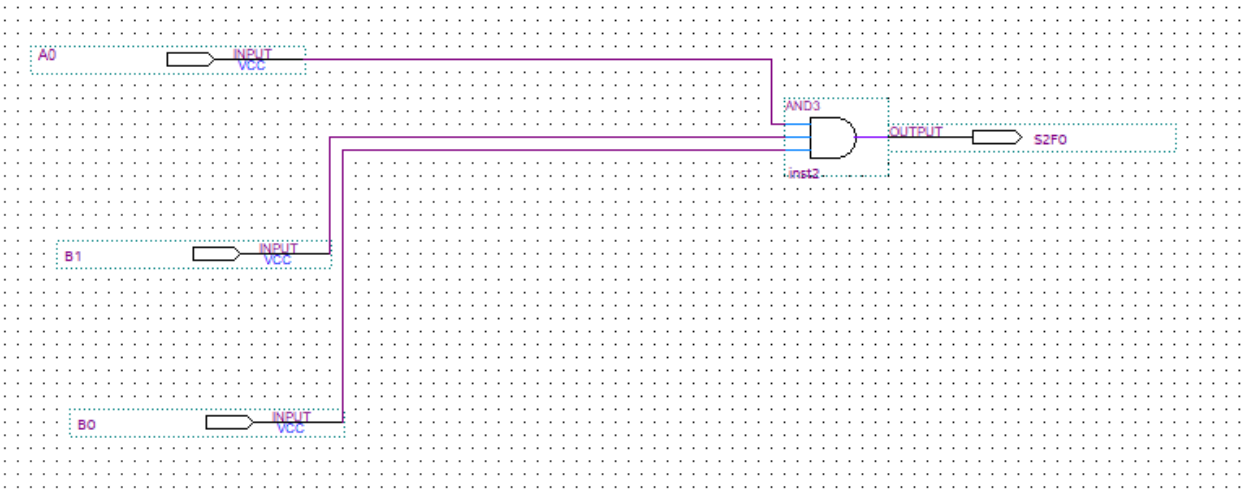
$S_1 F_0 = \bar{A}0 B1 + A0 \bar{B}1 B0 + B1 B0$

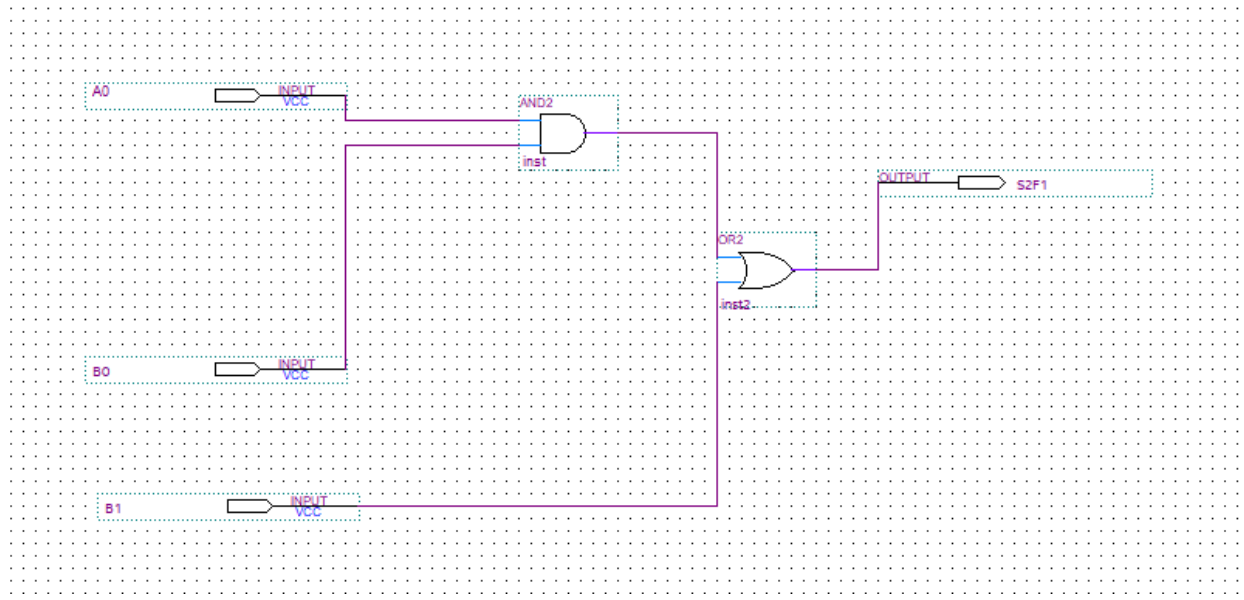
$S_1 F_1 = \bar{A}0 \bar{B}1 + A0 B1 B0 + \bar{B}1 B0$

Final Schematic



S2 Schematics



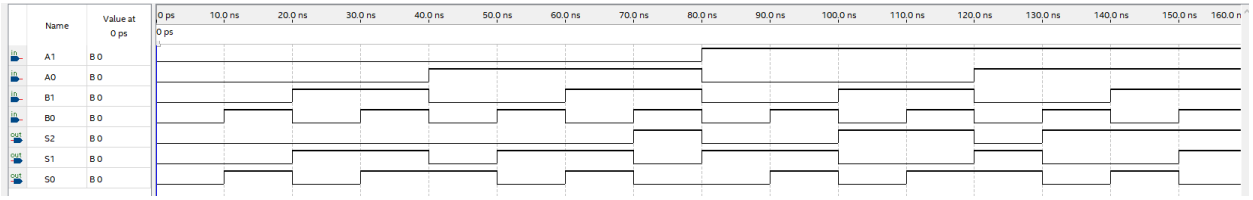


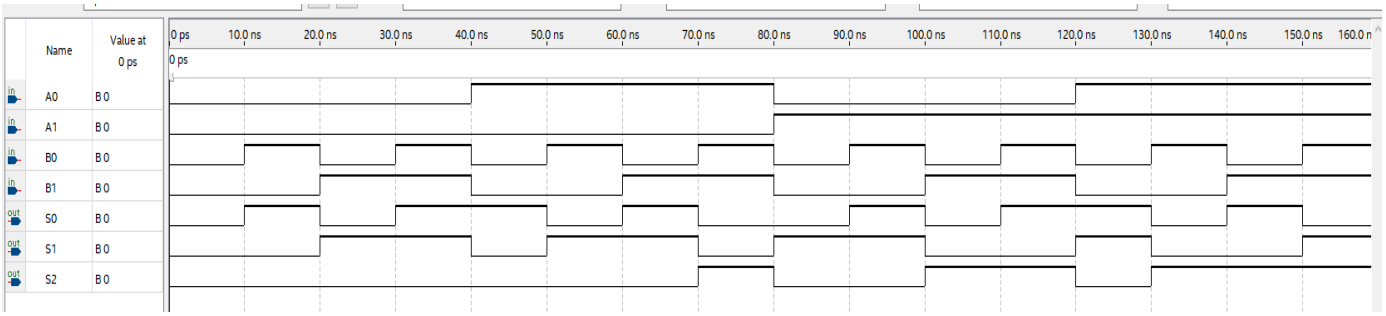
Final Verilog Code

```
1   module Mux2to1(x1,x2,A1,f);
2      input x1,x2,A1;
3      output f;
4
5      assign f=(~A1&x1)|(A1&x2);
6   endmodule
7
8   module S0(A0,B0,f);
9         input A0, B0;
10        output f;
11        assign f = A0 ^ B0;
12  endmodule
13
14  module S1F0(A0,B0,B1,f);
15      input A0,B0,B1;
16      output f;
17      assign f = (~A0&B1)|(B1&~B0)|(A0&~B1&B0);
18  endmodule
19
20  module S1F1(A0,B0,B1,f);
21      input A0,B0,B1;
22      output f;
23      assign f = (A0&B1&B0)|(~B1&~B0)|(~A0&~B1);
24  endmodule
25
```

Problems During Testing

We did not encounter any problems during testing since we tested our results in the waveform test before we burn it onto the FPGA.





Conclusion

In this lab, we actually applied Verilog to build circuits on top of the simulation and circuit building we did in prior labs. Our primary challenges were when needing to show the circuit on the FPGA board, but we pretty much fixed that by using a different board. Generally any other challenges were just working with the software to convert verilog and schematics onto the main block diagram using the create schematic into symbol option.