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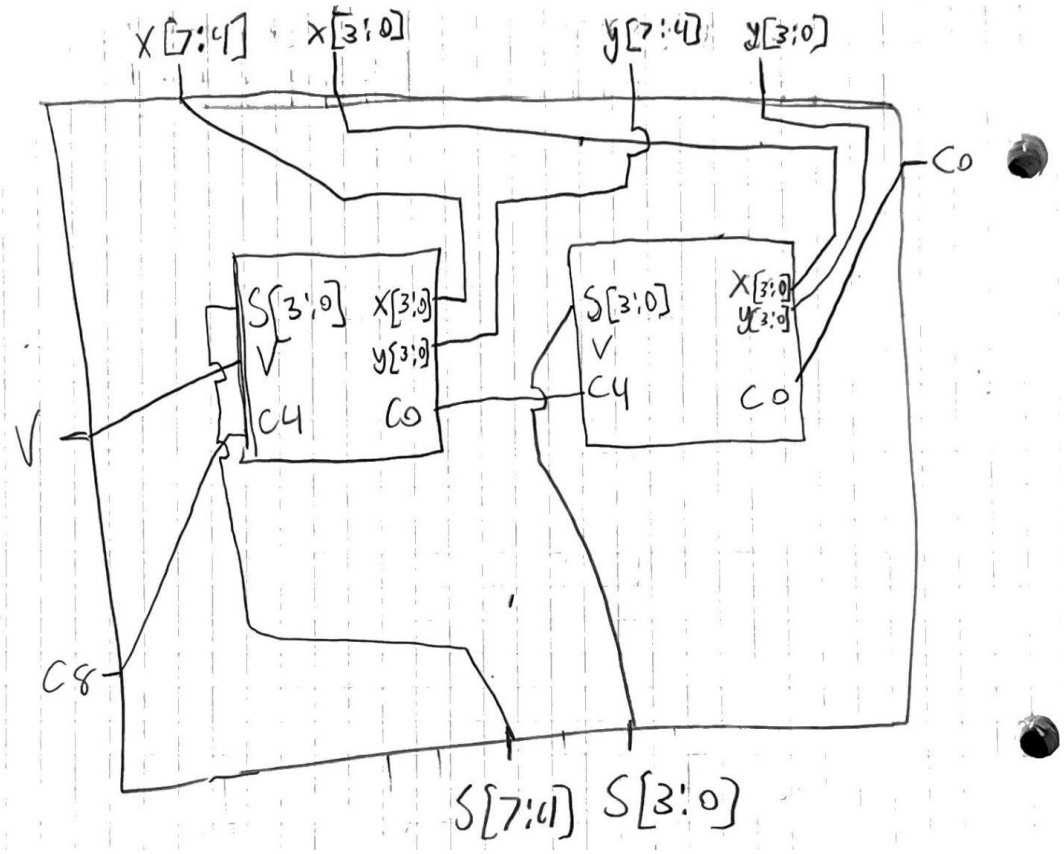
COEN 21 Lab 5 Report

1)

a.) X=4'b0000 (Hex: 0) & Y=4'b0000 (Hex: 0)
b.) X=4'b0100 (Hex: 4) & Y=4'b0100 (Hex: 4)
c.) X=4'b1100 (Hex = 9) & Y=4'b1100 (Hex: 7)
d.) X=4'b1100 (Hex = C) & Y=4'b1000 (Hex: A)

2)



3)

The Initial testing of the circuit went smoothly, and there were no errors in our Verilog code to cause any.

4) No, we would not be able to find a difference from the output, because the bits would be added normally since they are the same as their original values before swapping.

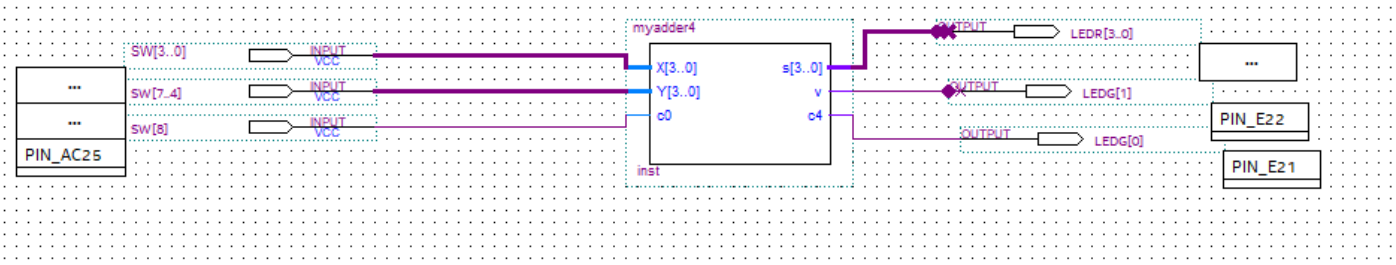
5)

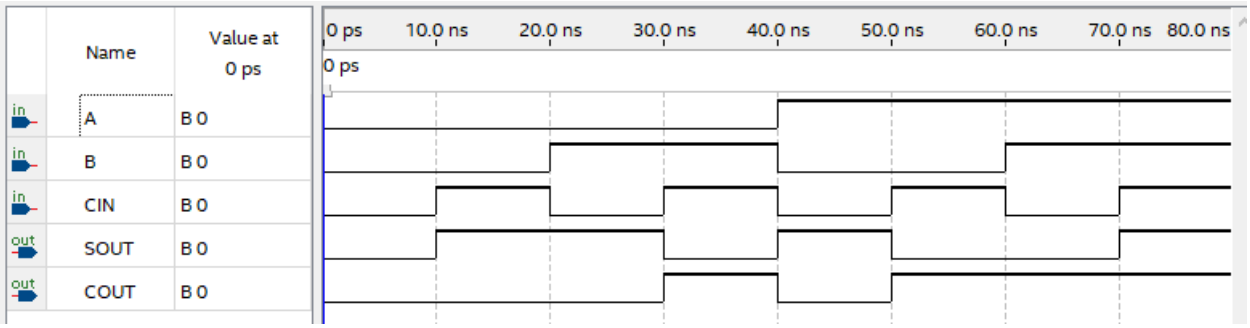
a) It is showing incorrect results at S1 and S0 (b1 and b0) (the values are swapped).
b) What is wrong is that the wires for S1 and S0 are connected to the incorrect outputs.

c) A test that might help to prove my hypothesis is to set the Inputs X and Y to 0100 and 0001 respectively, and the correct outputs would be 0101, while the incorrect output would be 0110.

Schematics, Verilog, and Waveforms

```
1   module myfulladd(A,B,CIN,SOUT,COUT);
2      input A,B,CIN;
3      output SOUT,COUT;
4
5      assign SOUT=A ^ B ^ CIN;
6      assign COUT=(A & B)|(B & CIN)|(A & CIN);
7   endmodule
8
9   module myadder4(X,Y,c0,s,v,c4);
10     input c0;
11     input [3:0]X,Y;
12     output[3:0]s;
13     output v,c4;
14     wire [2:0]c;
15
16     myfulladd(X[0],Y[0],c0,s[0],c[0]);
17     myfulladd(X[1],Y[1],c[0],s[1],c[1]);
18     myfulladd(X[2],Y[2],c[1],s[2],c[2]);
19     myfulladd(X[3],Y[3],c[2],s[3],c4);
20     assign v=c4^c[2];
21  endmodule
```





Truth Table Result

X	Y	C0	S	V	C4
0	0	0	0000	0	0
0	0	1	0001	0	0
1	0	0	0001	0	0

0	1	0	0001	0	0
2	0	0	0010	0	0
4	3	0	0111	0	0
4	4	0	1000	1	0
9	6	0	1111	0	0
9	7	0	0000	0	1
C	A	0	0110	1	1
E	A	0	1000	0	1
E	A	1	1001	0	1