TUSHAR SRIVASTAVA

COEN 21 - Lab#5 4-bit Ripple-Carry Adder

PRELAB

1. truth Table

A	B	CIN	SOUT	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$SOUT = \bar{A}\bar{B}\,CIN + \bar{A}B\overline{CIN} + A\bar{B}\,\overline{CIN} + AB\,CIN$

$= \overline{CIN}(\bar{A}B + A\bar{B}) + CIN(AB + \bar{A}\bar{B})$

using $X \oplus Y = \bar{X}Y + X\bar{Y}$ and $X \oplus Y = (X + \bar{Y}) \cdot (\bar{X} + Y)$

$\therefore SOUT = \boxed{CIN \oplus A \oplus B}$

$COUT = \bar{A}BCIN + A\bar{B}\,CIN + AB\overline{CIN} + AB\,CIN$

$\rightarrow CIN(\bar{A}B + A\bar{B}) + ABCIN + ABCIN$

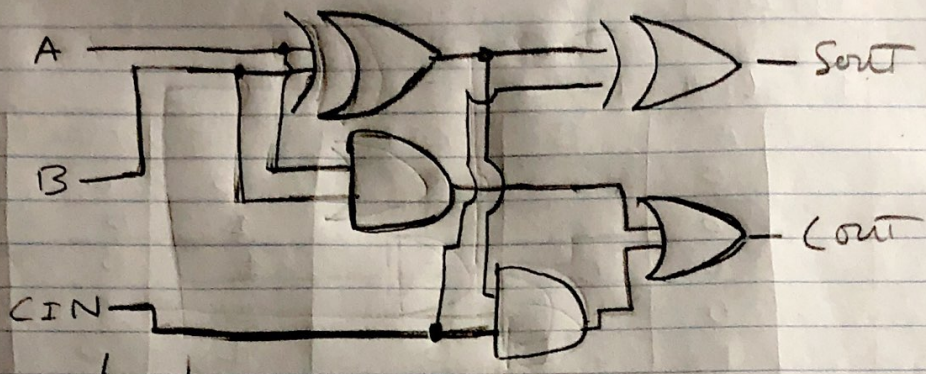
$\rightarrow CIN(A \oplus B) + AB$

A \ CIN / B	0	1
00		
01		1
11	1	1
10		1

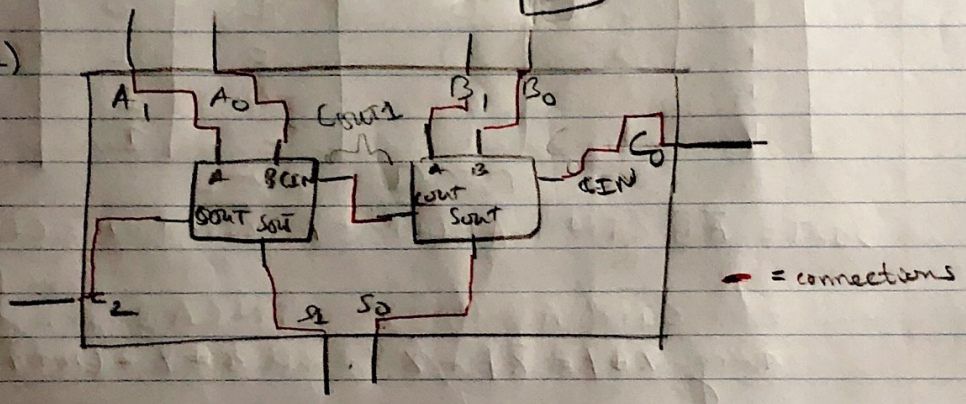
$COUT = AB + BCIN + ACIN$

OR $AB + (A \oplus B)CIN$

2. Logic Circuit



3. a)



b) 5 × 2 = 10 logic gates

4.
```
module fullAdd(A, B, CIN, SOUT, COUT);
    input A, B, CIN;
    output SOUT, COUT;
    assign SOUT = CIN ^ A ^ B;
    assign COUT = (CIN & (A^B)) | (A&B);
endmodule
```

5.
```
module twoBitRippleAdd(A1, A0, B1, B0, C0, S1, S0, C2);
    input A1, A0, B1, B0 C0;
    output S1, S0, C2;
    wire COUT1;
    fullAdd(A1, A0, C0, S0, COUT1);
    fullAdd(B1, B0, COUT1, S1, C2);
endmodule
```

6.

Test Procedure

1. If A1, A0, B1, B0, C0,

→ All outputs, S1, S0, C2 = 0

2. If one input = 1 and all other inputs are 0, then...

A1 = 1 then ⇒ S1 = 1, S0 = 0, C_2 = 0
A0 = 1 then ⇒ S1 = 1, S0 = 0, C2 = 0
B1 = 1 then ⇒ S1 = 0, S0 = 1, C2 = 0
B0 = 1 then ⇒ S1 = 0, S0 = 1, C2 = 0
C0 = 1 then ⇒ S1 = 1, S0 = 0, C2, = 0

3. Testing individual carry connections

See if $B_1 B_0 = 1$, output carry to Cout 1.
Similarly with $A_1 A_0 = 1$.