TUSHAR
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COEN 21 - HW #5

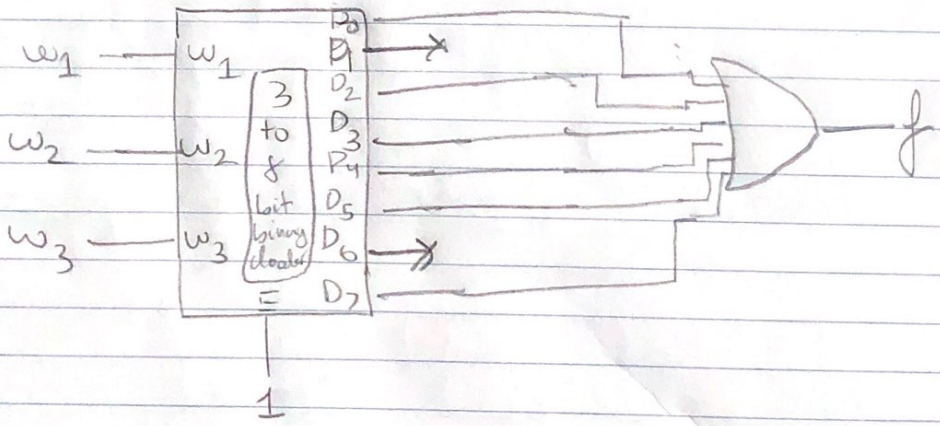
4.1] $f(w_1, w_2, w_3) = \sum m(0,2,3,4,5,7)$

using 3-to-8 binary decoder and an OR GATE

Truth TABLE

	w_1	w_2	w_3	f	Decoder value							
0	0	0	0	1	1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0	0	0	0	0	0
2	0	1	0	1	0	0	1	0	0	0	0	0
3	0	1	1	1	0	0	0	1	0	0	0	0
4	1	0	0	1	0	0	0	0	1	0	0	0
5	1	0	1	1	0	0	0	0	0	1	0	0
6	1	1	0	0	0	0	0	0	0	0	1	0
7	1	1	1	1	0	0	0	0	0	0	0	1

Logic Circuit



4.18]

The verilog code represents a 2 to 4 decoder.

The style of code is NOT a good choice, because it is not easy to read, and can be confused for a multiplexer with En as a select line.

4.21] verilog code for an 8-3 binary encoder

```
module enc8to3(W, En, Y);
  input [7:0] W;
  input En;
  output reg [0:2] Y;

  always @(W, En)
    case({En, W})
      8'b000000001: y = 3'b000;
      8'b000000010: y = 3'b001;
      8'b000000100: y = 3'b010;
      8'b000001000: y = 3'b011;
      8'b000010000: y = 3'b100;
      8'b000100000: y = 3'b101;
      8'b001000000: y = 3'b110;
      8'b010000000: y = 3'b111;
      default: y = 3'b000;
    endcase
endmodule
```

4.22] → The error is that Y[K] is not being set when W != K.