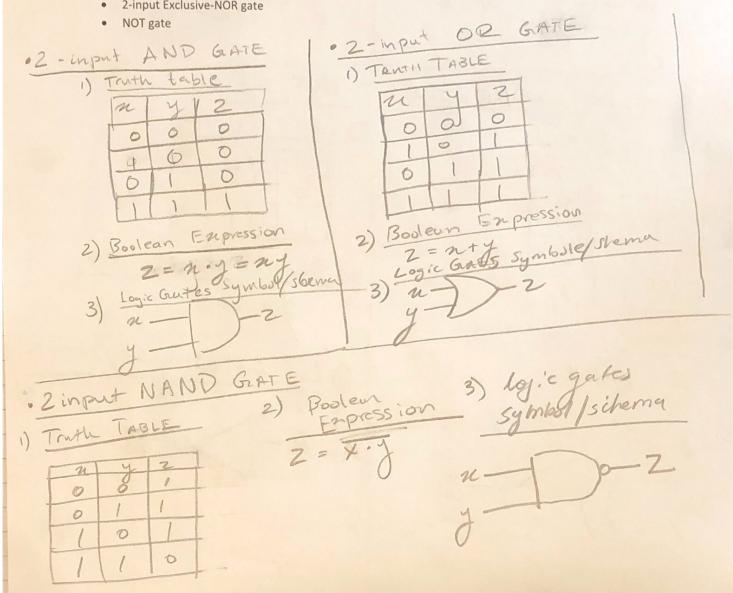
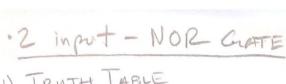
Santa Clara University Name: TUSH AR R **COEN 21 - Winter 2022** Homework #1 Please scan and upload your completed homework on Camino | Due Date: 1/7/2022

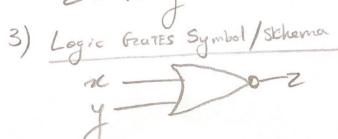
Draw the (1) truth table; (2) Boolean expressions, and (3) logic gates symbol/schematic for each of the following:

- 2-input AND gate
- 2-input OR gate
- 2-input NAND gate
- 2-input NOR gate
- 2-input Exclusive-OR gate
- 2-input Exclusive-NOR gate
- NOT gate





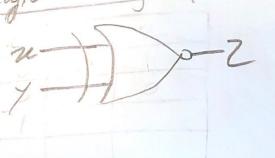
n.	1 7	2
no	0	1
10	1	0
1	0	0
1	1,	0



n	y	2	
0	0	0	
0	١	1	
1	0	1	
1	1	0	

1) TRUTH TABLE

れ	4	121
0	0	12
0	1	0
1	0	0.
T	1	11



n	4
0	
	0

