Lab 1 – Alice EduBase Keypad

CSE 479 – Advanced Embedded Systems
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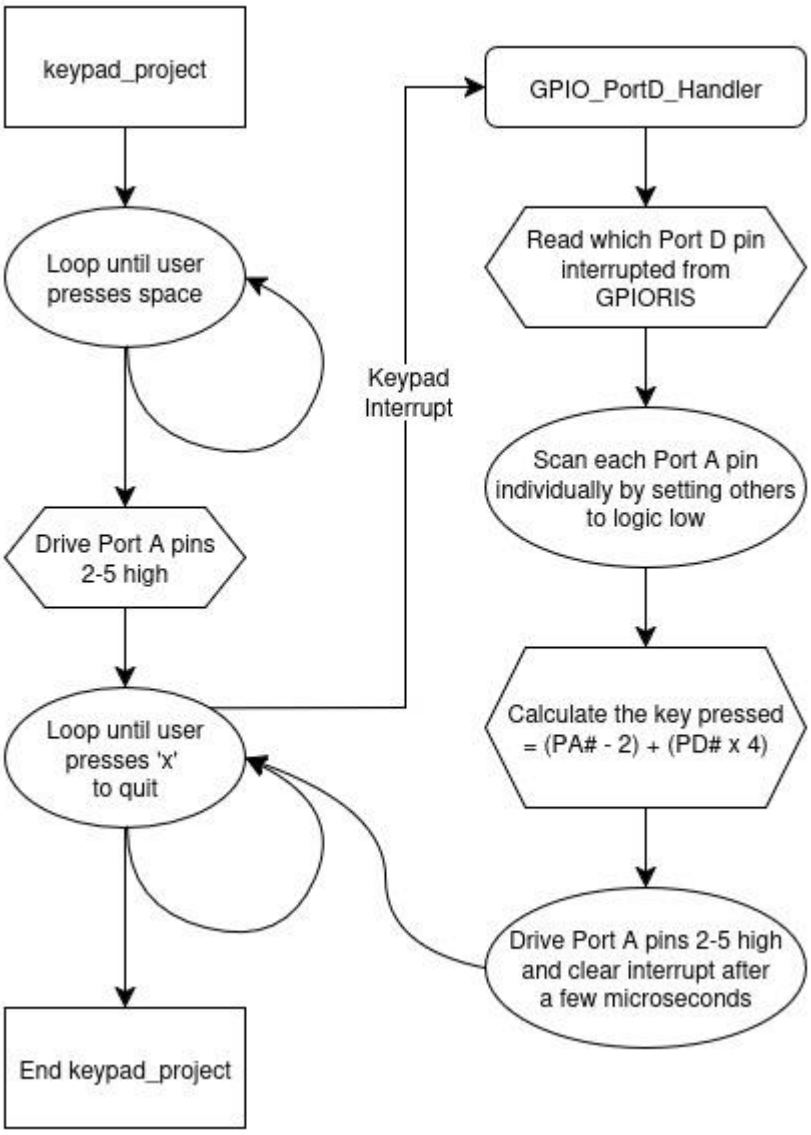
Section 1: Keypad Routine Documentation



Section 2: Tiva-Keypad Hypothesis

If students accidentally wrote to the GPIODATA register on Port D using the same bits as used on Port A (corresponding to P2:5), the PD4 and PD5 pins may have damaged the Tiva due to their Non-Fail-Safe design. According to the Tiva C Series TM4C123GH6PM data sheet, Port D pins PD4 and PD5 are classified as "non-fail-safe pins". This means that they lack the ESP protection that prevents indirect power between the I/O pads and power supply rails. Their protection consists of two diodes, one from ground to the I/O pad, and another from the I/O pad to VDD. It is possible to open a path between the I/O pad and the internal power rail if the diodes became forward biased (24.13.2.2, pg. 1387).

Another important characteristic of pins PD4 and PD5 are only 3.6V tolerant when configured as input, whereas the other GPIO pins are 5V tolerant (10.1, pg. 649). Texas Instruments provides the application report "Use Conditions for 5-V Tolerant GPIOs on Tiva C Series TM4C123x Microcontrollers," which states that since the GPIO pins with fail-safe ESD circuitry do not use a diode, there is no potential to form path from the pin to the power supply (3.1.4, pg. 4). Therefore, the non-fail-safe ESDs, which use diodes, are susceptible to forward biasing conditions when the input voltage is greater than its power supply voltage plus 0.6V. This situation could lead to damage to the device.

Finally, the Tiva C Series data sheet provides a list of situations in which improper input voltages and currents could damage the board due to the characteristics described above (Table 24-32[abcd], pg. 1387-1388). Given that pins PD4 and PD5 can also be used as input and output for USB0 (Table 18-1, pg. 1101), it is possible to have written to those pins if the Port D base address was accidentally used in place of the Port A base address. When configured as USB, there are internal resistors that protect these pins (18.2, pg. 1100). When configured as GPIO, Table 24-32[a] recommends an external resistor.

This hypothesis could be disproved if more information were readily available for the output characteristics. In any case, physical damage due to improper powering seems like a more likely explanation than a situation such as changing a critical bit in a GPIO register unrelated to the project (where it is assumed that the CSE 379 students received information about the exact registers that are needed for configuration).