Unit 8. Combinational Circuit Design And Simulation using Gates

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Objectives

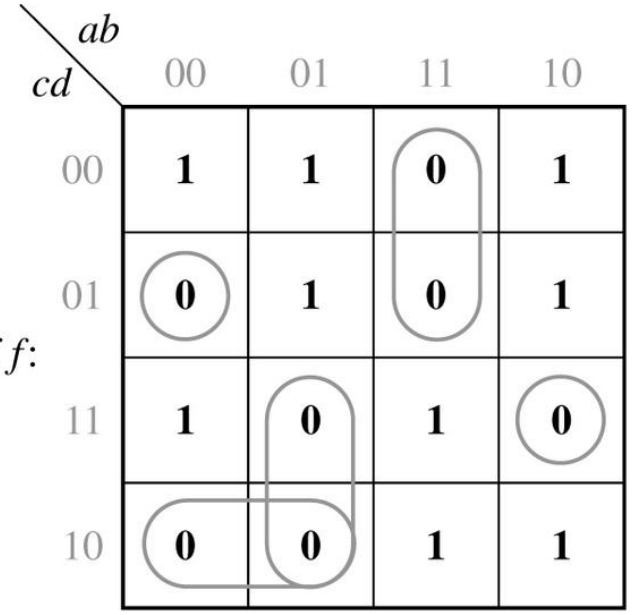
Topics introduced in this chapter:

- Draw a timing diagram for a combinational circuit with gate delays.
- Define static 0-and 1-hazards and dynamic hazard. Given a combinational circuit, find all of the static 0-and 1-hazards. For each hazard, specify the order in which the gate outputs must switch in order for the hazard to actually produce a false output.
- Given switching function, realize it using a two-level circuit which is free of static and dynamic hazards (for single input variable changes).
- Design a multiple-output NAND or NOR circuit using gates with limited fan-in.
- Explain the operation of a logic simulator that uses four-valued logic.
- Test and debug a logic circuit design using a simulator.

Design of Circuits with Limited Gate Fan-in

Example: Realize $f(a,b,c,d) = \sum m(0,3,4,5,8,9,10,14,15)$ using 3-input NOR gate

map of f:



$f' = a'b'c'd + ab'cd + abc' + a'bc + a'cd'$

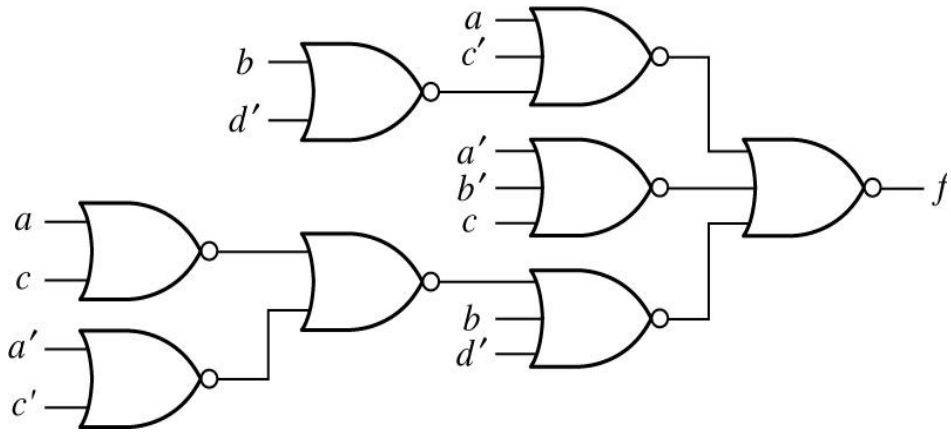
- Fan-in : maximum number of inputs on each gate

Design of Circuits with Limited Gate Fan-in

$$f' = b'd(a'c') + a'c(b + d') + abc'$$

$$f = [b + d' + (a + c)(a' + c')][a + c' + b'd][a' + b' + c']$$

- Wrong equations!!



Design of Circuits with Limited Gate Fan-in

Example: Realize the functions given in Figure 8-2,
using only 2-input NAND gates and inverters.(NAND? → SOP)

If we minimize each function separately, the result is

$$f_1 = b'c' + ab' + a'b$$
$$f_2 = b'c' + bc + a'b$$
$$f_3 = a'b'c + ab + bc'$$

we need 3-input OR gates,
so ...

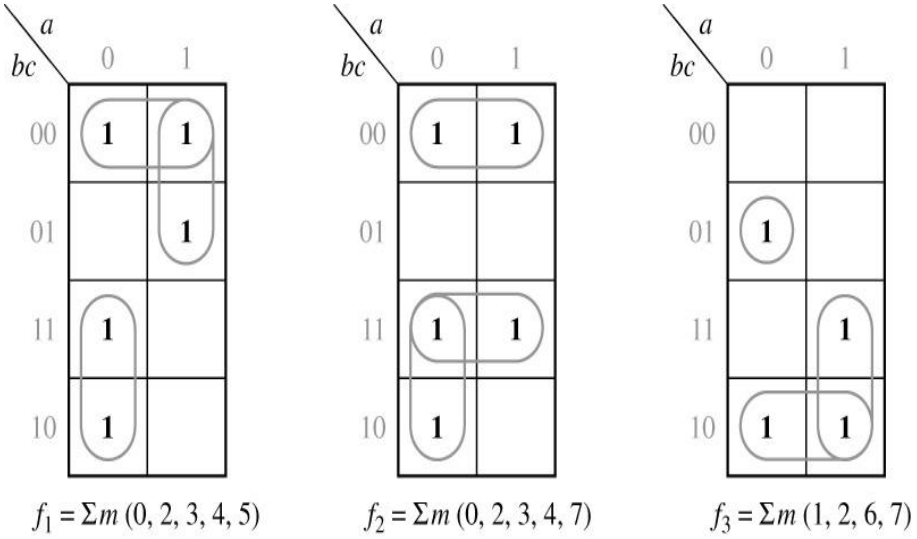


Figure 8-2

Design of Circuits with Limited Gate Fan-in

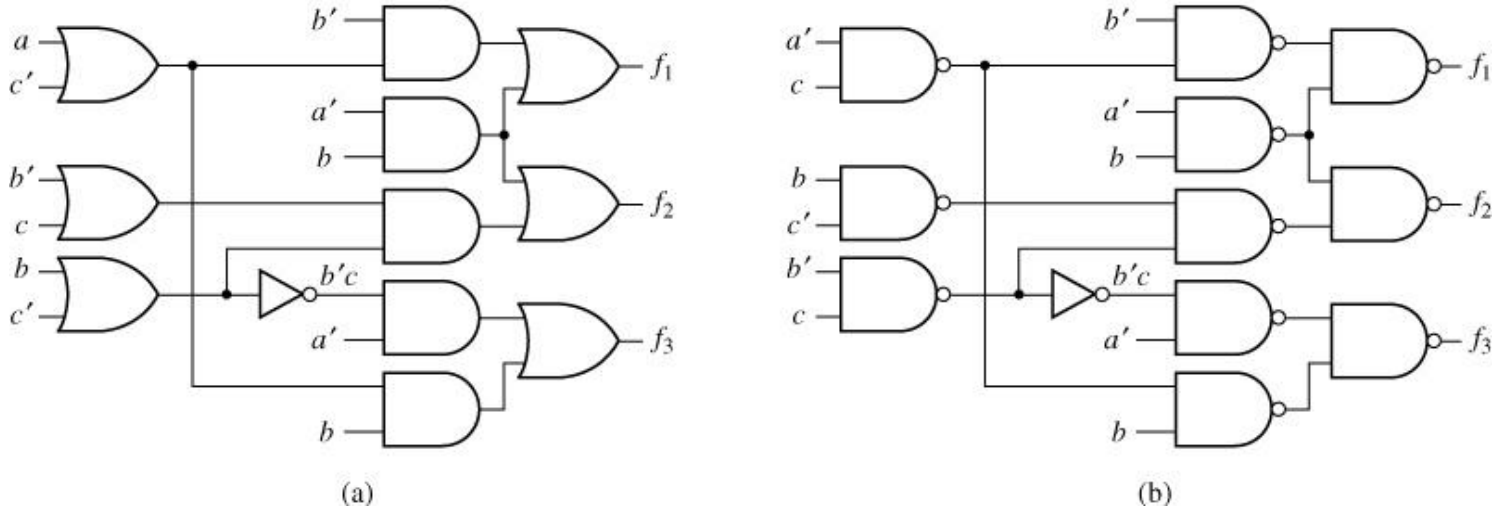


Figure 8-3: Realization of Figure 8-2

$$f_1 = b'(\underline{a'+c'}) + \underline{a'b}$$

$$f_2 = b(a'+c) + \underline{b'c'}$$

$$f_3 = a'b'c + b(\underline{a+c'})$$

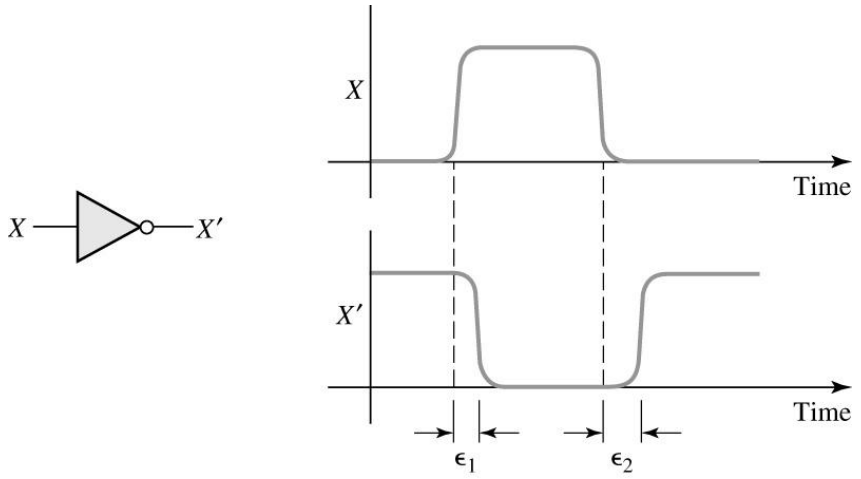
$$f_2 = (b'+c) + (b+c') + \underline{a'b}$$

- Wrong equations!!

$$a'b'c = a'(b'c) = a'(b+c')'$$

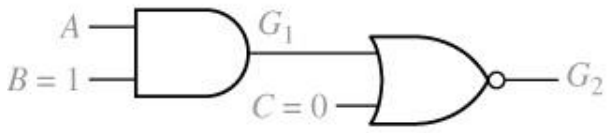
Gate Delays & Timing Diagram

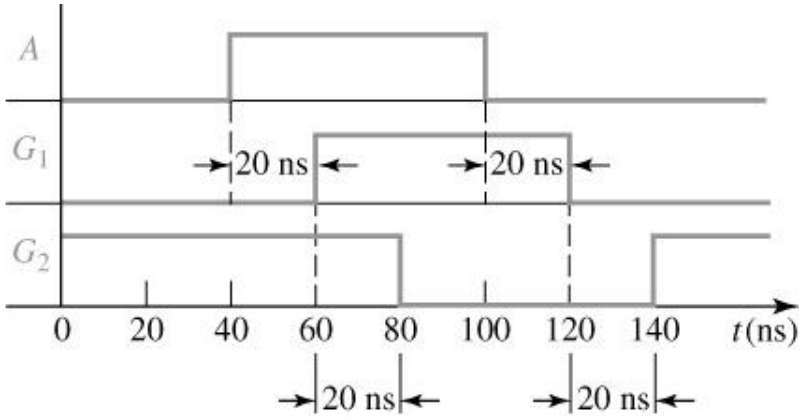
- When input changes, output will not change instantaneously
  - TR or other elements take a finite time to react to a change
  - propagation delays ε are different (for 0-1 & 1-0 change)
  - a few nanoseconds (10^{-9} second) is typical for gates in current process technology
- Propagation delay in inverter
  - take a finite time to react to a change in input



Timing Diagram

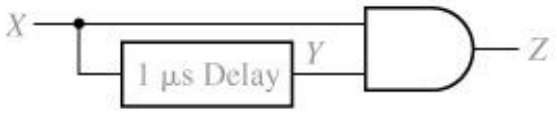
- Frequently used in the analysis of sequential networks
- Shows various signals in the networks as a function of time
- AND-NOR network
  - assume each gate's propagation delay = 20 ns
  - B, C are held at constant values

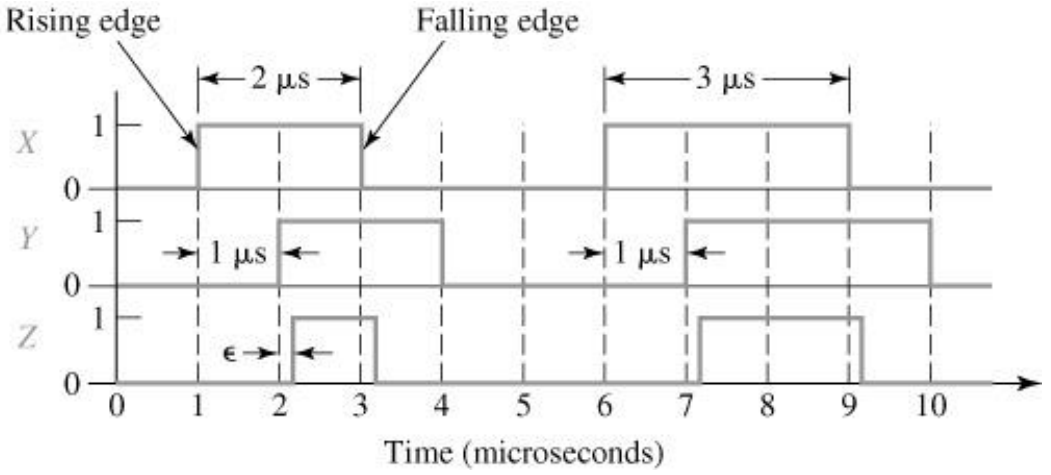




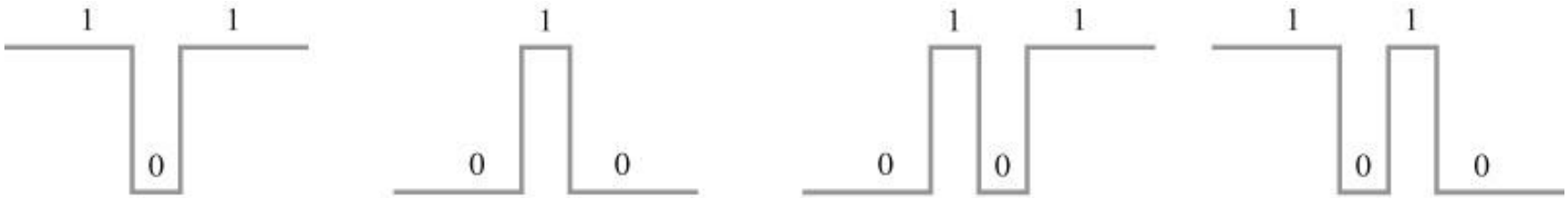
Timing Diagram

- for networks with an added delay element





Hazards in Combinational Logic



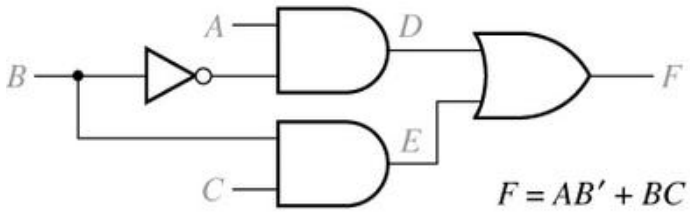
(a) Static 1-hazard (b) Static 0-hazard (c) Dynamic hazards

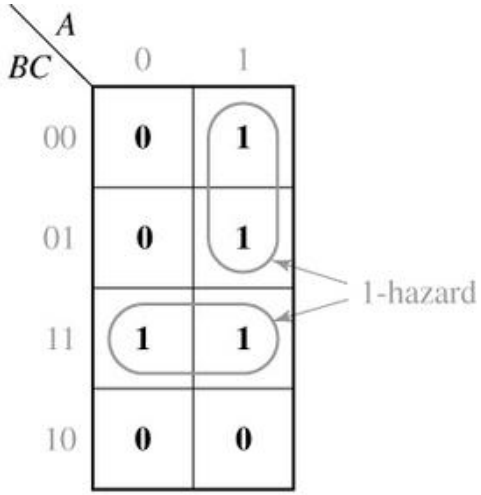
Types of Hazards

Hazards in Combinational Logic

Detection of a 1-Hazard

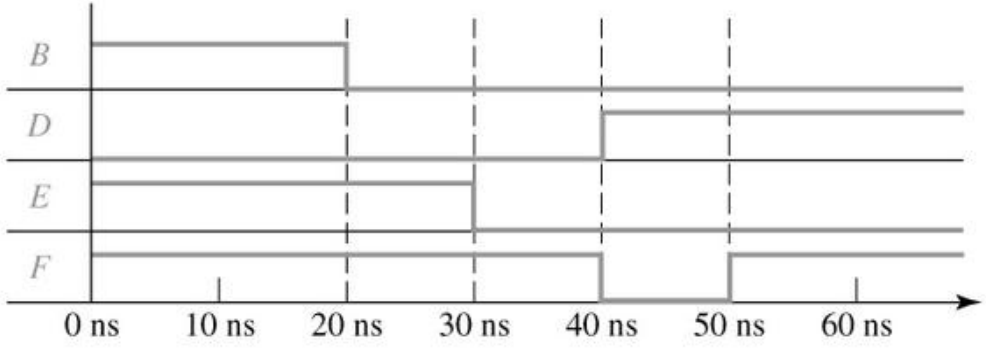
A=C=1, then F should be 1
But??→ glitch





(a) Circuit with a static 1-hazard

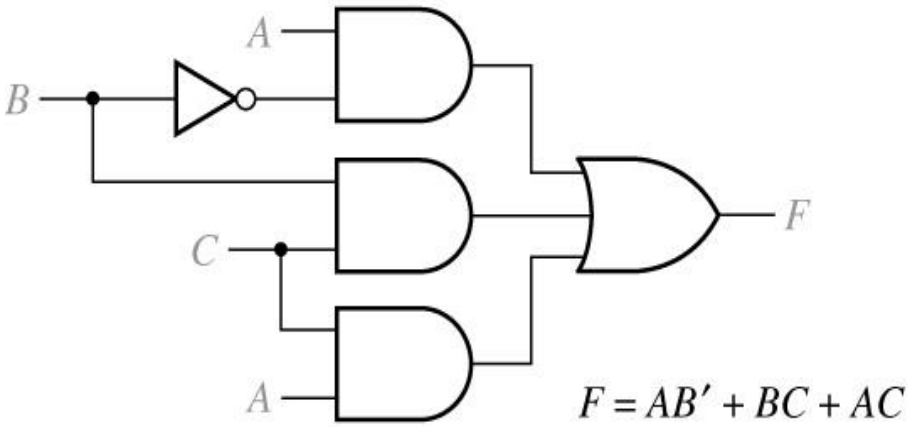
Propagation delay for gates: 10ns

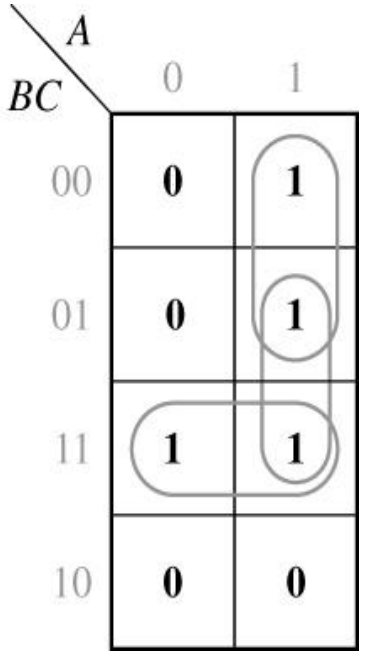


(b) Timing chart

Hazards in Combinational Logic

Circuit with Hazard Removed

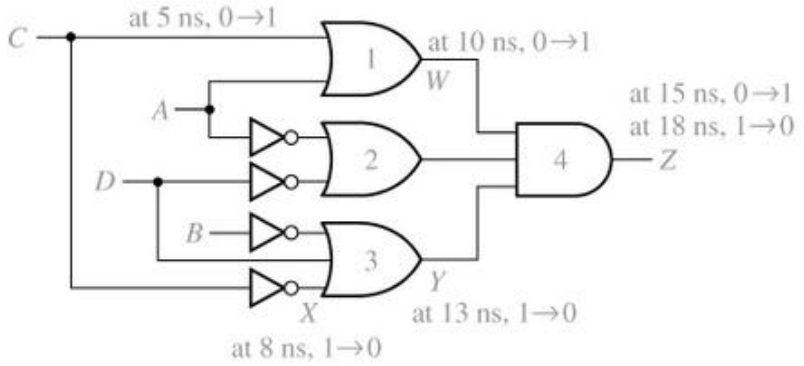




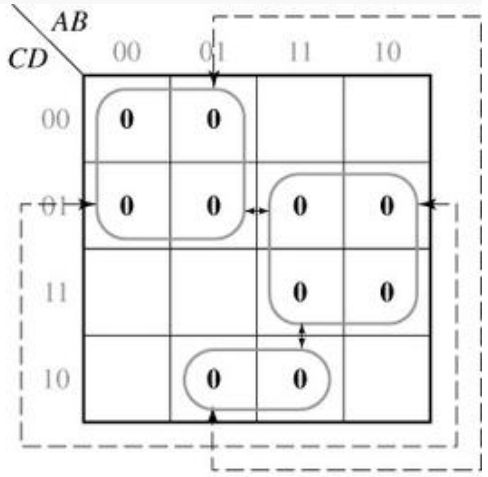
Hazards in Combinational Logic

Detection of a Static 0-Hazard

$$F = (A+C)(A'+D')(B'+C'+D)$$

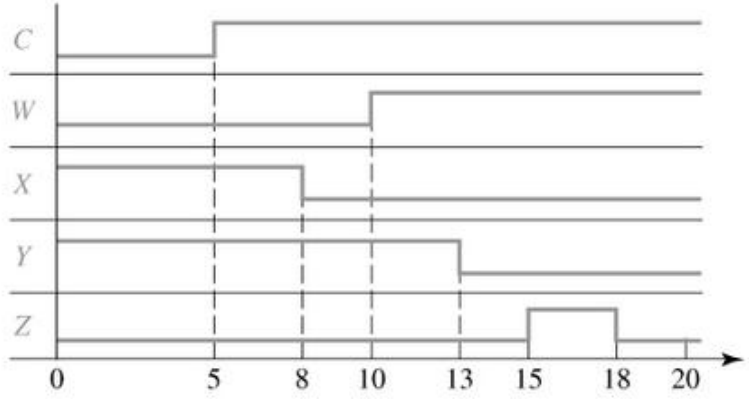


(a) Circuit with a static 0-hazard



(b) Karnaugh map for circuit of (a)

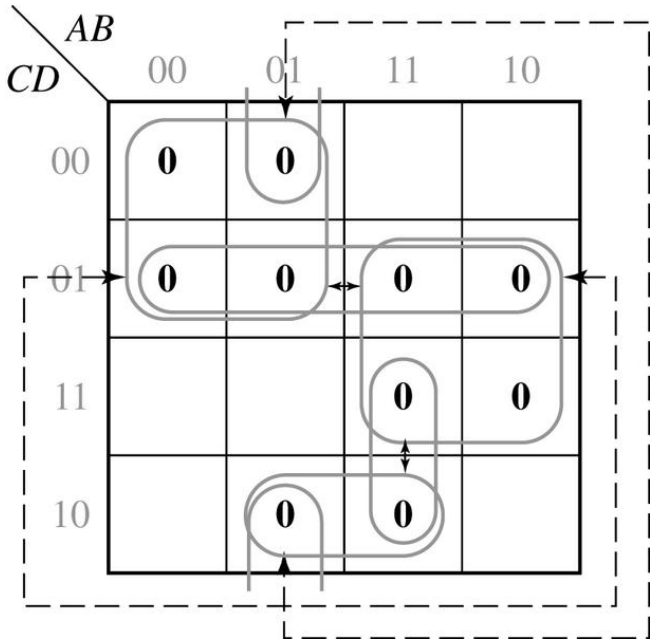
Propagation delay for AND: 3ns, OR: 5ns



(c) Timing diagram illustrating 0-hazard of (a)

Hazards in Combinational Logic

Karnaugh Map Removing Hazards

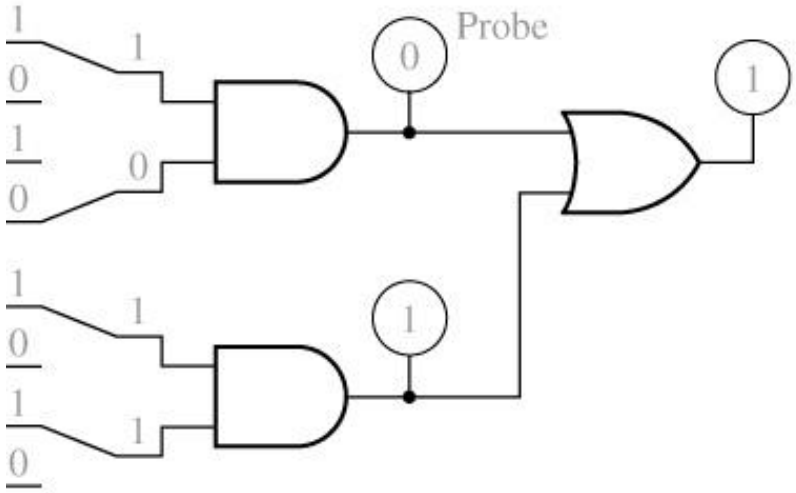


$$F = (A+C)(A'+D')(B'+C'+D)(C+D')(A+B'+D)(A'+B'+C')$$

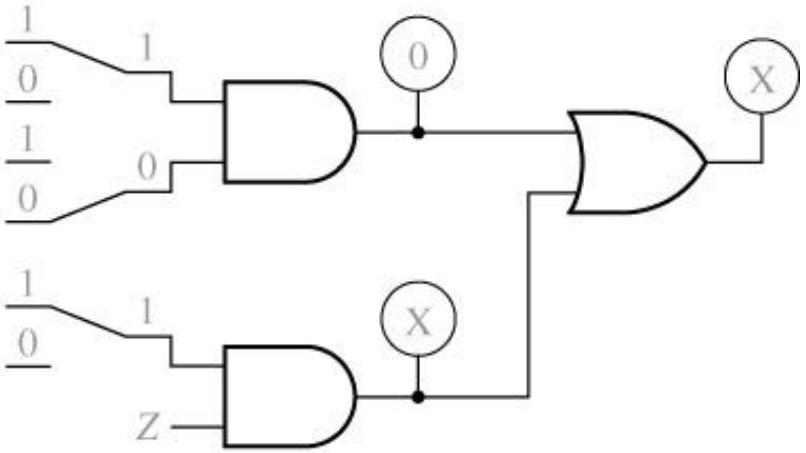
Simulation & Test

- Test of logic circuits
  - by actually building them
  - by simulating them on a computer
- Why do we need simulations?
  - verification of correct design
  - verification of timing of logic signals is correct
  - simulation of faulty components to test ..
- Circuit descriptions
  - by list of connections
  - by logic diagram

Simulation and Testing of Logic Circuit



(a) Simulation screen showing switches



(b) Simulation screen with missing gate input

Simulation and Testing of Logic Circuit

And and OR Functions for Four-Valued Simulation

·	0	1	X	Z
0	0	0	0	0
1	0	1	X	X
X	0	X	X	X
Z	0	X	X	X

+	0	1	X	Z
0	0	1	X	X
1	1	1	1	1
X	X	1	X	X
Z	X	1	X	X

Simulation and Testing of Logic Circuit

Logic Circuit with Incorrect Output

Example: $F = AB(CD'+CD') + A'B'(C+D)$

A=B=C=D=1, but F=1. Why?