Unit 11. Latches and Flip-Flops

Spring 2015

School of Electrical Engineering

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Objectives – To Learn

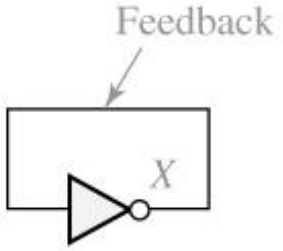
- ⇨ Explain in words the operation of S-R and gated D latches
- ⇨ Explain in words the operation of D, D-CE, S-R, J-K, and T flip-flops
- ⇨ Make a table and derive the characteristic (next-state) equation for such latches and flip-flops. State any necessary restrictions on the input signals
- ⇨ Draw a timing diagram relating the input and output of such latches flip-flops
- ⇨ Show how latches and flip-flops can be constructed using gates. Analyze the operation of a flip-flop that is constructed of gates and latches

Introduction

- Sequential switching networks
  - Output depends on both present inputs and past sequence of inputs
  - Latches & Flip-Flops are most commonly used memory devices
- Latches & Flip-Flops
  - Assume one of two stable output states
  - Has one or more inputs which can cause the output state to change
  - Latch : a memory element that has no clock input
  - Flip-Flop : a memory device that changes output state in response to a clock input and not in response to a data input

Feedback

- Feedback
  - output of one gate is connected back into the another gate's input so as to form a closed loop
  - needed to construct a switching circuit which has a memory
- Inverter with feedback
  - oscillate back and forth between 0 and 1
  - never reach a stable condition
  - oscillation rate is determined by the inverter's propagation delay



(a) Inverter with feedback

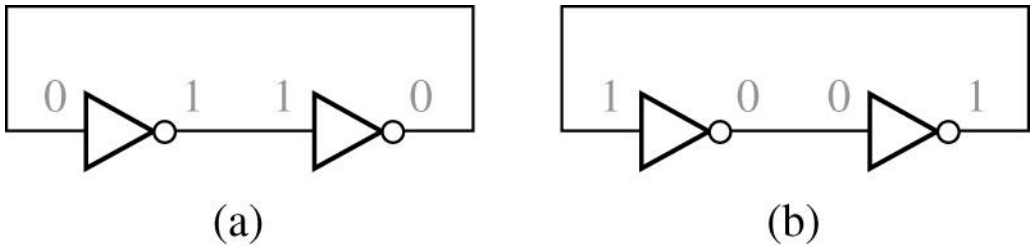
(b) Oscillation at inverter output

Introduction

Two inverters with feedback
two stable conditions –
stable states

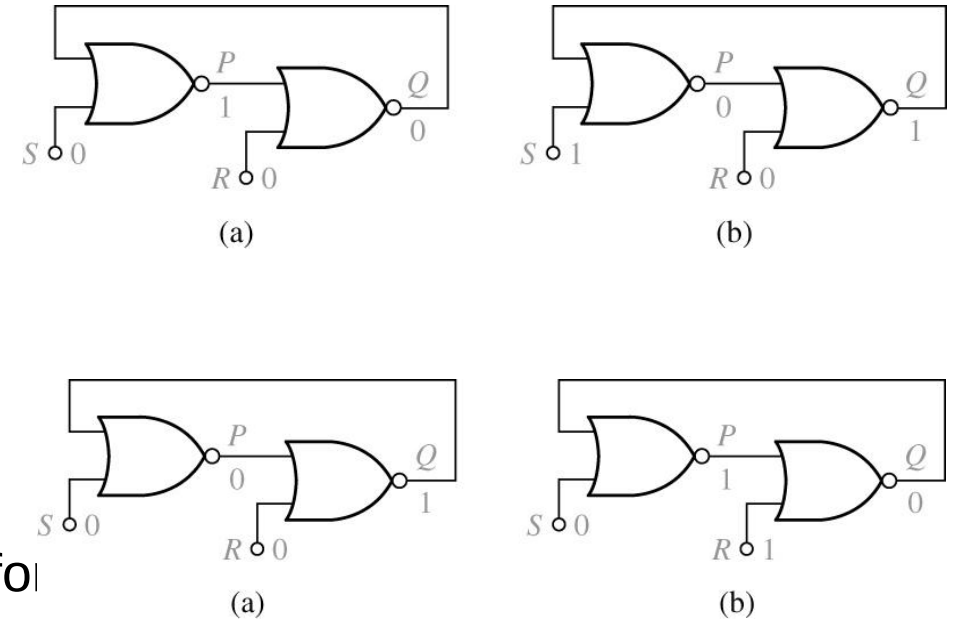
Fig 11-2.

➔ Stable state



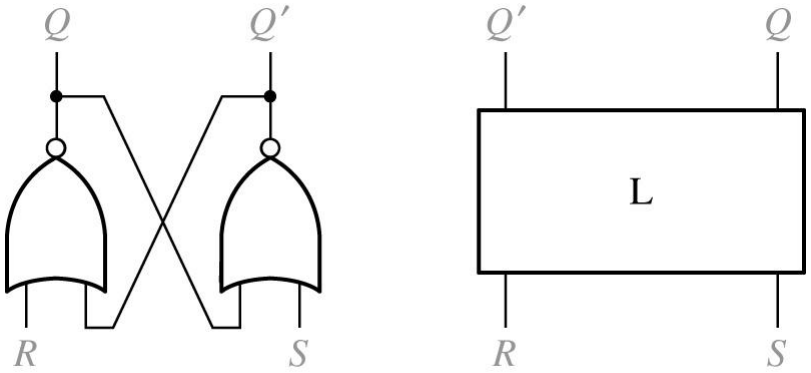
Set–Reset Latch (S–R Latch)

- can make a simple Latch by using a feedback
- Operations :
  - S=R=0, Q=0, P=1?
    - stable? yes
  - becomes S=1
    - S=1, R=0 P=0, Q=1
  - S=0 again. Then?
    - P=0, Q=1
  - R=1 – Q=0, P=1
  - R=0 : go back to first
  - Two different stable state fo a given set of inputs
  - R=S=1을 허용하지 않으며 항상 P=Q'



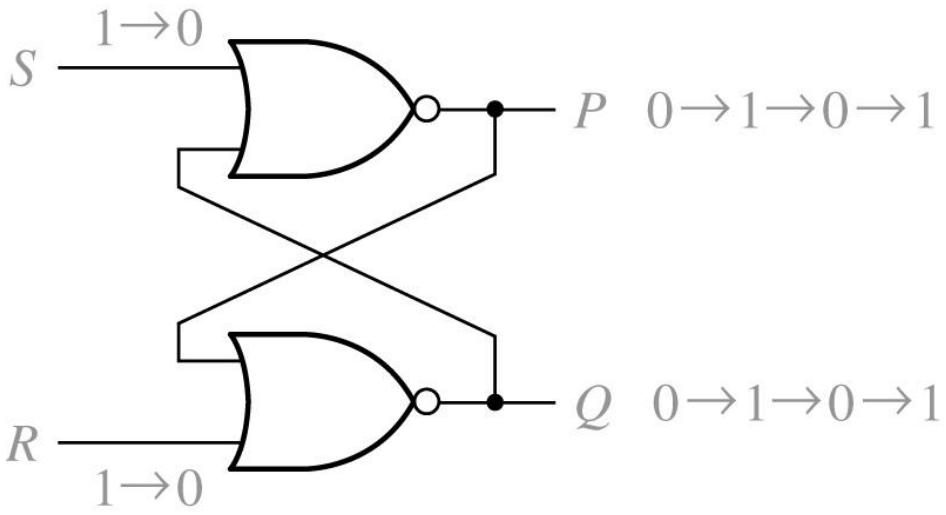
SR Latch : Cross–Coupled Structure

- To emphasize the symmetry, SR latch is often drawn in cross-coupled form
- Although Q comes out of NOR gate with R input, the symbol has Q directly above S input



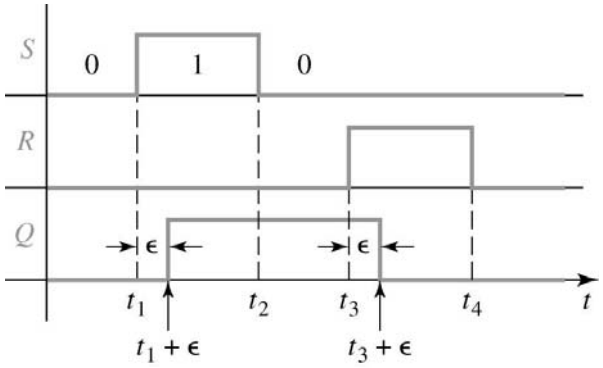
Improper S-R Latch Operation

- What if S=R=1?
  - P=Q=0 (violate basic rule of latch operation that requires the latch outputs to be complements)
  - if S & R change back to 0, P=Q=1 and .. (oscillate if the gate delays are exactly equal)



Set–Reset Latch

Fig 11-7. Timing Diagram for S-R Latch



ε : response time or delay time of the latch

Table 11-1. S-R Latch Operation

S R Q^+

0 0 Q

0 1 0 ←

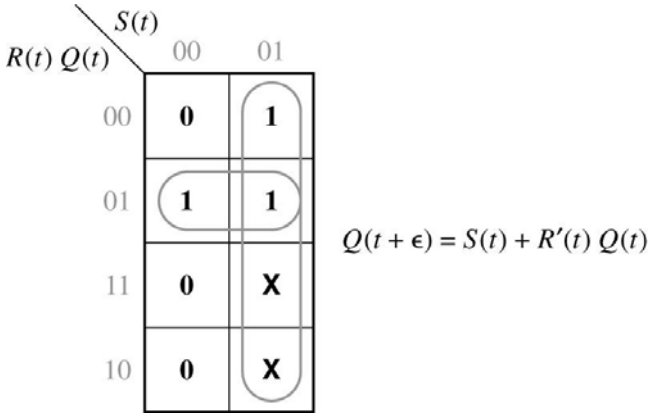
1 0 1

1 1 -

$S(t)$	$R(t)$	$Q(t)$	$Q(t+\varepsilon)$	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	-	} Inputs not allowed
1	1	1	-	

Set–Reset Latch

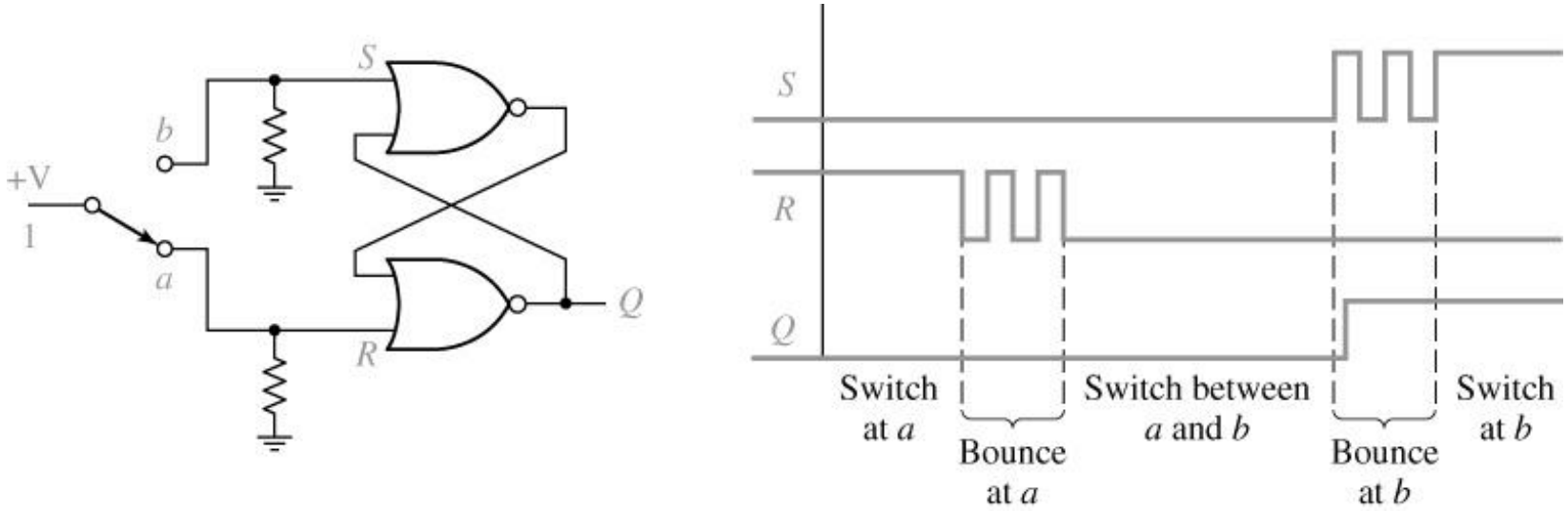
Fig 11-8. Map for $Q(t+\varepsilon)$



$Q(t+\epsilon) = S(t) + R'(t)\,Q(t)$ ⟶ $Q^+ = S + R'Q \qquad (SR = 0)$

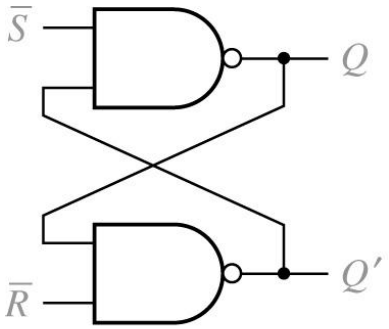
next-state equation(다음상태 방정식) or
characteristic equation(특성방정식)

Switch Debouncing with an S–R Latch

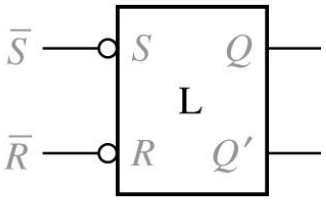


Alternative Form of Set–Reset Latch

$\overline{S} - \overline{R}$ Latch



(a)

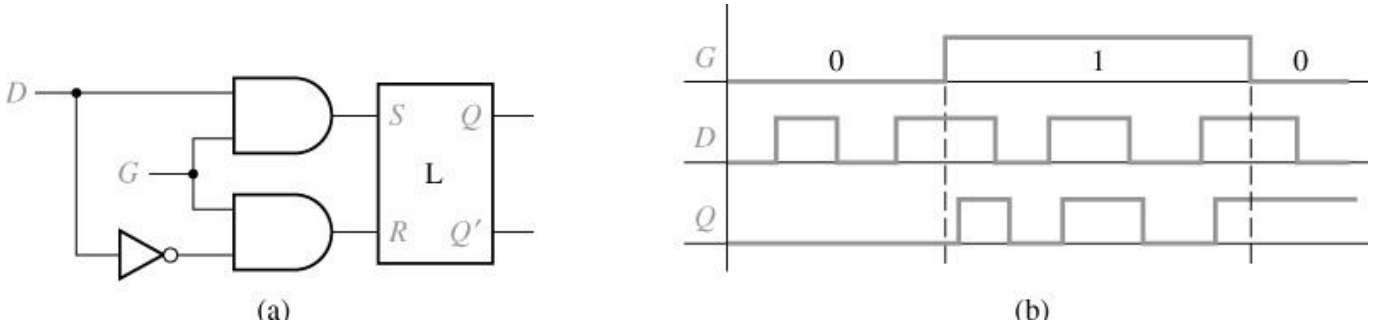


(b)

$\overline{S}$	$\overline{R}$	Q	Q^+	
1	1	0	0	
1	1	1	1	
1	0	0	0	
1	0	1	0	
0	1	0	1	
0	1	1	1	
0	0	0	-	} Inputs not allowed
0	0	1	-	

(c)

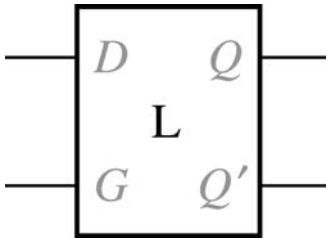
Gated D Latch



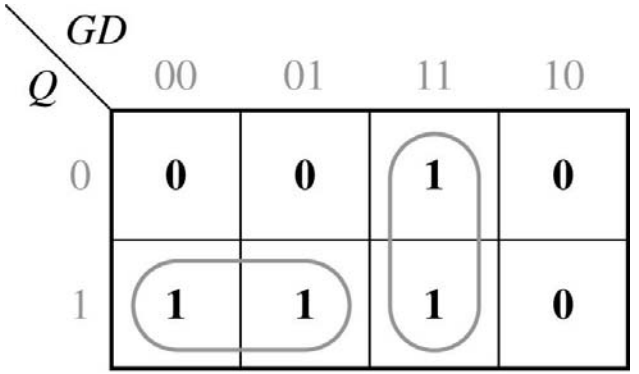
- Two inputs : D, G
  - when G=0 → S=R=0 ☞ Q does not change
  - when G=1, D=1, S=1, R=0 ☞ Q=1
  - when G=1, D=0, S=0, R=1 ☞ Q=0
- ☞ when G=1, the Q output follows D input
  when G=0, Q does not change
- Transparent latch

Gated D Latch

Figure 11-12. Symbol and Truth Table for Gated Latch



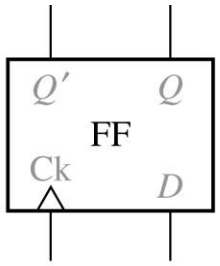
G	D	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



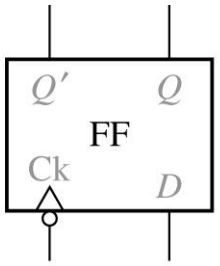
$$Q^+ = G'Q + GD$$

Edge-Triggered D Flip-Flop

Figure 11-13. D Flip-Flops



(a) Rising-edge trigger



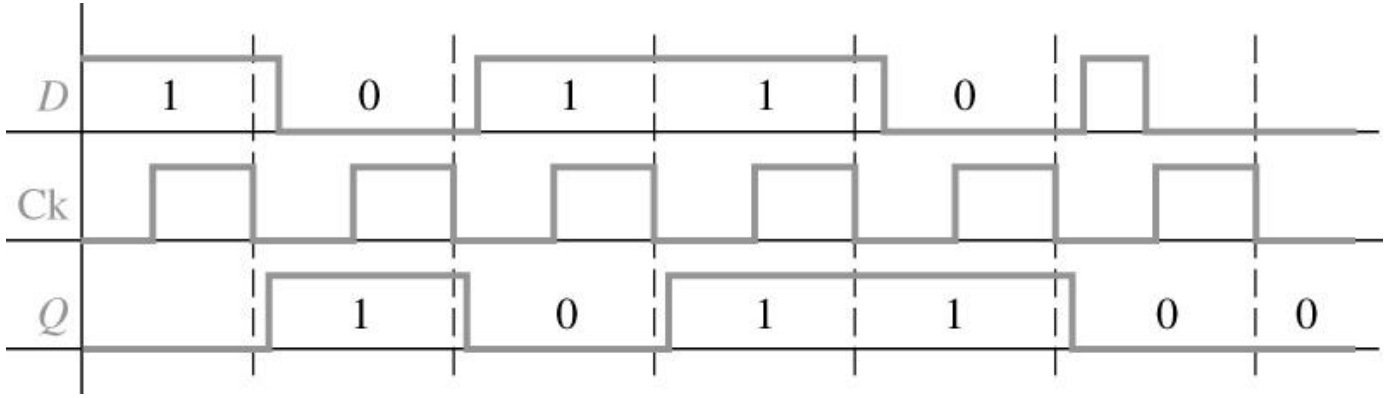
(b) Falling-edge trigger

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

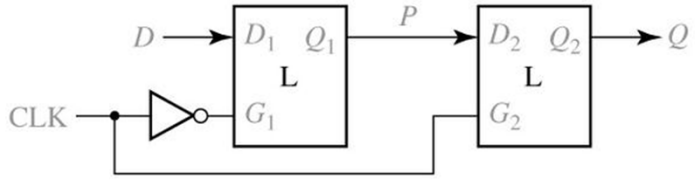
(c) Truth table

$$Q^+ = D$$

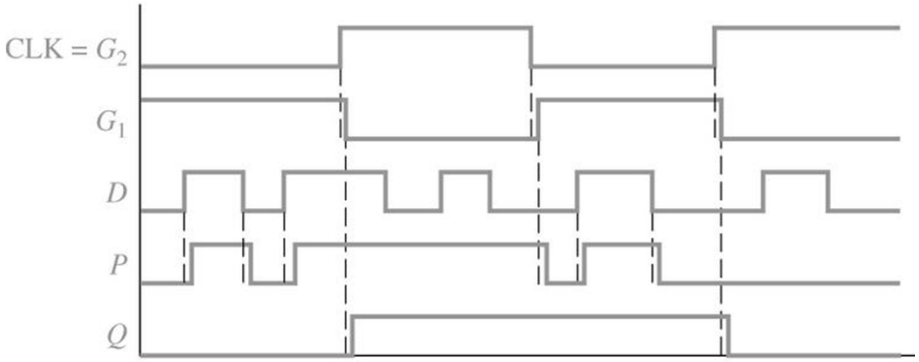
Figure 11-14. Timing for D Flip-Flop (Falling-Edge Trigger)



Rising-Edge-Triggered D F/F



(a) Construction from two gated D latches

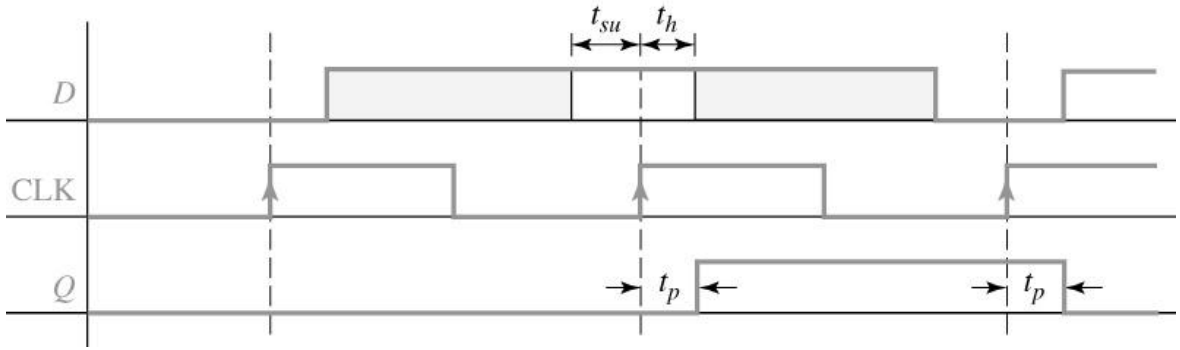


(b) Time analysis

- CLK=0, G1=1
  - P output follows D input
  - since G2=0, 2nd latch hold current Q
- CLK=1, G1=0
  - current D is stored in 1st latch
  - since G2=1, P flows thru 2nd latch to Q output

Edge-Triggered D Flip-Flop

Figure 11-16. Setup and Hold Times for an Edge-Triggered D Flip-Flop



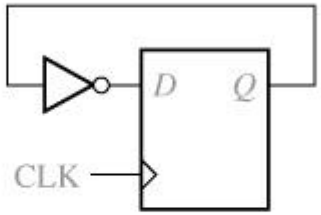
t_{su} : the setup time

t_h : the hold time

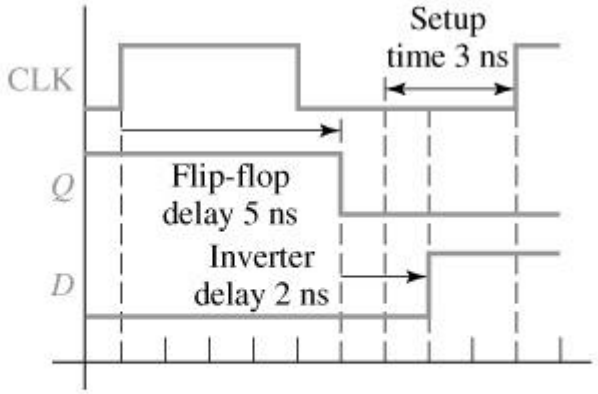
t_p : the propagation delay

Edge-Triggered D Flip-Flop

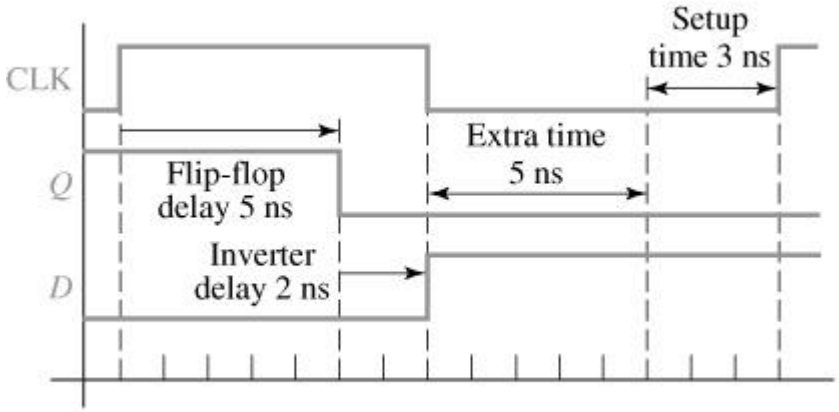
Figure 11-17. Determination of Minimum Clock Period



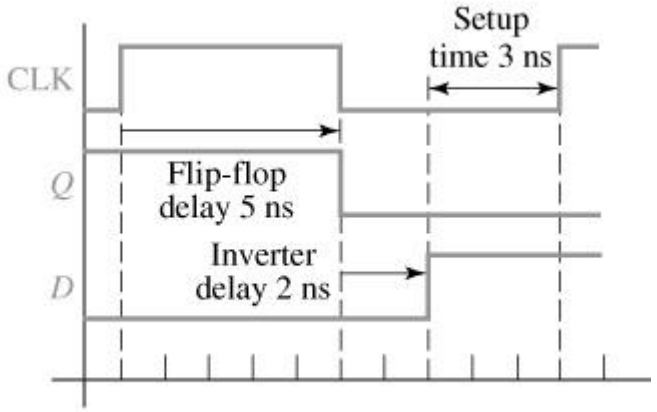
(a) Simple flip-flop circuit



(b) Setup time not satisfied



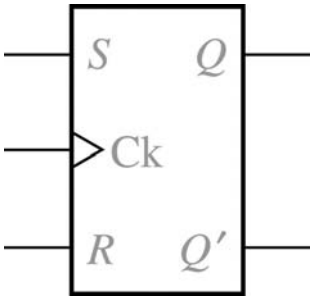
(c) Setup time satisfied



(d) Minimum clock period

S–R Flip–Flop

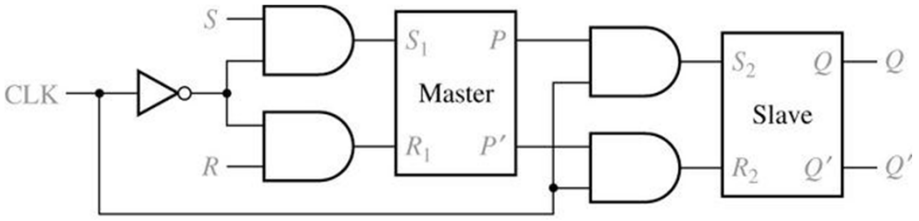
Figure 11-18. S-R Flip-Flop



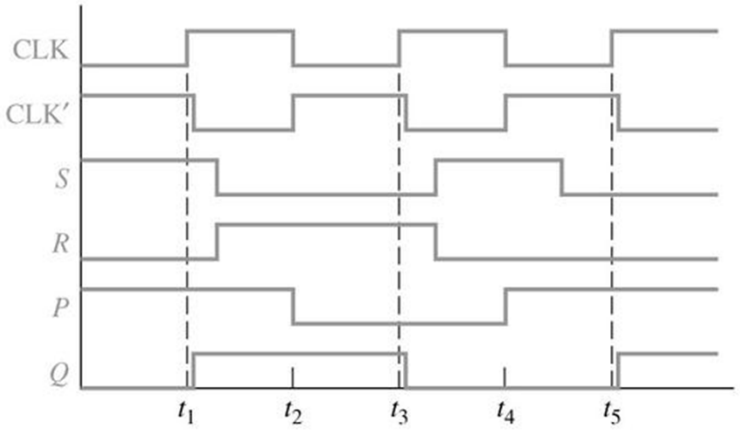
Operation summary :

S=R=0	No state change
S=1, R=0	Set Q to 1 (after active Ck edge)
S=0, R=1	Reset Q to 0 (after active Ck edge)
S=R=1	Not allowed

S-R F/F Implementation & Timing



(a) Implementation with two latches



(b) Timing analysis

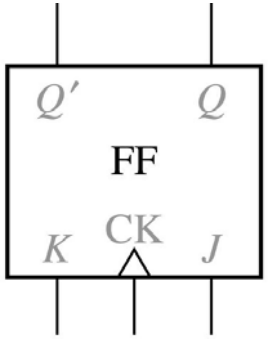
- constructed from two S-R latches & gates
- master-slave F/F
- ML : master latch, SL : slave latch

- CLK=0
  - ML's output : appropriate value
  - SL hold prev. value Q (S_2=R_2=0)
- CLK 0→1
  - ML's P output is transferred to SL
- CLK=1
  - ML holds P
  - Q does not change
- CLK 1→0
  - Q(P?) value is latched in SL
  - ML processes new input

- Problem at t5?
  - → S & R inputs to change while the clock is high

J–K Flip–Flop

Figure 11-20. J-K Flip-Flop (Q Changes on the Rising Edge)

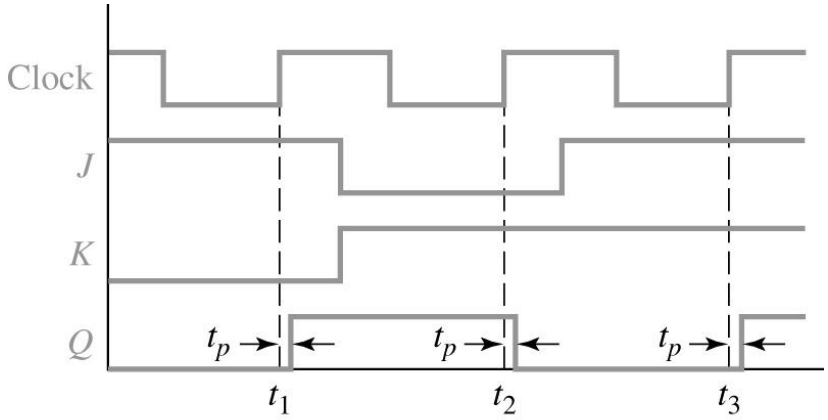


(a) J-K flip-flop

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b) Truth table and characteristic equation

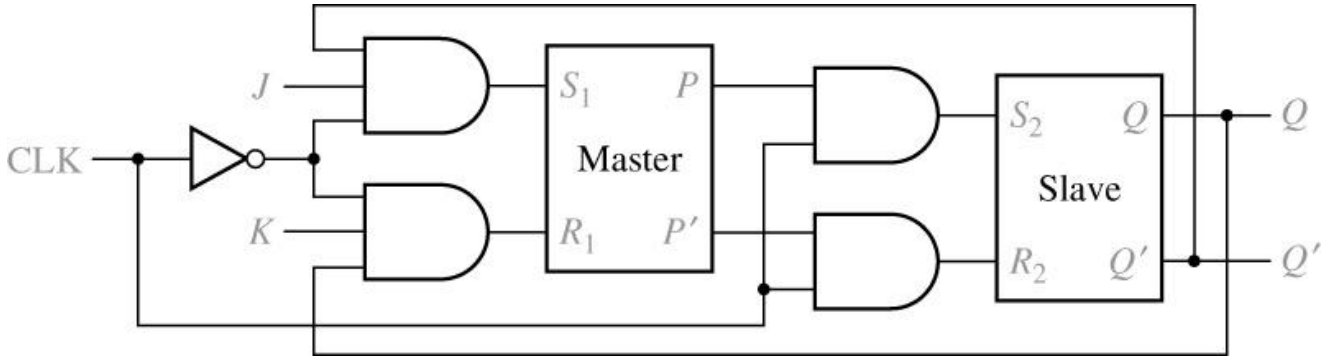
$$Q^+ = JQ' + K'Q$$



(c) J-K flip-flop timing

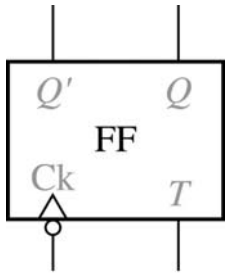
J–K Flip–Flop

Figure 11-21. Master-Slave J-K Flip-Flop (Q Changes on Rising Edge)



T Flip–Flop

Figure 11-22. T Flip-Flop



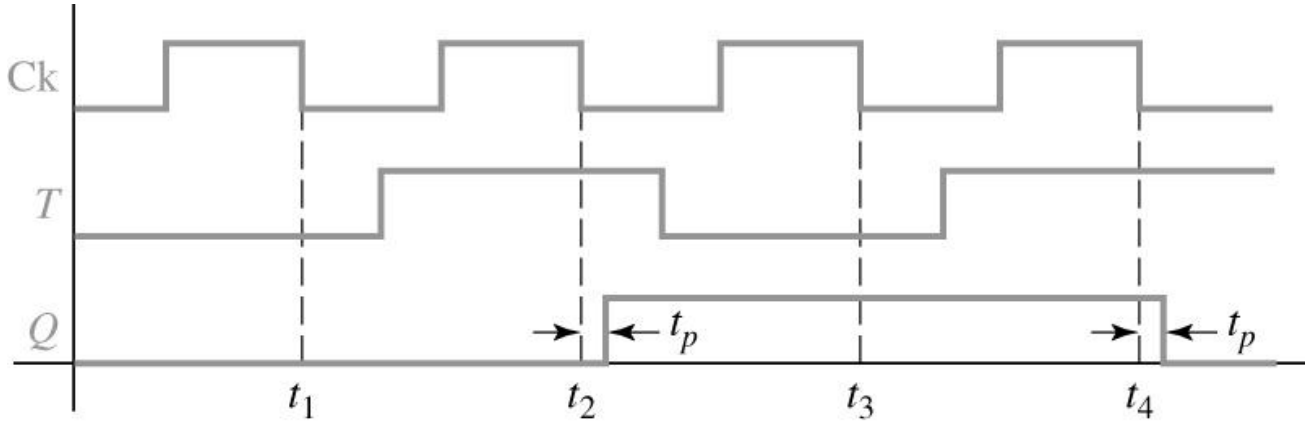
(a)

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

(b)

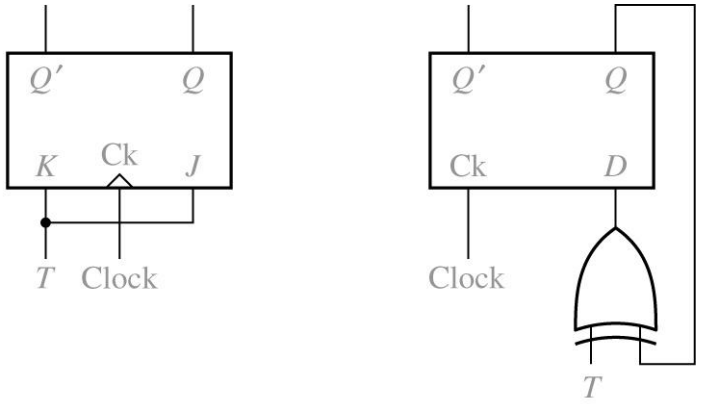
$$Q^+ = T'Q + TQ' = T \oplus Q$$

Figure 11-23. Timing Diagram for T Flip-Flop (Falling-Edge Trigger)



T Flip–Flop

Figure 11-24. Implementation of T Flip-Flop



(a) Conversion of J-K to T (b) Conversion of D to T

$$Q^+ = JQ' + K'Q = TQ' + T'Q$$

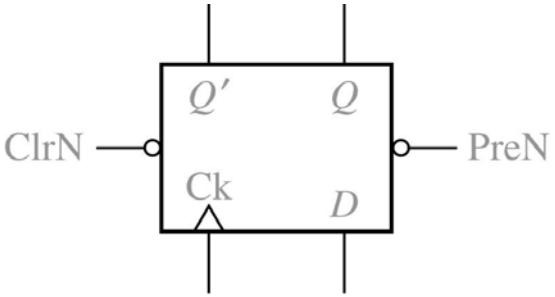
$$Q^+ = D = T \oplus Q = TQ' + T'Q$$

Flip-Flops with Additional Inputs

- additional inputs to set the F/F to an initial state independent of the clock
- active-low signals ☞
- ClrN=0 → Q=0
  PreN=0 → Q=1로 됨
- ClrN=PreN=1 → normal operation
- ClrN, PreN override the clock & D input

Flip–Flops with Additional Inputs

Figure 11-25. D Flip-Flop with Clear and Preset

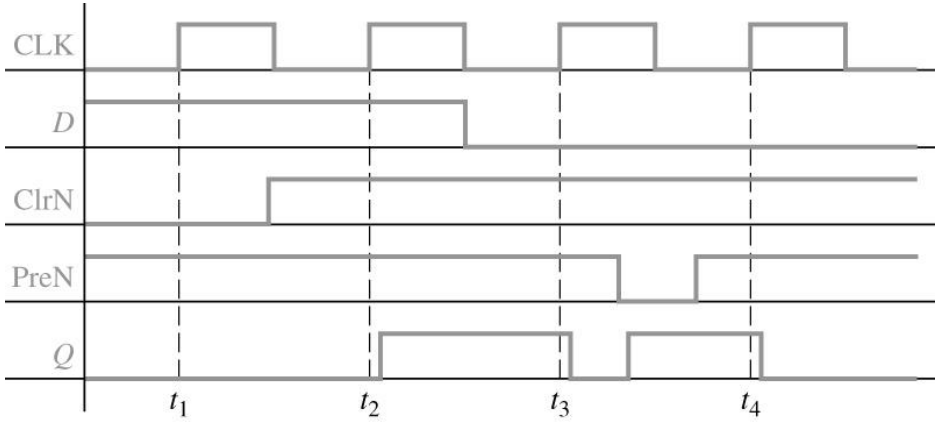


(a)

Ck	*D*	PreN	ClrN	Q^+
x	x	0	0	(not allowed)
x	x	0	1	1
x	x	1	0	0
↑	0	1	1	0
↑	1	1	1	1
0,1,↓	x	1	1	Q(no charge)

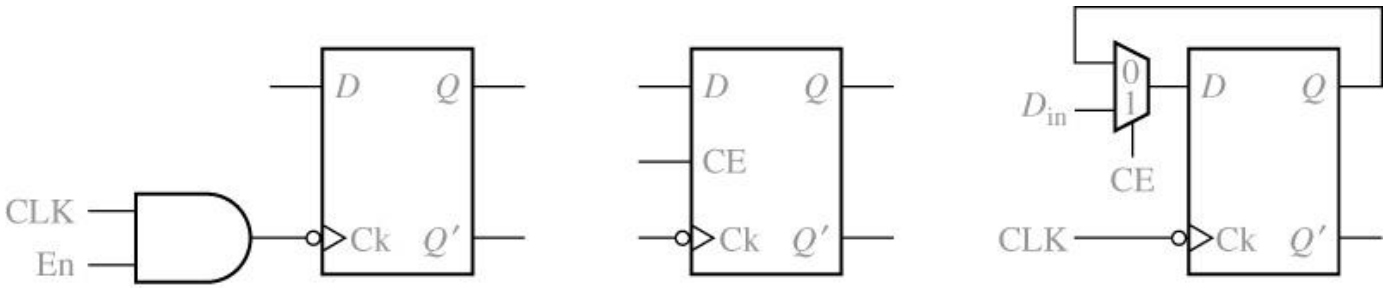
(*b*)

Figure 11-26. Timing Diagram for D Flip-Flop with Asynchronous Clear and Preset



Flip–Flops with Additional Inputs

Figure 11-27. D Flip-Flop with Clock Enable



The characteristic equation : $Q^+ = Q \cdot CE' + D \cdot CE$

The MUX output : $Q^+ = D = Q \cdot CE' + D_{in} \cdot CE$

Summary

$Q^+ = S + R'Q \quad (SR = 0)$ (S-R latch or flip-flop)

$Q^+ = GD + G'Q$ (gated D latch)

$Q^+ = D$ (D flip-flop)

$Q^+ = D \cdot CE + Q \cdot CE'$ (D-CE flip-flop)

$Q^+ = JQ' + K'Q$ (J-K flip-flop)

$Q^+ = T \oplus Q = T'Q + TQ'$ (T flip-flop)