**Tsung-Wei Huang**

**Education**

Ph.D Computer Engineering University of Illinois at Urbana-Champaign 2017

M.S. Computer Science Taiwan’s National Cheng Kung University 2011

B.S. Computer Science Taiwan’s National Cheng Kung University 2010

**Academic and Professional Experience**

University of Wisconsin-Madison Assistant Professor 2023-present Full Time

University of Utah Assistant Professor 2019-2023 Full Time

University of Illinois Research Assistant Professor 2018-2019 Full Time

**Professional Credentials, Certifications, or Liscensing**

None

**Recent Professional Development Activities**

Professional Conferences and Industry Meetings

* ACM/IEEE Design Automation Conference
* ACM/IEEE International Conference on Computer-aided Design
* ACM International Conference on Parallel Processing
* IEEE International Parallel & Distributed Processing Symposium
* NSF AI Institute at University at Buffalo Meeting
* International Symposium on High-Performance Parallel and Distributed Computing
* ACM/IEEE Supercomputing Conference
* IEEE Computer Society Annual Symposium on VLSI

**Contributions to the Discipline**

**Honors and Awards**

* Innovation Award, IEEE HPEC Sparse Deep Neural Network Graph Challenge, 2023
* Innovation Award, IEEE HPEC Streaming Graph Challenge, 2023
* ACM SIGDA Outstanding New Faculty Award, 2023
* ACM SIGDA Meritorious Service Award, 2022
* Humboldt Research Fellowship Award, Alexander von Humboldt Foundation, 2022
* NSF Faculty Early Career Development Program (CAREER) Award, 2022
* Top 15% Instructors, College of Engineering, University of Utah, 2021
* Best Paper Award, ACM TAU Workshop, 2021
* First Place, IEEE HPEC Large Sparse Neural Network Challenge, 2020
* Second Place, Open-source Software Competition, ACM Multimedia Conference, 2019
* ACM SIGDA Outstanding PhD Dissertation Award, 2019

**Professional Organizations**

IEEE Computer Society, ACM Special Interest Group on Design Automation (SIGDA)

**Recent Service Activities**

*University of Utah*

* ECE Department: Graduate Committee
* ECE Department: Faculty Search Committee
* ECE Department: Asia Campus Committee
* ECE Department: Asia Campus Summer Program Committee

*University of Wisconsin-Madison*

* ECE Department: Graduate Committee
* ECE Department: MS Accelerated Committee

*Professional Service*

* Panelist: NSF, DOE, Swiss NSF
* Conference Program Committee: DAC, ICCAD, IPDPS, MLCAD, ISVLSI, SC, ISVLSI, ICCD, ASPDAC, etc.
* Journal Reviewers: TCAD, TPDS, TVLSI, TODAES, TACO, JETC, Software X, TOPC, TBD, etc.
* Workshop Organization: NSF FuSe Workshop on Quantum Computing, DAC Open-source EDA Bird of Feather Meeting

**Select Publications**

1. Chih-Chun Chang, Boyang Zhang, and Tsung-Wei Huang, “GSAP: A GPU-Accelerated Stochastic Graph Partitioner,” ACM International Conference on Parallel Processing (ICPP), Gotland, Sweden, 2024
2. Shui Jiang, Rongliang Fu, Lukas Burgholzer, Robert Wille, Tsung-Yi Ho, and Tsung-Wei Huang, “TaroRTL: Accelerating RTL Simulation using Coroutine-based Heterogeneous Task Graph Scheduling,” ACM International Conference on Parallel Processing (ICPP), Gotland, Sweden, 2024
3. Dian-Lun Lin, Joshua San Miguel, Umit Ogras, Tsung-Wei Huang, “TaroRTL: Accelerating RTL Simulation using Coroutine-based Heterogeneous Task Graph Scheduling,” European Conference on Parallel and Distributed Computing (Euro-Par), Madrid, Spain, 2024
4. Jie Tong, Liangliang Chang, and Umit Ogras, and Tsung-Wei Huang, “BatchSim: Parallel RTL Simulation using Inter-cycle Batching and Task Graph Parallelism,” IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2024
5. Cheng-Hsiang Chiu and Tsung-Wei Huang, “An Experimental Study of Dynamic Task Graph Parallelism for Large-Scale Circuit Analysis Workloads,” IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2024
6. Che Chang, Cheng-Hsiang Chiu, Boyang Zhang, and Tsung-Wei Huang, “Incremental Critical Path Generation for Dynamic Graphs,” IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2024
7. Wan-Luan Lee, Dian-Lun Lin, Tsung-Wei Huang, Shui Jiang, Tsung-Yi Ho, Yibo Lin, and Bei Yu, “G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner,” ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, 2024
8. Che Chang, Tsung-Wei Huang, Dian-Lun Lin, Guannan Guo, and Shiju Lin, “Ink: Efficient Incremental k-Critical Path Generation,” ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, 2024
9. Boyang Zhang, Dian-Lun Lin, Che Chang, Cheng-Hsiang Chiu, Bojue Wang, Wan-Luan Lee, Chih-Chun Chang, Donghao Fang, and Tsung-Wei Huang, “G-PASTA: GPU Accelerated Partitioning Algorithm for Static Timing Analysis,” ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, 2024
10. Shiju Lin, Guannan Guo, Tsung-Wei Huang, Weihua Sheng, Evangeline Young, and Martin Wong, “GCS-Timer: GPU-Accelerated Current Source Model Based Static Timing Analysis,” ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, 2024