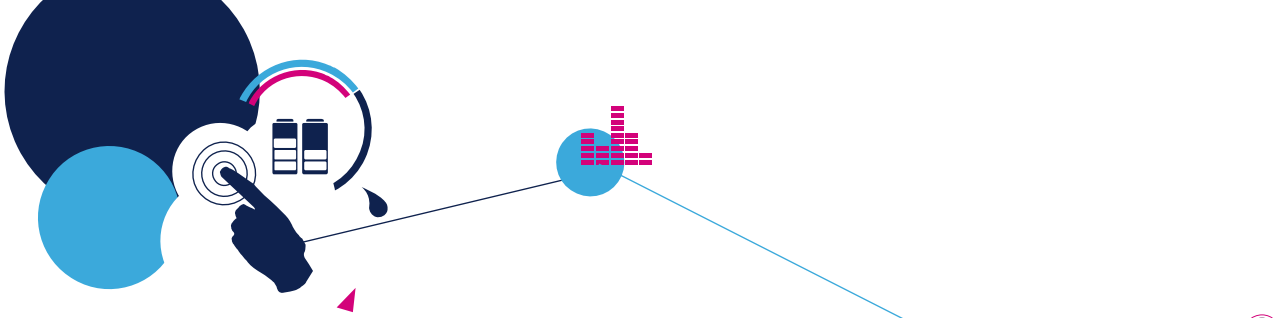

STM32G4 Mainstream Series Mixed Signals MCU

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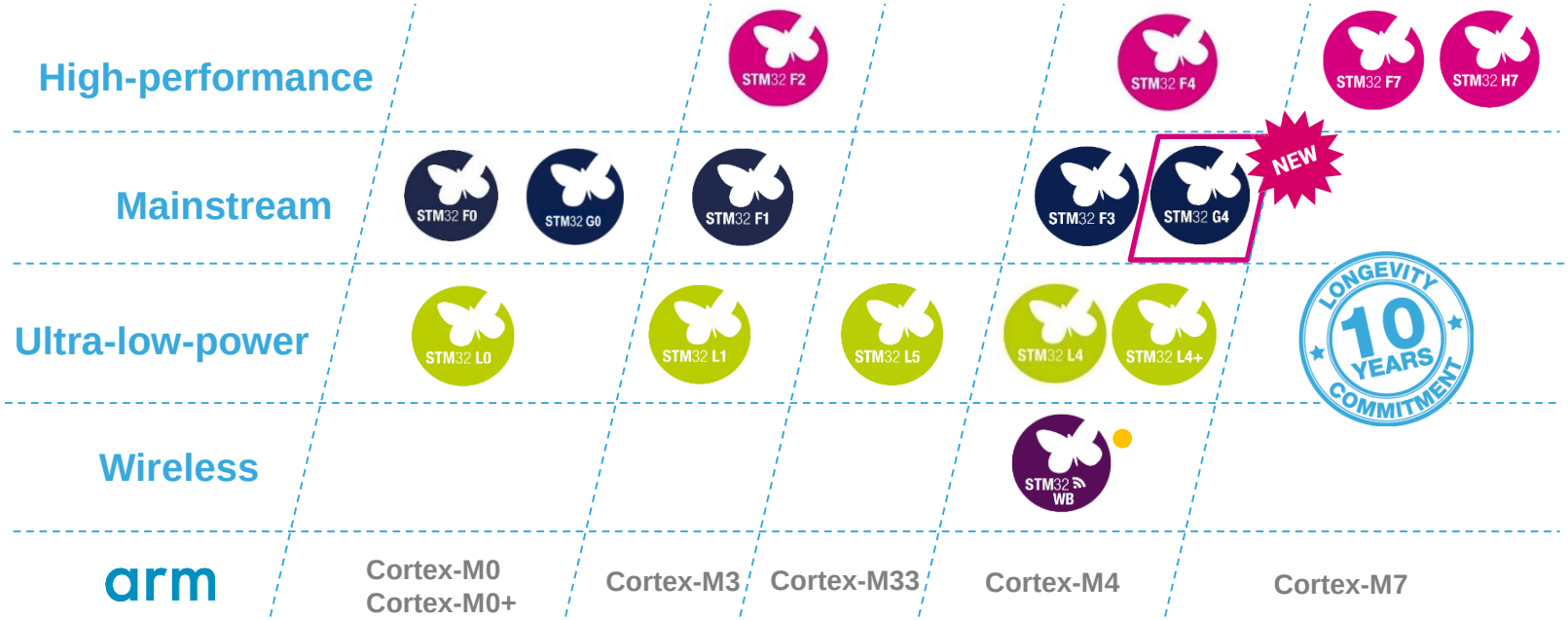
STM32G4: Continuity in STM32 MCUs

Keep releasing your growing creativity



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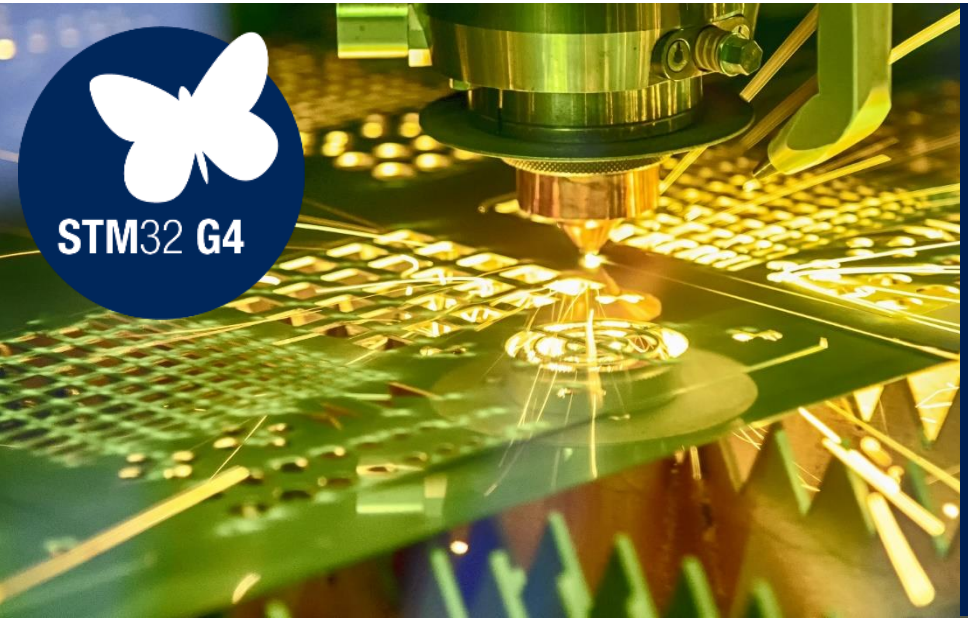
G4 = Next Generation of F3 series

- **Gain in robustness, Safety, Security**
  - ✓ EMC (EMI, EMS) → continuous improvement
  - ✓ **Dual Bank** Flash w/ ECC (Live FW Upgrade)
  - ✓ HW encryption AES
  - ✓ **Securable Memory Area**
- **Gain in Performance**
  - ✓ **170MHz** even from internal oscill. (**213DMIPS**)
    1. ART accelerator (~dynamic cache)
    2. CCM-SRAM Routine Booster (~static cache)
    3. **Mathematical accelerator** (Trigo, Filtering)
  - ✓ Better dynamic power conso (160µA/Mhz) = ~2.7 times lower than F3 series
- **Gain in Peripheral set and Architecture**
  - ✓ **1%** RC accuracy [-5°..90°C], 2% full range
  - ✓ ADC with HW oversampling = 16-bit resolution
  - ✓ Renewed Op-Amp, DAC, Comparator
  - ✓ New HR timer features (digital part)
  - ✓ MC timer improvements (encoder mode…)
  - ✓ USB type-C with Power Delivery incl. PHY
  - ✓ 85°, 105° and up to **125°C** (limited condition)
- **STM32 F3 portfolio extension**
  - ✓ D-Power portfolio (STM32F334) extension
  - ✓ **NEW 128pin** and **80pin** package (LQFP)

STM32G4 Series

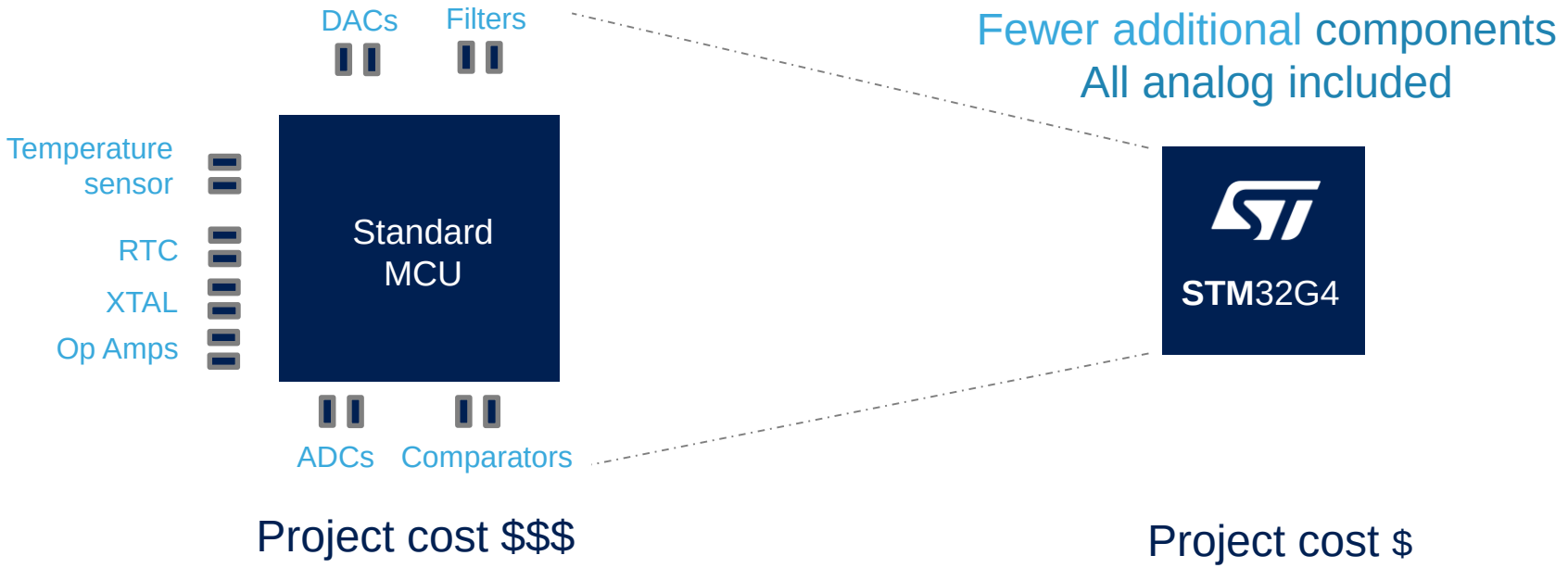
Ideal for applications requiring MCU with advanced and rich analog peripherals



- Control applications (Motor Control…)
- Industrial equipment
- Instrumentation and Measurement
- Digital Power
  - Digital SMPS (switch mode power supply)
  - PFC (power factor correction)

Reducing PCB Size and BOM Cost

System-on-Chip – All-in-one solution



STM32G4 Series – Key Messages

Performance

- Arm® Cortex®-M4 at 170 MHz
- 213 DMIPS and 550 CoreMark® results
- Better dynamic power consumption (163µA/MHz)
- ART Accelerator™ (dynamic cache)
- Mathematical accelerators
- CCM-SRAM Routine Booster (static cache)

Rich Integrated Analog and Digital

- Op-Amps (Built-in gain), DACs, Comparators
- 12-bit ADCs 4Msps with hardware oversampling
- CAN-FD (flexible data rate – 8Msps bit rate)
- High resolution timer (184 ps)
- USB type-C Power Delivery3.0
- 1% RC accuracy [-5°..90°C], 2% full T° range

Safety and security focus

- Dual Bank Flash with ECC (error code correction)
- Securable Memory Area
- Hardware encryption AES-256
- SIL, Class-B

SRAM with Parity bit

Secure Live Upgrade

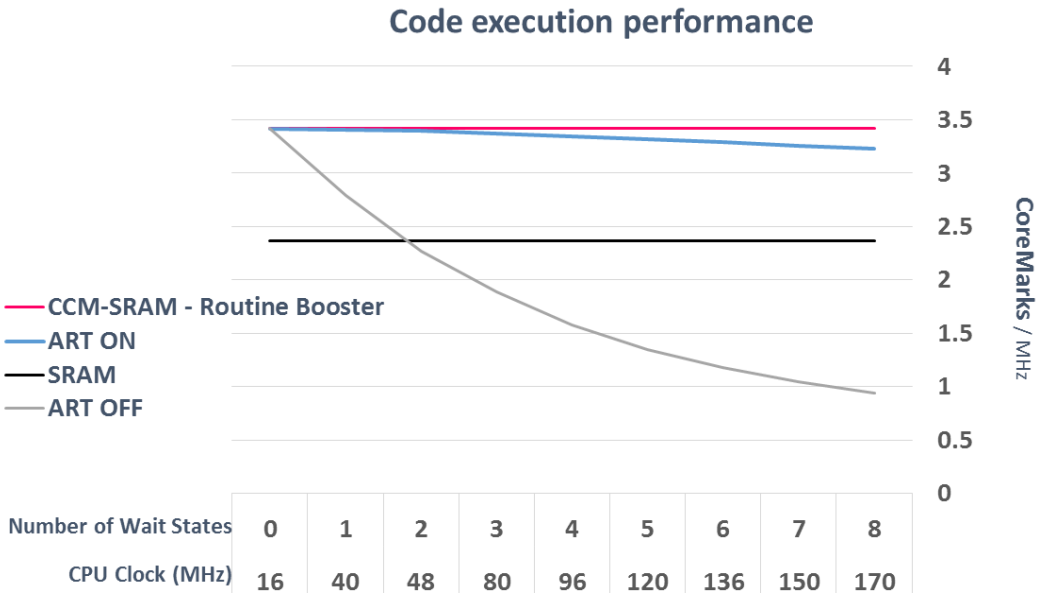
Functional safety design packages

Complete portfolio

- Complements existing STM32F3 Series portfolio
- From -40°c up to 85 or 125°C devices
- From 32- up to 128-pin
- From 32KB to 512KB Flash

Greater Performance

Pure 170 MHz CPU performance (Arm® Cortex®-M4) with 3 accelerators



Arm Cortex-M4 with **FPU**

Up to 170 MHz CPU frequency

Up to 213 DMIPS and 550 CoreMark® results

3 different **HW accelerators**:

- **ART accelerator** (~dynamic cache) → Full code acceleration (average)
- **Routine Booster** CCM-SRAM (~static cache) → determinism preserved
- **Mathematical** (Cordic + FMAC)

NEW

Mathematical Accelerators

NEW

Function acceleration and CPU offload

1. Cordic (Trigo)

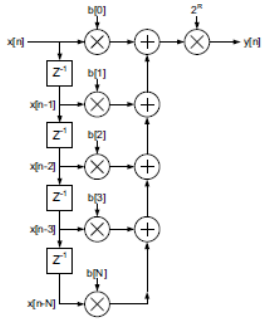
- Very helpful for Field Oriented Motor Control method (FOC)

- Vector rotation (polar to rectangular): Sin, Cos
- Vector translation (rectangular to polar): Atan2, Modulus
- Sinh, Cosh, Exp
- Atan, Atanh
- Square root
- Ln

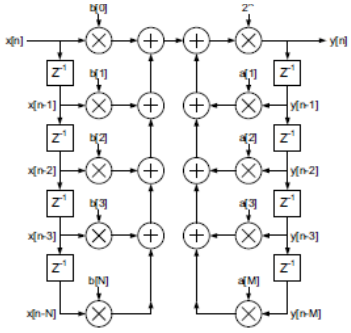
2. Filter Math ACcelerator (FMAC)

- Can be used to create
  - 3p3z Compensator (→ Digital power)
  - Sigma Delta modulator
  - Noise Shaper

FIR filter



IIR filter



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Rich, Advanced Analog

Mixed-signal SoC for wide variety of applications

ADC (up to 5)	Values
Topology	**SAR 12-bit** + HW oversampling → **16-bit**
Sampling rate	Up to **4 Msps**
Input	Single-ended and differential
Offset and Gain compensation	Auto calibration to reduce gain and offset

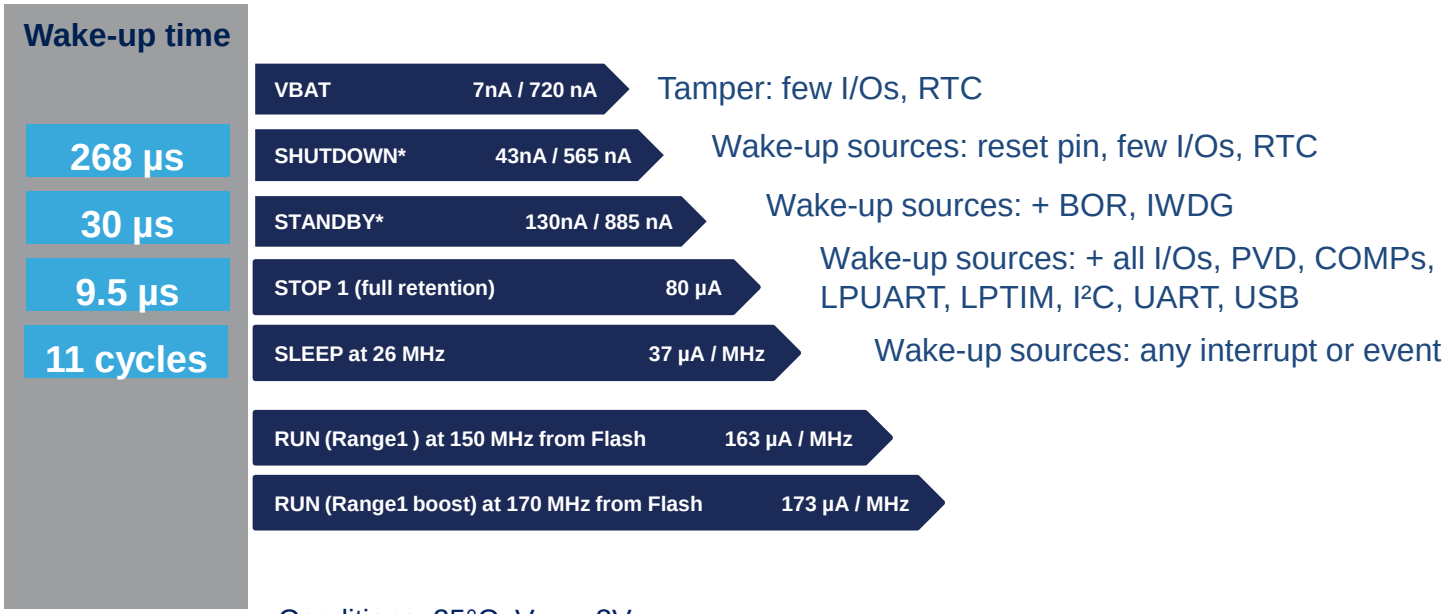
DAC (up to 7)	Values
Sampling rate	**15 Msps** (internal) 1Msps (from buffered output)
Settling time	16ns

Op-Amp (up to 6)	Values
GBW	**13 MHz**
Slew rate	**45 V/µs**
Offset	3mV over full T° range 1.5mV @ 25°C
PGA Gain (accuracy)	2, 4, 8, 16, -1,-3,-7,-15 **(1%)** 32, 64, -31,-63 (2%)

Comparator (up to 7)	Values
Power supply	1.62 .. 3.6V
Propagation delay	**16.7ns**
Offset	-6 .. +2 mV
Hysteresis	8 steps: 0, 9, 18, 27, 36, 45, 54, 63 mV

Dynamic Efficiency Modes

When Mainstream MCU Series meets low-power requirements



Conditions: 25°C, V_{DD} = 3V

Note : * without RTC / with RTC

Key Features for Targeted Applications

STM32 G4

Motor Control

Home appliances, E-bikes, Air Conditioning

- Fast CPU 170MHz
- Mathematical accelerator (Cordic)
- Advanced Motor Control timers
- Fast comparators
- 4Msps ADC-12bit + HW oversampling
- Op-Amp with built-in gain (PGA)
- DAC-12bit
- 1% RC accuracy
  (UART communication w/o external Xtal)

High-End Consumer

Rechargeable devices, drones, toys

- Low-thickness, small form-factor
- Low consumption in run mode ~ 160µA/MHz
- Embedded analog
- SAI (Sound Audio Interface)
- USB type-C Power Delivery 3.0

Industrial devices Measurements

Industrial equipment

- Fast CPU 170MHz
- Mathematical accelerator (Cordic)
- High temperature 125°C
- CAN FD support
- SPI, USART, I²C
- Advanced timers
- Real Time Clock with backup registers
- Dual bank flash for **live** upgrade
- AES & security

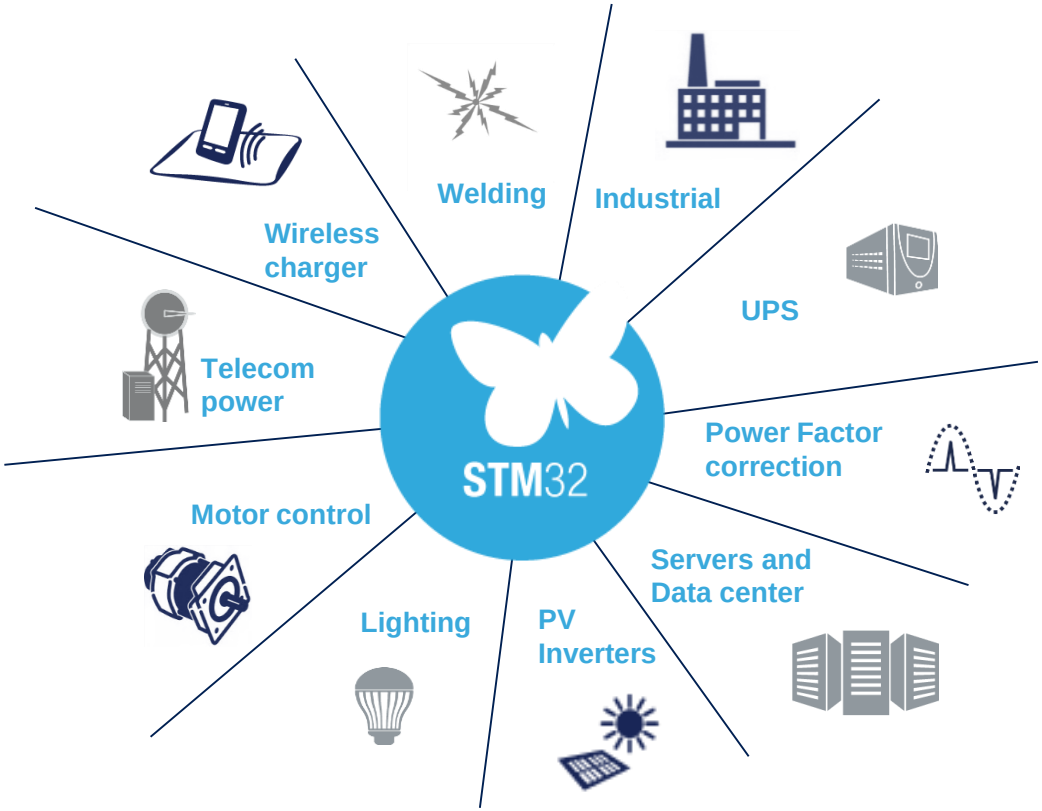
Digital Power

Servers, Telecom, EV Charging station

- Fast CPU 170 MHz
- Mathematical accelerator (Filtering)
- 12ch High Resolution timer (184ps)
- 4Msps ADC-12bit + HW oversampling
- Fast comparators (17ns)
- Embedded analog
- Dual bank flash for **live** upgrade
- AES & security
- FMAC for 3p3z compensation

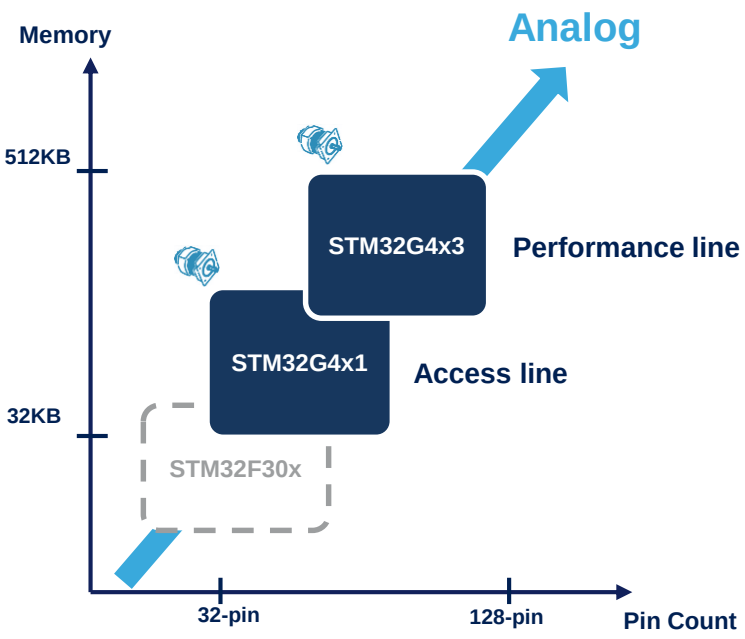
Ease Digital Power Conversion

Enhance your digital power solutions using the STM32G4's full features High Resolution Timer (HRTIM)

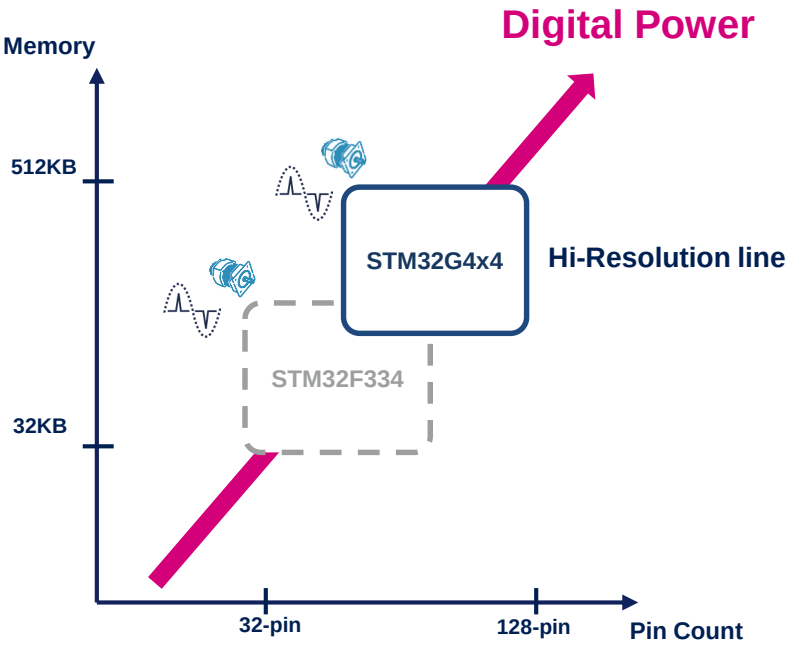


STM32 G4 products lines

General Purpose



Applications Specific



STM32 G4

Block diagrams & Portfolio

STM32 G4 product lines

Common peripherals and architecture:

- ARM Cortex-M4 + FPU 170MHz
- ETM, MPU
- Math Accelerator/
- Securable Memory Area
- Com. Peripheral: USART, SPI, I2C, SAI
- Multiple general-purpose timers
- Integrated reset and brown-out waming
- Multiple DMA
- 2x watchdogs Real-time clock
- Integrated regulator PLL and clock circuit
- Main oscillator and 32 kHz oscillator
- Low-speed and high-speed internal RC oscillator
- -40 to +85 °C and up to 105°C operating temperature range
- Low voltage 1.65 to 3.6 V
- Temperature sensor

STM32G4x4 – Hi-Resolution line

Up to 512KB Flash	Up to 96KB SRAM	Up to 32KB CCM	FSMC	Up to 5x 12b ADC 5MSPS	Up to 6x Op-Amp	Up to 7x Comp.	Up to 7x 12b DAC	3x 16-bit AMC timer	CAN-FD USB-PD	12 ch Hi-Res Timer

STM32G4x3 - Performance Line

Up to 512KB Flash	Up to 96KB SRAM	Up to 32KB CCM	FSMC	Up to 5x 12b ADC 5MSPS	Up to 6x Op-Amp	Up to 7x Comp.	Up to 7x 12b DAC	3x 16-bit AMC timer	CAN-FD USB-PD

STM32G4x1 - Access Line

Up to 512KB Flash	Up to 96KB SRAM	Up to 32KB CCM	2x 12b ADC 5MSPS	3x Op-Amp	4x Comp.	4x 12b DAC	2x 16-bit AMC timer	CAN-FD USB-PD

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STM32 G4 - 512KB die - STM32G47x

Block diagram

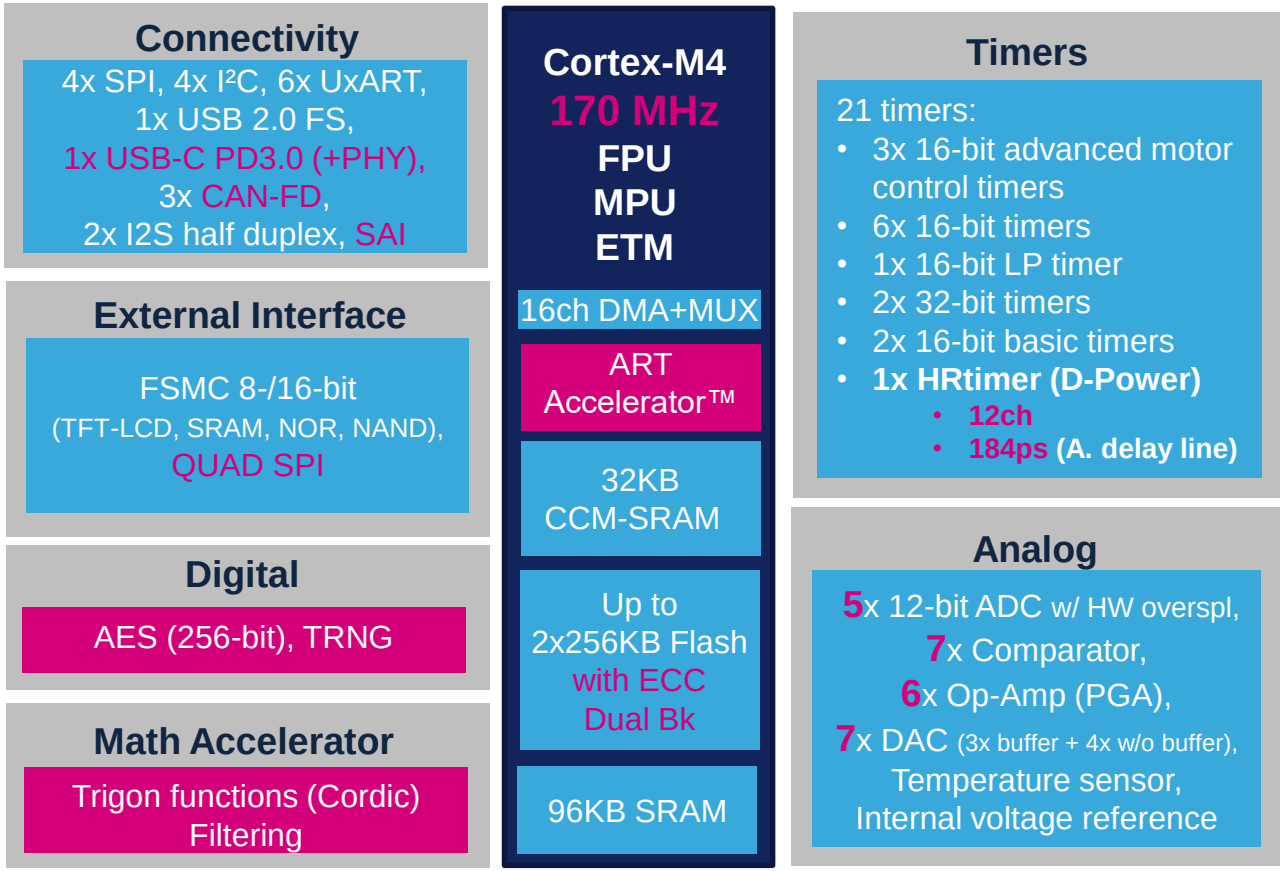
Key parameters

- 96KB SRAM + 32KB CCM-SRAM with parity bit (partial)
- **3x Accelerators: ART + CCM-SRAM + Mathematic**
- **213DMIPS**
- **Dual Bank (RWW)** Flash with **ECC**
- **Securable Memory Area** (ex: FW upgrade)

- 1.65V to 3.6V
- **RC 1%** [-5°C..90°C]
- 12-bit ADC 5MSPS + HW overspl.
- **HRtimer (12ch; 184ps min)**

- Max ambient T° 125°C (limited spec)
- **Run mode 170µA/MHz (Fmax 170Mhz)**
- Stop1 50µA @ 25°C, 3V

- Package: LQFP128/100/80/64/48; QFN48; TFBGA 100; WLCSP81
- 100 I/Os min
- Robust EMC/ESD/EMS



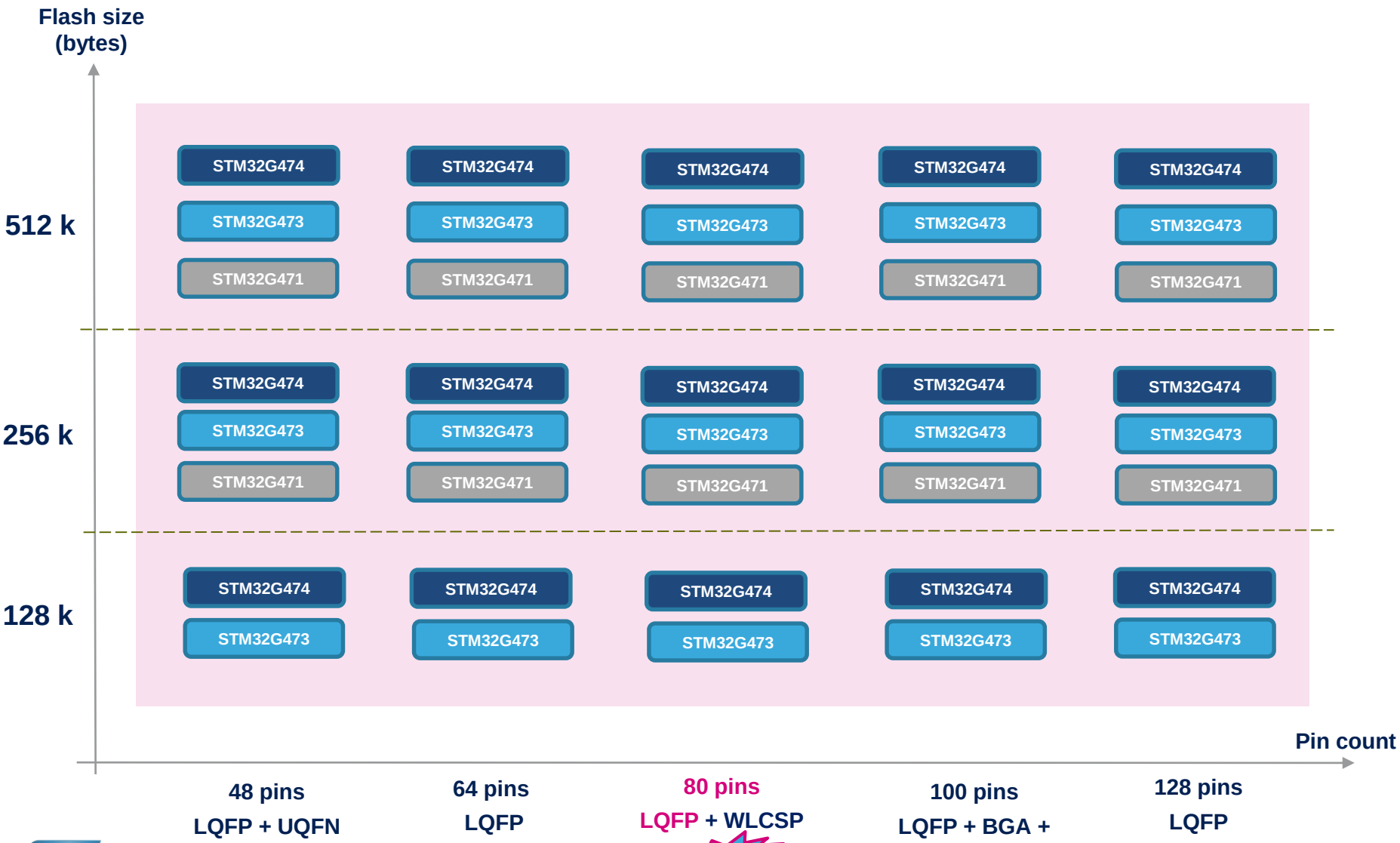
Fmax:

- ✓ ***170Mhz in performance mode*** *(~170µA/MHz w/ ART enabled)*
- ✓ ***150Mhz in normal mode*** *(~160µA/MHz w/ ART enabled)*

Legend:

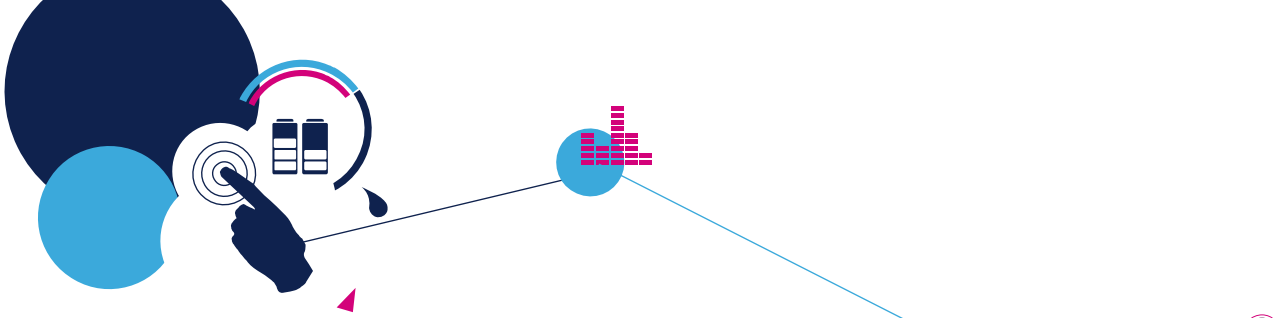
- *In pink: Main changes vs F3 series*

STM32G47x Product line - Portfolio



Legend:

Hi-Resolution line | Performance line | Access line | Dedicated PN w/ AES/TRNG



STM32 G4 product series

Jean-Marc MATHIEU
MCD Marketing Product Line Manager

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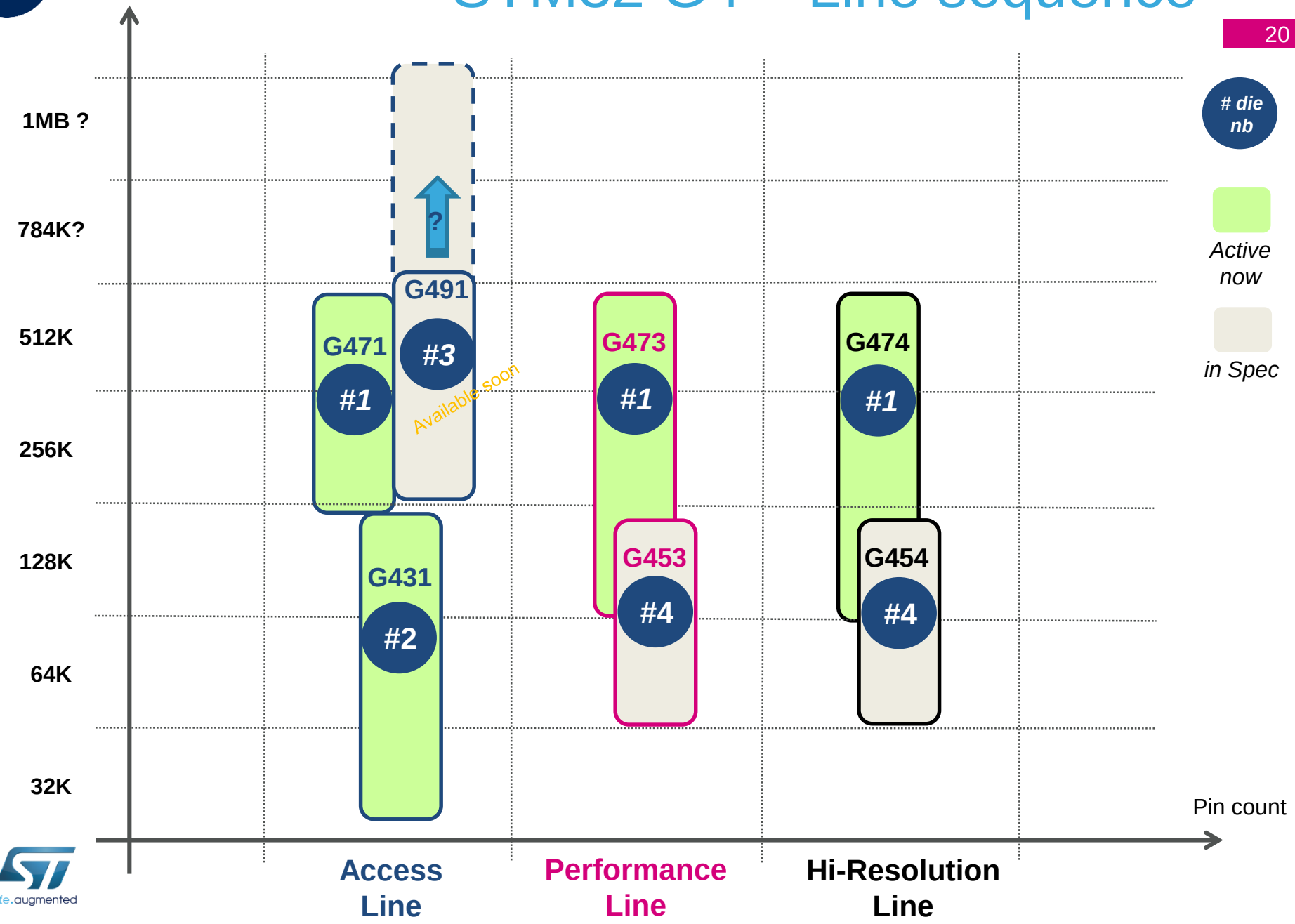
STM32 G4 – Line sequence



STM32 G4 - 128KB die - STM32G431

Access line - Block Diagram (w/o Hi-res Timer)

Key parameters

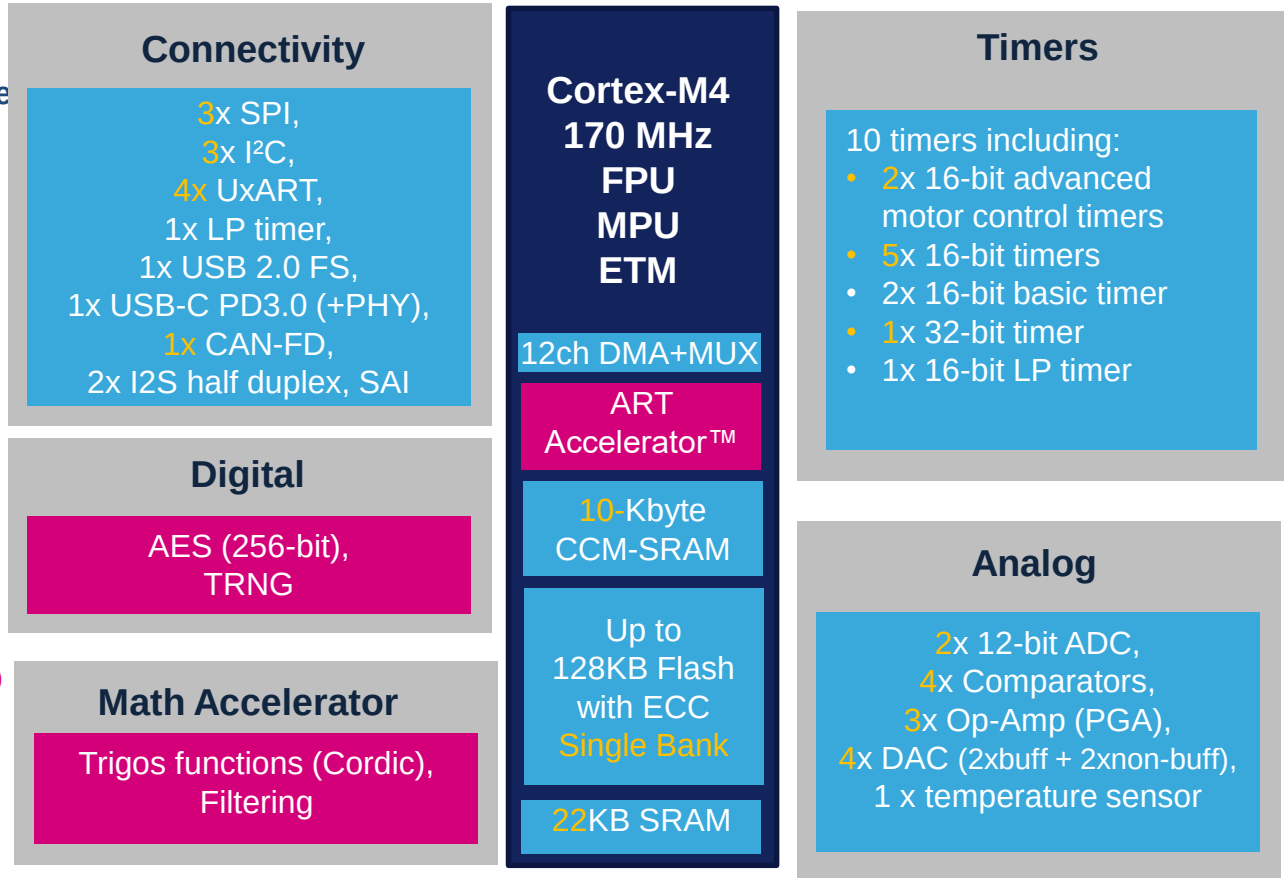
- 32KB SRAM = 22KB SRAM + 10KB CCM-SRAM with parity bit (partial)
- **3x Accelerators: ART + CCM routine booster + Mathematic**
- **213DMIPS**
- **Single Bank** Flash with **ECC**
- **Securable Memory Area**

- 1.65V to 3.6V
- **RC 1%** [-5°C..90°C]
- **16-bit ADC** resolution by HW overspl.

- Max ambient T° 125°C (limited spec)
- **Run mode ~160µA/MHz** **(Fmax 170MHz)**
- Stop1 50µA @ 25°C, 3V

- Package LQFP100/64/48/32; QFN32/48, BGA64; CSP64
- Robust EMC/ESD/EMS

- 81 I/Os min



Fmax:

- ✓ ***170Mhz in performance mode*** *(~170µA/MHz w/ ART enabled)*
- ✓ ***150Mhz in normal mode*** *(~160µA/MHz w/ ART enabled)*

Legend:

- *In orange: Main change vs 512K version*

Available soon

STM32 G4 – 512KB die - STM32G491

Access line - Block Diagram (w/o Hi-res Timer)

Key parameters

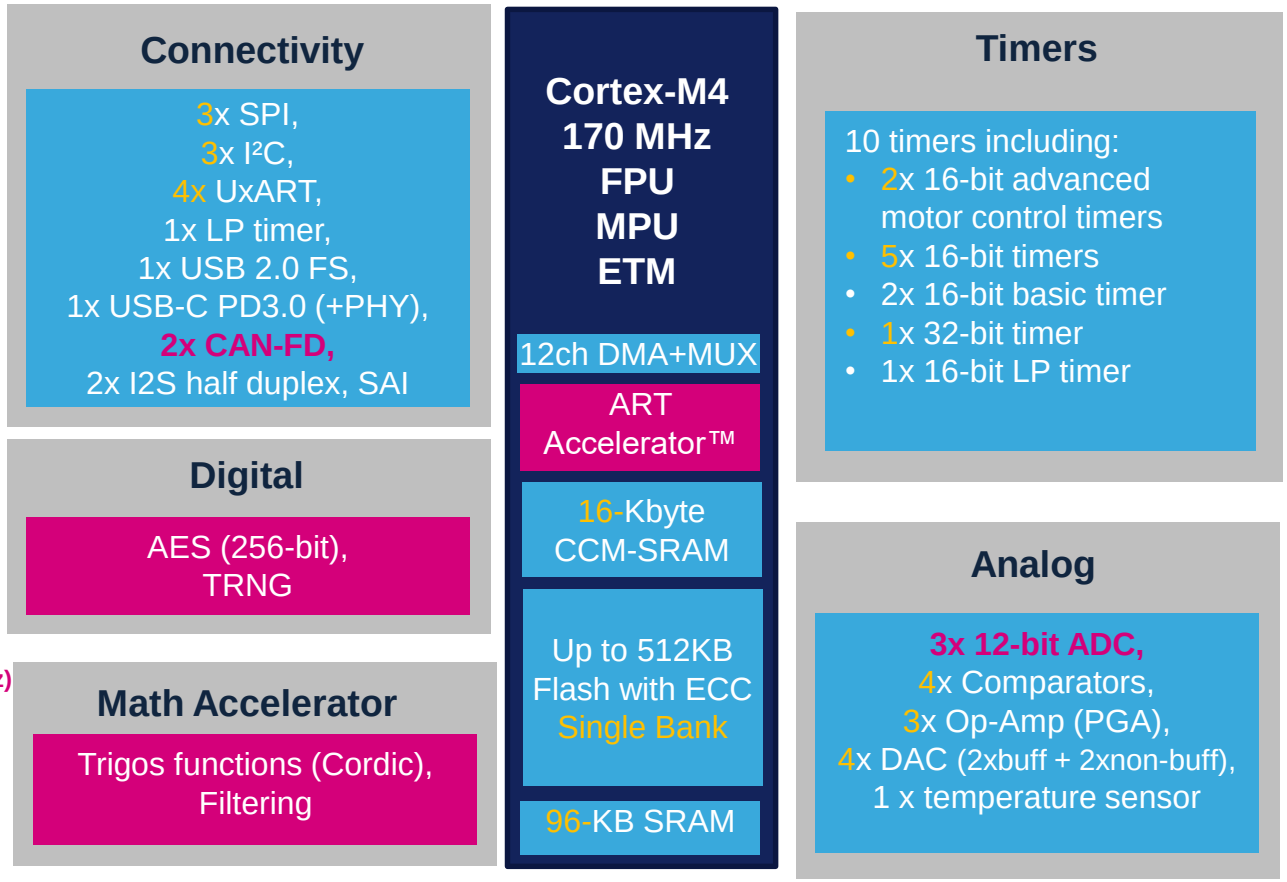
- 88KB SRAM = 64KB SRAM + 24KB CCM-SRAM with parity bit (partial)
- **3x Accelerators: ART + CCM routine booster + Mathematic**
- **213DMIPS**
- **Single Bank** Flash with **ECC**
- **Securable Memory Area**

- 1.65V to 3.6V
- **RC 1%** [-5°C..90°C]
- **16-bit ADC** resolution by HW overspl.

- Max ambient T° 125°C (limited spec)
- **Run mode ~160µA/MHz** **(Fmax 170MHz)**
- Stop1 50µA @ 25°C, 3V

- Package LQFP100/64/48/32; QFN32/48, BGA64; CSP64
- Robust EMC/ESD/EMS

- 81 I/Os min



Fmax:

- ✓ ***170Mhz in performance mode*** *(~170µA/MHz w/ ART enabled)*
- ✓ ***150Mhz in normal mode*** *(~160µA/MHz w/ ART enabled)*

Legend:

- *In orange: Main change vs superset version*

STM32 G4 - 128KB die - STM32G45x

Block diagram (w/ Hi-res Timer)

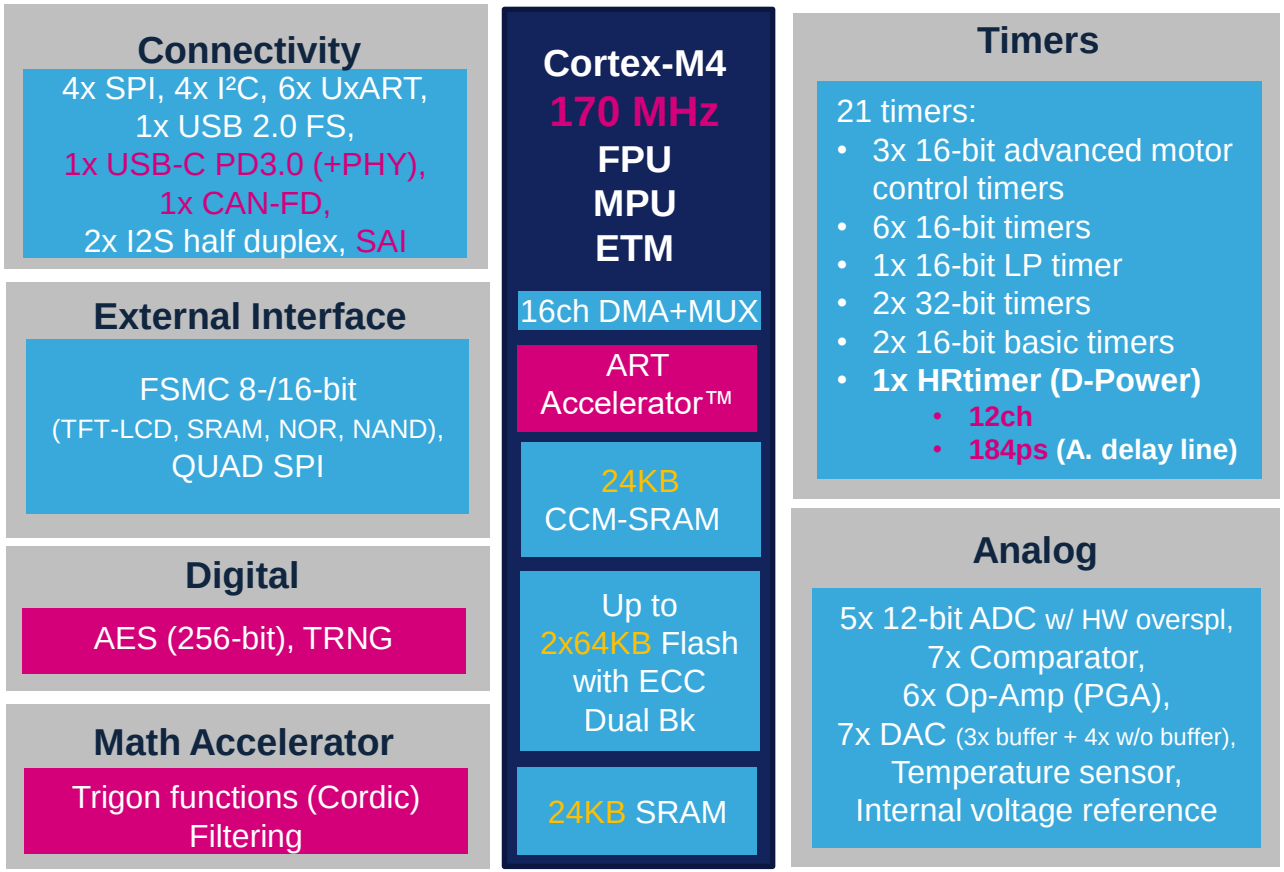
Key parameters

- 24KB SRAM + 24KB CCM-SRAM with parity bit (partial)
- **3x Accelerators: ART + CCM routine booster + Mathematic**
- **213DMIPS**
- **Dual Bank** Flash with **ECC**
- **Securable Memory Area** (ex: FW upgrade)

- 1.65V to 3.6V
- **RC 1%** [-5°C..90°C]
- 12-bit ADC 5MSPS + HW overspl.
- **HRtimer (12ch; 184ps min)**

- Max ambient T° 125°C (limited spec)
- **Run mode ~160µA/MHz** **(Fmax 170MHz)**
- Stop1 50µA @ 25°C, 3V

- Package: LQFP100/64/48/32; QFN48/32; BGA 64
- 100 I/Os min
- Robust EMC/ESD/EMS



Fmax:

- ✓ ***170Mhz in performance mode*** *(~170µA/MHz w/ ART enabled)*
- ✓ ***150Mhz in normal mode*** *(~160µA/MHz w/ ART enabled)*

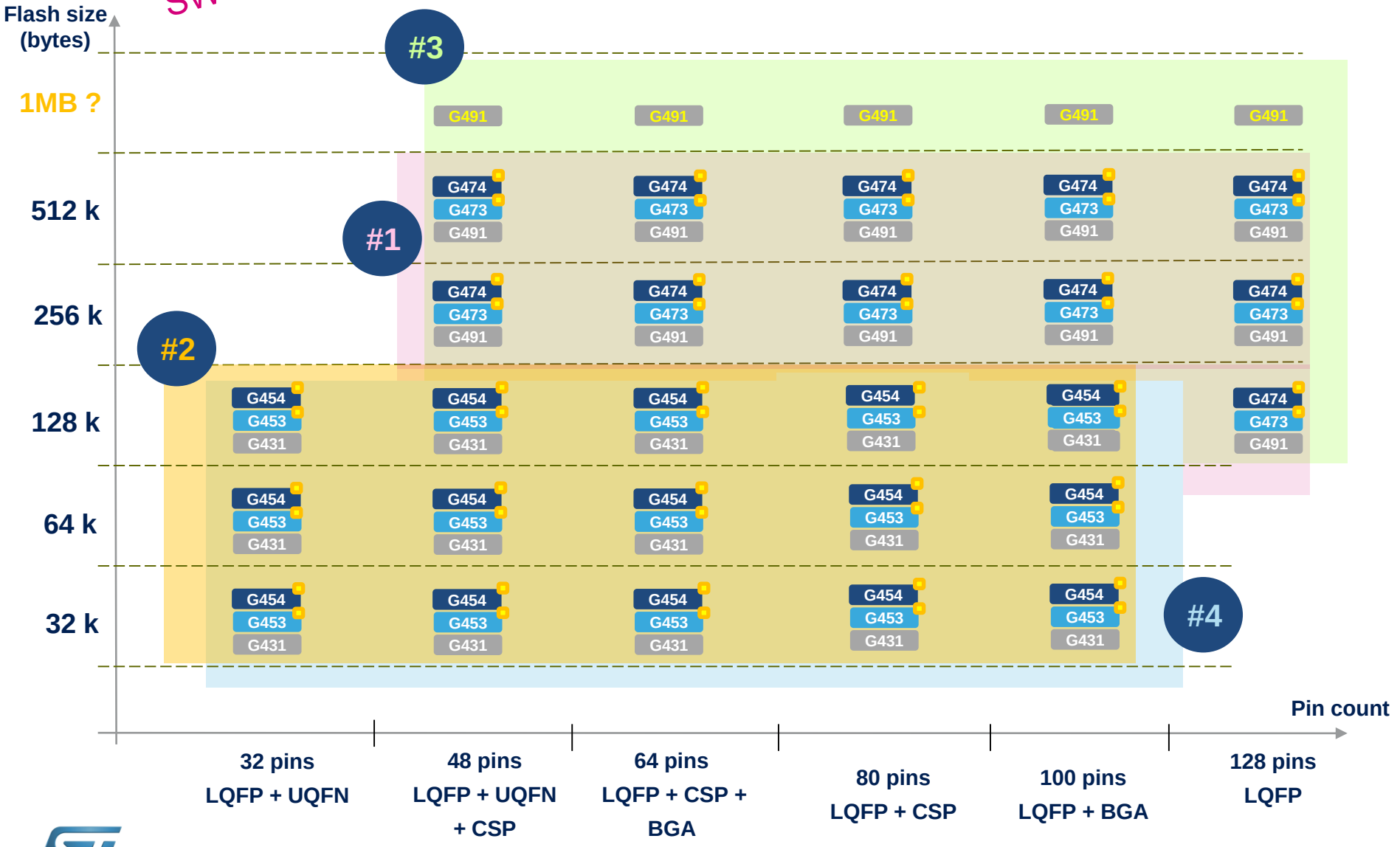
Legend:

- *In orange: Main change vs superset version*

STM32 G4 series - Portfolio

based on 4 dice

100% pinout and SW compatible !



Legend:

- Hi-Resolution line
- Performance line
- Access line
- Dedicated PN w/ AES/TRNG

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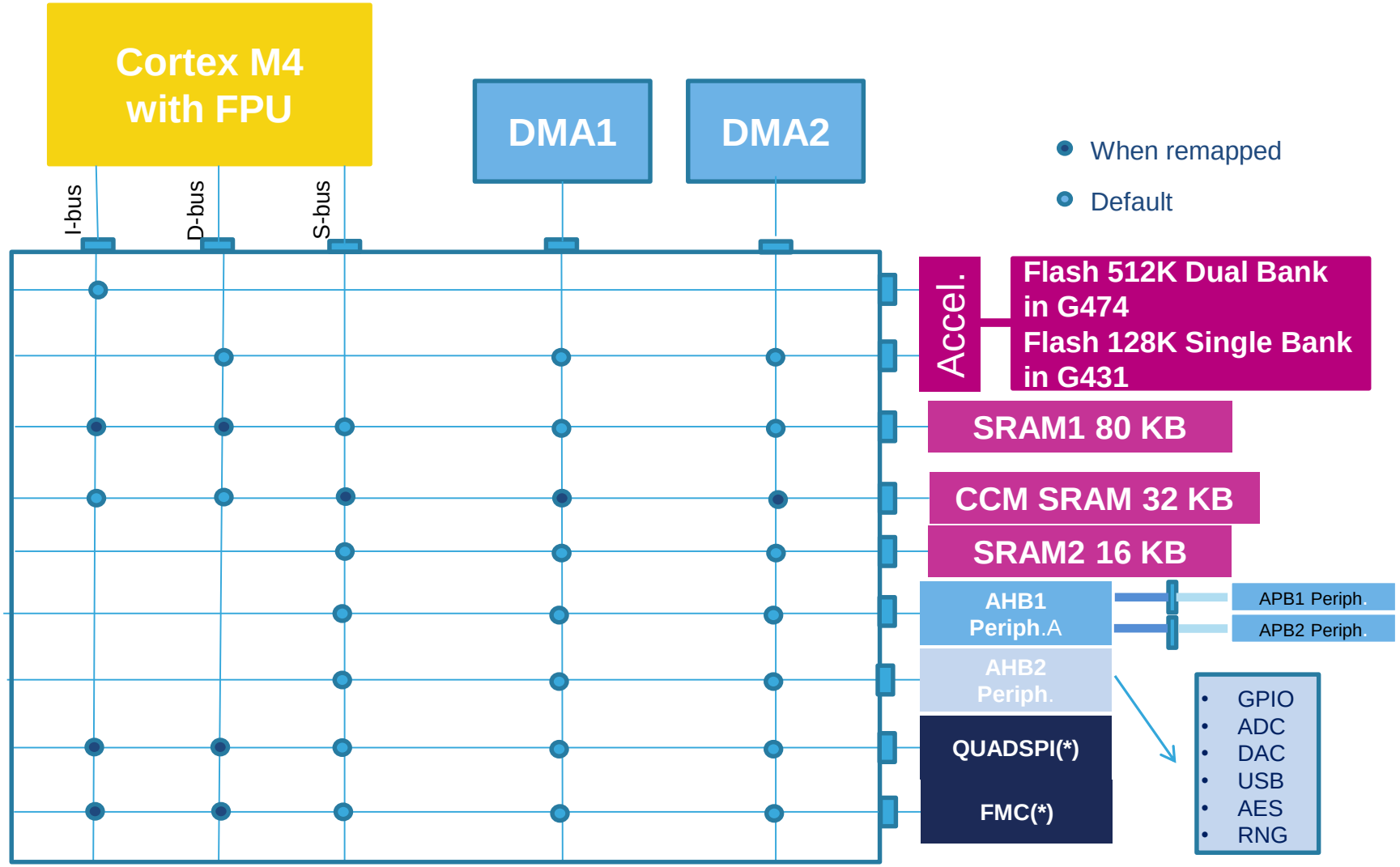
Bus matrix

G4 series



*: Only on STM32G474

STM32G4 vs STM32F3 Peripherals Summary

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STM32G4 Versus STM32F3

	STM32F3 Family	STM32G4 Family	Comments
Maximum Frequency	72MHz	170MHz	
Flash	Up to 512K	Up to 512KB	
	Single Bank	Dual Bank (RWW) or Single Bank	Modified Flash interface + more protection features in the G4.
External Memory FSMC	8-,16-bit NOR, PSRAM, SRAM and NAND memories	8-,16-bit NOR, PSRAM, SRAM and NAND memories	
External Memory QuadSPI	NA	1x QuadSPI	New in G4. Same as L4.
DMA	DMA1: 7ch, DMA2:5ch	DMA1: Up to 8ch, DMA2:Up to 8ch	Same as F3.
DMAMUX	NA	YES	Same as STM32L4+
CORDIC	NA	YES	New in G4.
Filter Math Accelerator FMAC	NA	YES	New in G4
RTC	YES	YES	G4 RTC implementation is the same as F3, with separated RTC/TAMP peripherals in G4.

Connectivity

	STM32F3 Family	STM32G4 Family	Comments
USART	Up to 3xUSART Up to 2xUART	Up to 3xUSART Up to 2xUART	More features in the G4 USART: - Clock source prescaler - SPI Slave mode, - Tx/Rx FIFOs
LPUART	NA	1	LPUART has less features than USART.
I2C	Up to 4xI2C	Up to 4 x I2C	Same as F3 I2C
SPI/I2S	Up to 4xSPI 2xI2S full duplex	Up to 4xSPI 2xI2S half duplex	Same as F3. Only few minor fixes are made in G4 SPI.
SAI	NA	YES	Same as L4
FDCAN	NA	Up to 3 x FDCAN	1 Kbyte SRAM per FDCAN. FDCAN like H7 but lighter version.
bXCAN	YES	NA	
USB device	YES	YES	
UCPD	NA	YES 1 UCPD	G4 UCPD same as G0.

Analog

	STM32F3 Family	STM32G4 Family	Comments
ADC	Up to 4	Up to 5	More features in G4.
DAC	Up to 3 external DAC channels	Up to 7 DAC channels: - 3 external channels 1MSPS - 4 internal channels 15MSPS	More features in G4.
OPAMP	Up to 4	Up to 6	More features in G4.
COMP	Up to 7	Up to 7	
VREFBUF	NA	Yes, with 3 voltages support: 2.5V, 2.048V and 2.90V	New in G4

Timers

Timer type	STM32F3 Family	STM32G4 Family	Comments
Advanced control	Up to 3 (TIM1/8/20)	Up to 3 (TIM1/8/20)	Same as F3, with more features.
General purpose 32bits	Up to 2 (TIM2/TIM5)	Up to 2 (TIM2/TIM5)	Same as F3 with more features.
General purpose 16bits (TIM3/4/15/16/17)	Up to 5 (TIM3/4/15/16/17)		Same as F3 with more features.
Basic	Up to 2 (TIM6/7)		Same as F3.
LPTimer	NA	1	New in G4.
High resolution timer	1 (in the F334 only)	1	Same as F334, with more features.
Systick timer	1	1	Same as F3.
Watchdog timers(independent/window)	2	2	Same as F3.

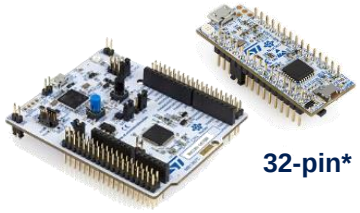
Security

	STM32F3 Family	STM32G4 Family
MPU	YES (in some F3 devices)	YES
Crypto	NA	Tiny AES 256-bit
TRNG	NA	YES
Protection features in the flash	Write protection Readout protection (Level 0/1/2)	Write protection Readout protection (Level 0/1/2) PCROP protection Securable memory area

STM32 Ecosystem

STM32G4 Hardware Solutions

Accelerate evaluation, prototyping and design



STM32 Nucleo	Evaluation boards	Motor Control Pack	Discovery kits
Flexible prototyping	**Full feature STM32G4 evaluation**	**Full feature for Motor Control and Analog**	**Key feature prototyping**
• NUCLEO-G431RB • NUCLEO-G474RE • NUCLEO-G431KB*	• STM32G484E-EVAL • STM32G474E-EVAL • STM32G474E-EVAL1	• P-NUCLEO-IHM03	• B-G474E-DPOW1* • B-G431B-ESC1*

Available now from distributor stocks

* Available in distributor stocks from Q3-2019

Examples of Nucleo expansion boards

BLE

WiFi 802.11 b/g/n

Dynamic NFC tag

Motion & Environmental sensors

Proximity & Light sensor

Audio Microphones

Motor driver

LED driver

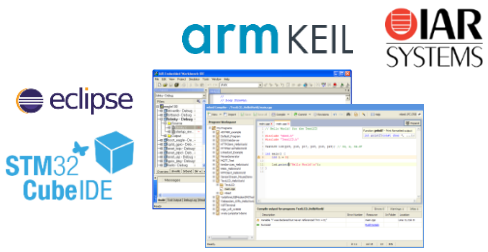
Sub-1GHz

Security

Software Development Tools

C/C++ Focus

Complete support of Arm Cortex-M ecosystem

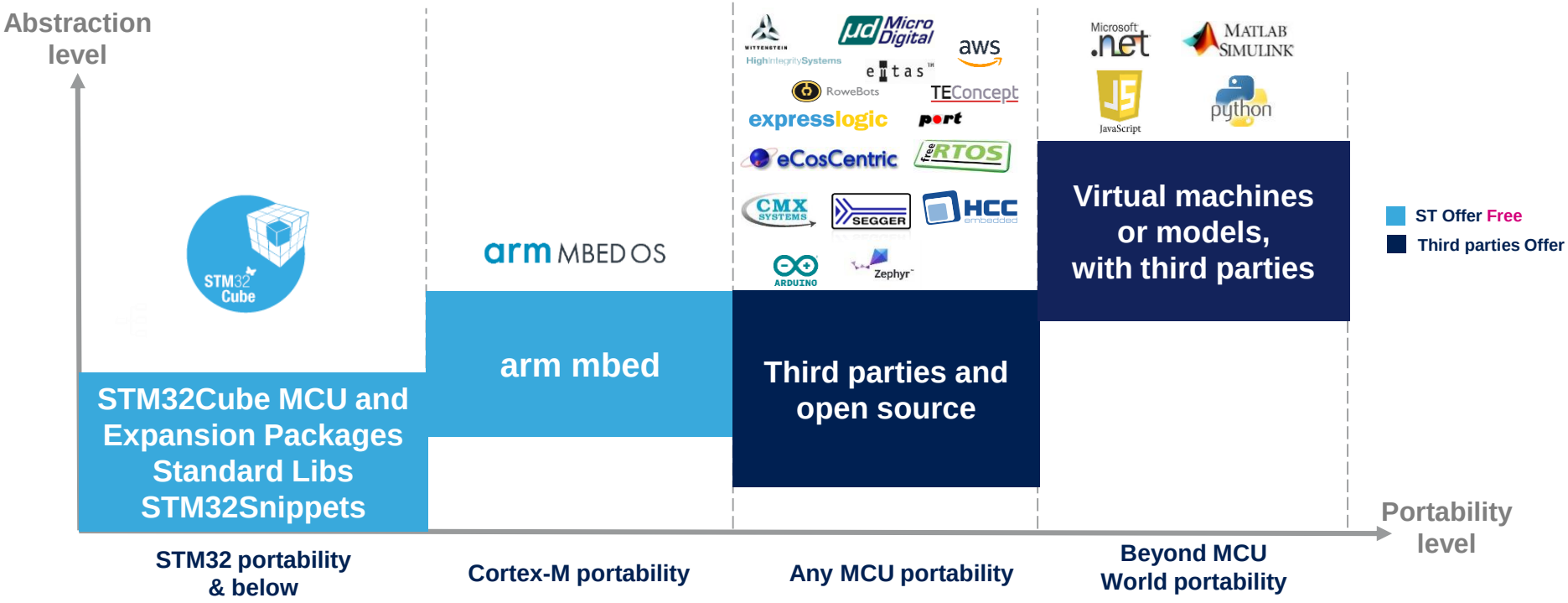


STM32CubeMX	IDEs Compile and Debug	STM32 Programming Tool
STM32CubeMX • Configure and generate Code • Conflicts solver	**Flexible Solutions** • Partners IDE, like IAR and Keil • Free IDE based on Eclipse like STM32CubeIDE*	**STM32CubeProgrammer** • Flash and/or system memory • GUI or command line interface

* SW examples will be available in Q4 19

Embedded Software

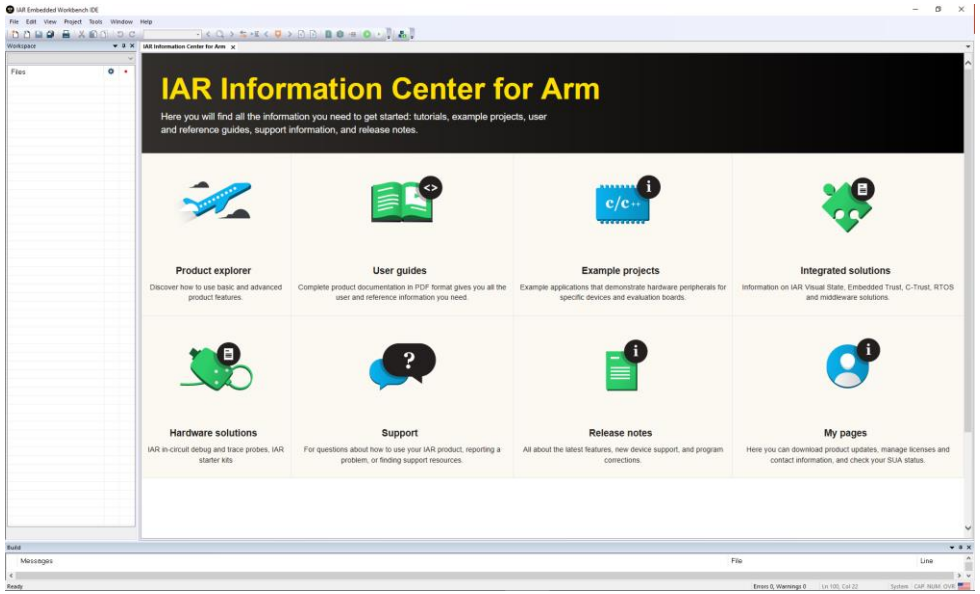
Several solutions mixing levels of Portability and Abstraction



IAR IDE for STM32

- Comprehensive software development environment for Cortex-M devices :
  - Comprehensive support for STM32 firmware (Std Peripheral library or Cube HAL).
  - Free trail version : 30-day time limited fully functional licence or size-limited version without time limit.

- Key features :
  - IAR C/C++ compiler.
  - IAR IDE, debugger and simulation environment.
  - CMSIS-compliant.
  - ST-Link support.
  - The setup of peripherals configured by CubeMX is directly exported to IAR.



Free MDK-ARM for ST

ARM KEIL Microcontroller Tools

- Free licenses for STM32 devices based on Cortex-M0/M0+ cores :
  - Applicable immediately to all STM32F0 and STM32L0 mcus.
  - PC-locked multi-year licenses.
  - No code size limit.
  - Multiple language support.
  - Technical support included.
- Direct download from Keil website :
  - No limit of number of downloads by customer.
  - Direct access to configuration files for STM32 and associated boards.
  - Free access to MDK-ARM periodic updates.

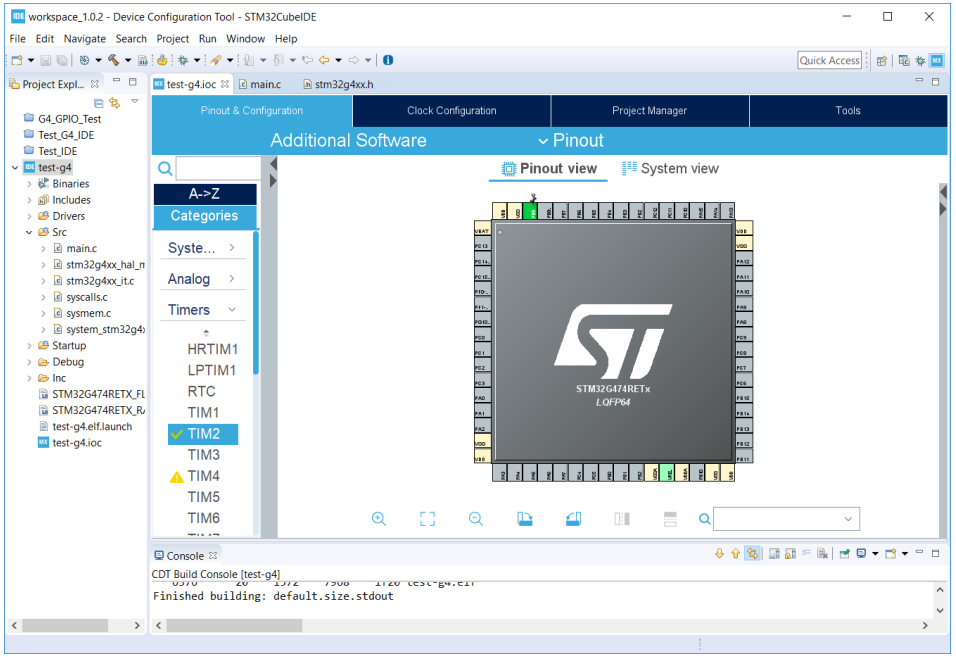
- How to get free MDK-ARM licenses for STM32F0 and STM32L0 ?

  - Go to Keil website at : www.keil.com/mdk-st
  - Download MDK-ARM toolchain.
  - Activate the free license using this Product Serial Number (PSN) : **4PPFW-QBEHZ-M0D5M**

STM32CubeIDE for STM32

- Free STM32CubeIDE for STM32. v1.0.2 is available now !
  - No code size limit.
  - With full Pro feature set
- Direct download from ST website

- Key features :
  - C/C++ compiler.
  - IDE, debugger and simulation environment.
  - ST-Link support.
  - The setup of peripherals configured by CubeMX is directly exported to CubeIDE.

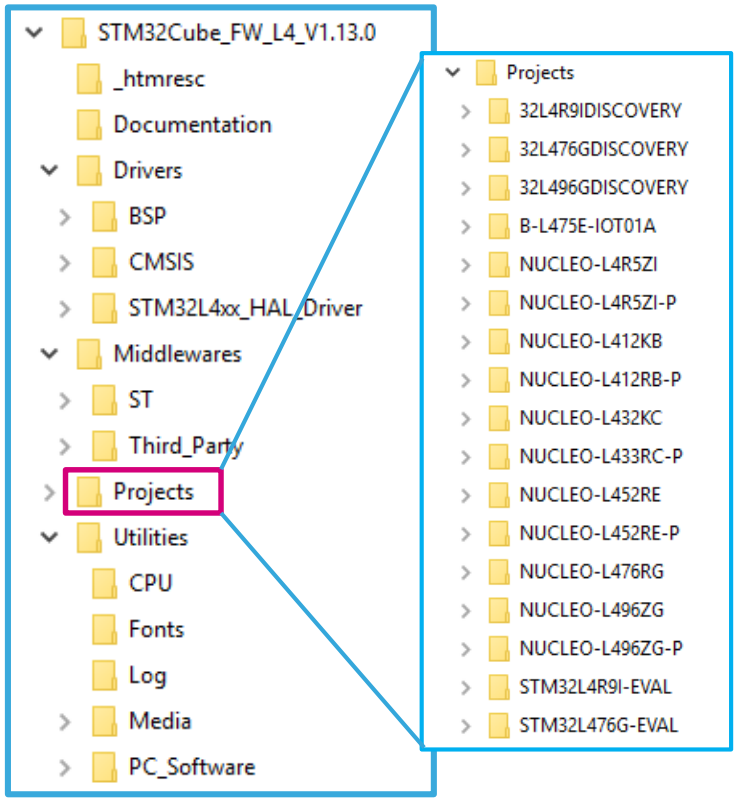


Major Steps

- Power Consumption Calculator
- MCU Selector
- Code generation
- Pinout Configuration
- Middleware Parameters
- Clock Tree Initialization
- Peripherals
  - CAN
  - I²C
  - SPI
  - UART

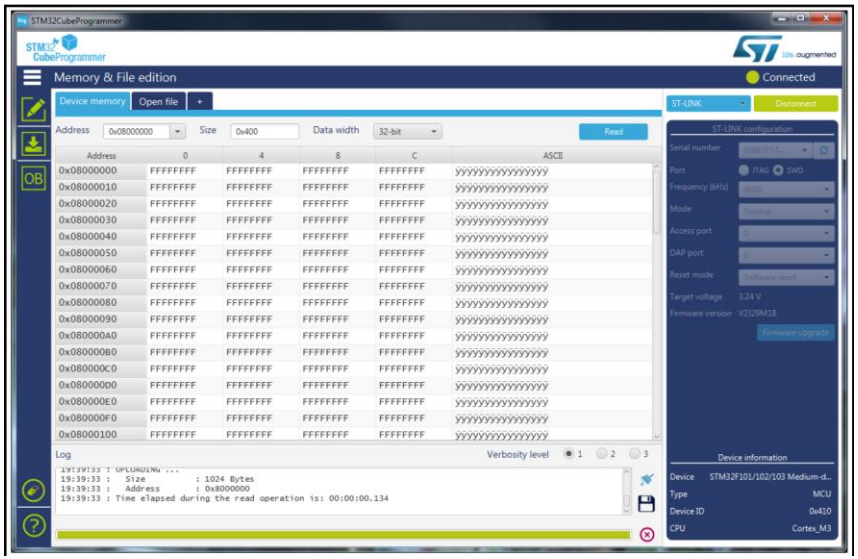
Software Libraries

- ST software libraries free at www.st.com/mcu
- C source code for easy implementation of all STM32 peripherals in any application
  - STM32Cube HAL library – source code for implementation of all standard peripherals. Code implemented in demos for STM32 evaluation boards
  - Standard library –(Previous product)
- Cryptographic library – A set of cryptographic algorithms used in all STM32 microcontrollers(free with license agreement).
- ARM CMSIS DSP library – (free with license agreement)
- Graphic library – STemWin/TouchGFX (free with license agreement).



New STM32CubeProg

STM32 CubeProgrammer



http://www.st.com/content/st_com/en/products/development-tools/software-development-tools/stm32-software-development-tools/stm32-programmers/stm32cubeprog.html

- Erases, programs, views and verifies the content of the device Flash memory
- Supports debug and bootloader interfaces:
  - ST-LINK debug probe (JTAG/SWD)
  - UART and USB DFU bootloader interfaces
  - OTA for STM32WB via BLE(new on Ver2.0)
- Multi-OS support: Windows® , Linux® , macOS®

STM32 & TouchGFX

STMicroelectronics Adds High-Quality User-Interface Design Software to Free Development Ecosystem for STM32 Microcontrollers

Press release available here
ST Media Lib collection here

www.st.com/stm32gui

life.augmented

ST-LINK/V2 Debugger

ST-Link/V2 provides low-cost debugging and programming capabilities

In-circuit Programming / Debugging

Direct firmware update feature supported (DFU)

Order code: **ST-LINK/V2**

- ST-Link/V2 extends programming and debugging capabilities to STM8 with addition of SWIM adapter.
- STM8 applications use the USB full speed interface to communicate with STMicroelectronic's ST Visual Develop (STVD) or ST Visual Program (STVP) software.
- STM32 applications use the USB full speed interface to communicate with Atollic, IAR, Keil or CooCox integrated development environments.

Note: ST-Link/V2 supports connections for a complete range of ST MCUs including JTAG for ARM core-based families STM32.

ST-LINK/V2-ISOL Debugger

ST-Link/V2-ISOL provides low-cost debugging and programming capabilities

In-circuit Programming / Debugging

Direct firmware update feature supported (DFU)

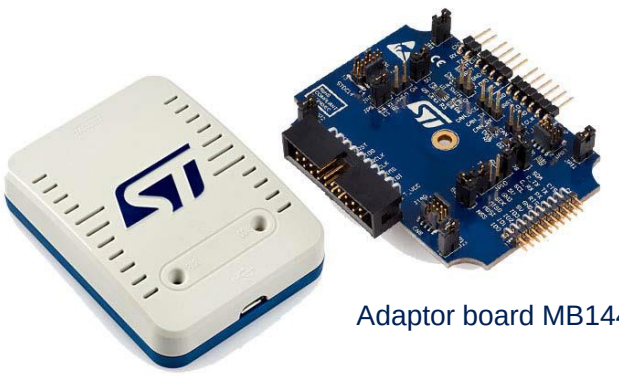
Order code: **ST-LINK/V2-ISOL**

- ST-Link/V2-ISOL extends programming and debugging capabilities to STM8 with addition of SWIM adapter.
- STM32 applications use the USB full speed interface to communicate with Atollic, IAR, Keil or TASKING integrated development environments.
- STM32 applications use the USB full speed interface to communicate with Atollic, IAR, Keil or CooCox integrated development environments

Note: ST-Link supports connections for a complete range of ST MCUs including JTAG for ARM core-based families STM32.

NEW ST-LINK/V3 Debugger

ST-Link/V3 modular in-circuit debugging and programming capabilities



Adaptor board MB1440

Main module MB1441

In-circuit Programming / Debugging

Direct firmware update feature supported (DFU)

Multi-path bridge

Order code: **ST-LINK/V3 SET**

- ST-Link/V3SET is a modular stand-alone debugging and programming probe for the STM8(SWIM) and STM32(JTAG/SWD) microcontrollers.
- Multi-path bridge USB to SPI/UART/I2C/CAN/GPIOs interfaces allowing for instance the programming of the target through bootloader.
- Extended features through additional modules such as the adapter board(MB1440).

Note: ST-Link supports connections for a complete range of ST MCUs including JTAG for ARM core-based families STM32.

STM32 – documentation structure

The documentation of STM32 devices is divided into group of separate documents:

- **DATASHEET** - electrical parameters, pinouts, pin functions, packaging
- **REFERENCE MANUAL** - functional description of each peripheral and its registers
- **ERRATA SHEET** – list of detected issues within the core and peripherals with suggested workaround
- **CORTEX Mx PROGRAMMING MANUAL** - core programming manual and NVIC description
- **APPLICATION NOTES** – list of short documents describing particular peripheral use cases, configurations.
- Standard peripherals library manual - **.CHM** file at library folder

All those documents can be found on dedicated web page at www.st.com/stm32

STM32 documentation

datasheet

- Datasheet contains main information for hardware developer:
  - List of features
  - Pinout information
  - Electrical characteristic
  - Package information

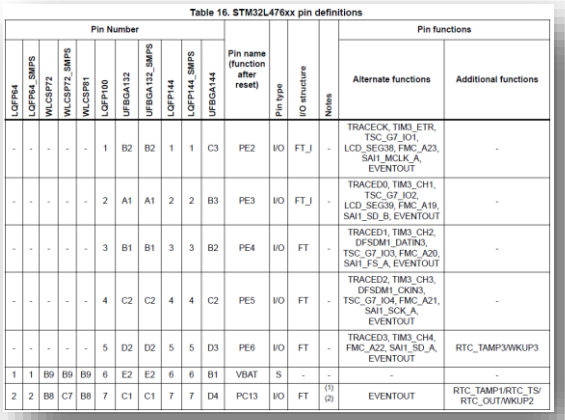
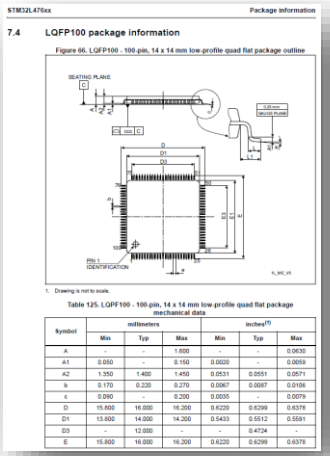


Table 16. STM32L476xx pin definitions

Pin Number											Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP72	WLCSP72_SMPS	WLCSP81	LQFP100	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA144					Alternate functions	Additional functions
-	-	-	-	-	1	B2	B2	1	1	C3	PE2	I/O	FT_l	-	TRACECK, TIM3_ETR, TSC_G7_IO1, LCD_SEG38, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	2	A1	A1	2	2	B3	PE3	I/O	FT_l	-	TRACED0, TIM3_CH1, TSC_G7_IO2, LCD_SEG39, FMC_A19, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	3	B1	B1	3	3	B2	PE4	I/O	FT	-	TRACED1, TIM3_CH2, DFSDM1_DATIN3, TSC_G7_IO3, FMC_A20, SAI1_FS_A, EVENTOUT	-
-	-	-	-	-	4	C2	C2	4	4	C2	PE5	I/O	FT	-	TRACED2, TIM3_CH3, DFSDM1_CKIN3, TSC_G7_IO4, FMC_A21, SAI1_SCK_A, EVENTOUT	-
-	-	-	-	-	5	D2	D2	5	5	D3	PE6	I/O	FT	-	TRACED3, TIM3_CH4, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_TAMP3/WKUP3
1	1	B9	B9	B9	6	E2	E2	6	6	B1	VBAT	S	-	-	-	-
2	2	B8	C7	B8	7	C1	C1	7	7	D4	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1/RTC_TS/ RTC_OUT/WKUP2



STM32L476xx Package information

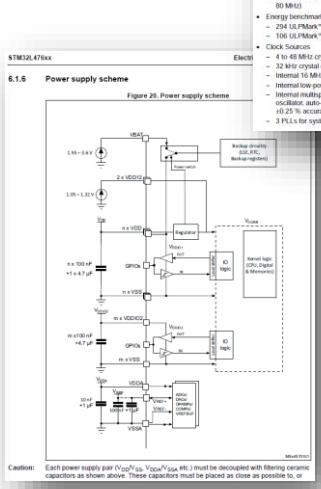
7.4 LQFP100 package information

Figure 66. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline

1. Drawing is not to scale.

Table 125. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3		12.000			0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

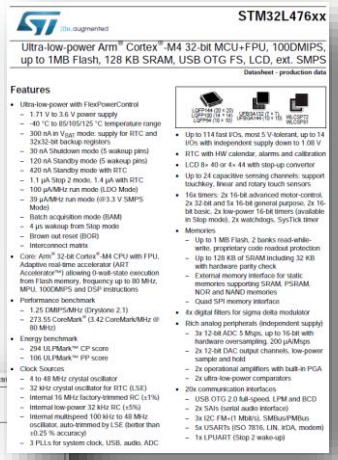


STM32L476xx

6.1.6 Power supply scheme

Figure 26. Power supply scheme

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or



STM32L476xx

Ultra-low-power Arm® Cortex®-M4 32-bit MCU+FPU, 100DMIPS, up to 1MB Flash, 128 KB SRAM, USB OTG FS, LCD, ext. SMPS

Datasheet - production data

Features

- Ultra-low-power with FlexPowerControl
  - 1.71 V to 3.6 V power supply
  - -40 °C to 85/105/125 °C temperature range
  - 300 nA in V_{BAT} mode: supply for RTC and 32x32-bit backup registers
  - 30 nA Shutdown mode (5 wakeup pins)
  - 120 nA Standby mode (5 wakeup pins)
  - 420 nA Standby mode with RTC
  - 1.1 µA Stop 2 mode, 1.4 µA with RTC
  - 100 µA/MHz run mode (LDO Mode)
  - 39 µA/MHz run mode (@3.3 V SMPS Mode)
  - Batch acquisition mode (BAM)
  - 4 µs wakeup from Stop mode
  - Brown out reset (BOR)
  - Interconnect matrix
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 80 MHz, MPU, 100DMIPS and DSP instructions
- Performance benchmark
  - 1.25 DMIPS/MHz (Dhrystone 2.1)
  - 273.55 CoreMark® (3.42 CoreMark/MHz @ 80 MHz)
- Energy benchmark
  - 294 ULPMark™ CP score
  - 106 ULPMark™ PP score
- Clock Sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal 16 MHz factory-trimmed RC (±1%)
  - Internal low-power 32 kHz RC (±5%)
  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
  - 3 PLLs for system clock, USB, audio, ADC
- Up to 114 fast I/Os, most 5 V-tolerant, up to 14 I/Os with independent supply down to 1.08 V
- RTC with HW calendar, alarms and calibration
- LCD 8× 40 or 4× 44 with step-up converter
- Up to 24 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- 16x timers: 2x 16-bit advanced motor-control, 2x 32-bit and 5x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Memories
  - Up to 1 MB Flash, 2 banks read-while-write, proprietary code readout protection
  - Up to 128 KB of SRAM including 32 KB with hardware parity check
  - External memory interface for static memories supporting SRAM, PSRAM, NOR and NAND memories
  - Quad SPI memory interface
- 4x digital filters for sigma delta modulator
- Rich analog peripherals (independent supply)
  - 3x 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 2x 12-bit DAC output channels, low-power sample and hold
  - 2x operational amplifiers with built-in PGA
  - 2x ultra-low-power comparators
- 20x communication interfaces
  - USB OTG 2.0 full-speed, LPM and BCD
  - 2x SAIs (serial audio interface)
  - 3x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 5x USARTs (ISO 7816, LIN, IrDA, modem)
  - 1x LPUART (Stop 2 wake-up)

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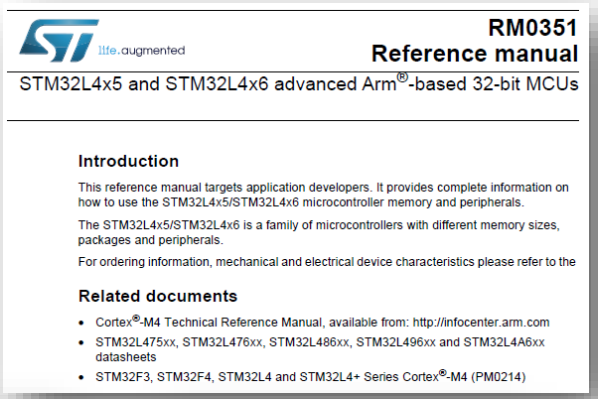
STM32 documentation

reference manual

- Reference manual contains main information for software developer:
  - Memory mapping
  - Block diagram of each peripheral
  - Peripherals description
  - Peripherals sets of register with bits description



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RM0351
Reference manual

STM32L4x5 and STM32L4x6 advanced Arm®-based 32-bit MCUs

Introduction

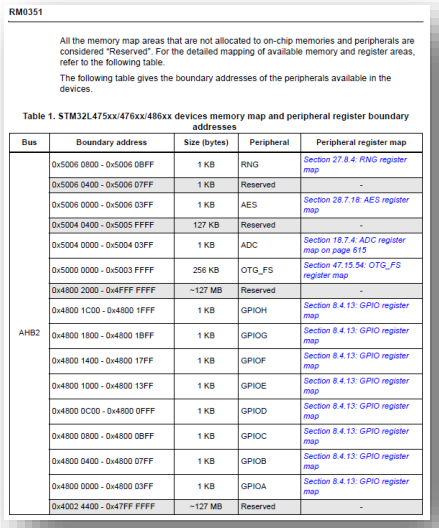
This reference manual targets application developers. It provides complete information on how to use the STM32L4x5/STM32L4x6 microcontroller memory and peripherals.

The STM32L4x5/STM32L4x6 is a family of microcontrollers with different memory sizes, packages and peripherals.

For ordering information, mechanical and electrical device characteristics please refer to the

Related documents

- Cortex®-M4 Technical Reference Manual, available from: http://infocenter.arm.com
- STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx and STM32L4A6xx datasheets
- STM32F3, STM32F4, STM32L4 and STM32L4+ Series Cortex®-M4 (PM0214)



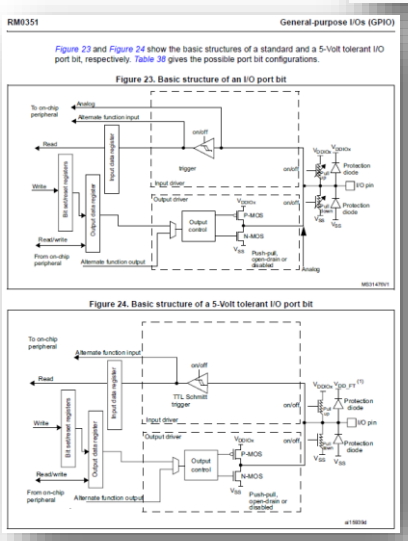
RM0351

All the memory map areas that are not allocated to on-chip memories and peripherals are considered "Reserved". For the detailed mapping of available memory and register areas, refer to the following table.

The following table gives the boundary addresses of the peripherals available in the devices.

Table 1. STM32L475xx/476xx/486xx devices memory map and peripheral register boundary addresses

Bus	Boundary address	Size (bytes)	Peripheral	Peripheral register map
AHB2	0x5006 0800 - 0x5006 0BFF	1 KB	RNG	Section 27.8.4: RNG register map
	0x5006 0400 - 0x5006 07FF	1 KB	Reserved	-
	0x5006 0000 - 0x5006 03FF	1 KB	AES	Section 28.7.18: AES register map
	0x5004 0400 - 0x5005 FFFF	127 KB	Reserved	-
	0x5004 0000 - 0x5004 03FF	1 KB	ADC	Section 18.7.4: ADC register map on page 615
	0x5000 0000 - 0x5003 FFFF	256 KB	OTG_FS	Section 47.15.54: OTG_FS register map
	0x4800 2000 - 0x4FFF FFFF	~127 MB	Reserved	-
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH	Section 8.4.13: GPIO register map
	0x4800 1800 - 0x4800 1BFF	1 KB	GPIOG	Section 8.4.13: GPIO register map
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF	Section 8.4.13: GPIO register map
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE	Section 8.4.13: GPIO register map
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD	Section 8.4.13: GPIO register map
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC	Section 8.4.13: GPIO register map
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB	Section 8.4.13: GPIO register map
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA	Section 8.4.13: GPIO register map
	0x4002 4400 - 0x47FF FFFF	~127 MB	Reserved	-

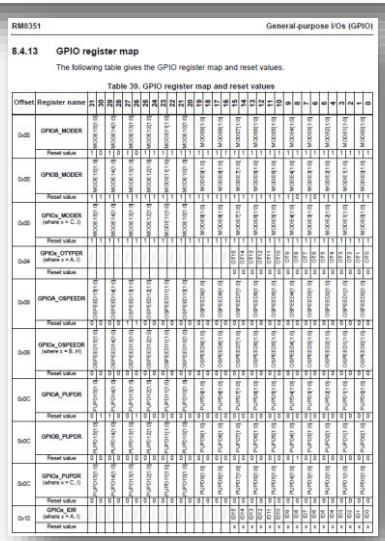


RM0351 General-purpose I/Os (GPIO)

Figure 23 and Figure 24 show the basic structures of a standard and a 5-Volt tolerant I/O port bit, respectively. Table 38 gives the possible port bit configurations.

Figure 23. Basic structure of an I/O port bit

Figure 24. Basic structure of a 5-Volt tolerant I/O port bit



RM0351 General-purpose I/Os (GPIO)

8.4.13 GPIO register map

The following table gives the GPIO register map and reset values.

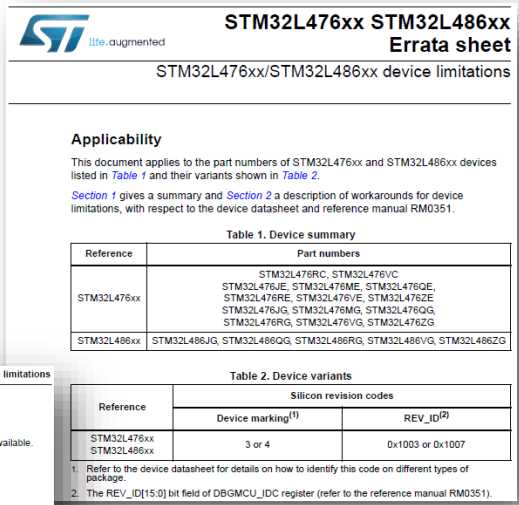
Table 39. GPIO register map and reset values

Offset	Register name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	GPIOA_MODER	MODE15[1:0]	MODE14[1:0]	MODE13[1:0]	MODE12[1:0]	MODE11[1:0]	MODE10[1:0]	MODE9[1:0]	MODE8[1:0]	MODE7[1:0]	MODE6[1:0]	MODE5[1:0]	MODE4[1:0]	MODE3[1:0]	MODE2[1:0]	MODE1[1:0]	MODE0[1:0]																	
	Reset value	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0																
0x00	GPIOB_MODER	MODE15[1:0]	MODE14[1:0]	MODE13[1:0]	MODE12[1:0]	MODE11[1:0]	MODE10[1:0]	MODE9[1:0]	MODE8[1:0]	MODE7[1:0]	MODE6[1:0]	MODE5[1:0]	MODE4[1:0]	MODE3[1:0]	MODE2[1:0]	MODE1[1:0]	MODE0[1:0]																	
	Reset value	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0																
0x00	GPIOx_MODER (where x = C..I)	MODE15[1:0]	MODE14[1:0]	MODE13[1:0]	MODE12[1:0]	MODE11[1:0]	MODE10[1:0]	MODE9[1:0]	MODE8[1:0]	MODE7[1:0]	MODE6[1:0]	MODE5[1:0]	MODE4[1:0]	MODE3[1:0]	MODE2[1:0]	MODE1[1:0]	MODE0[1:0]																	
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																
0x04	GPIOx_OTYPER (where x = A..I)																	OT15	OT14	OT13	OT12	OT11	OT10	OT9	OT8	OT7	OT6	OT5	OT4	OT3	OT2	OT1	OT0
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	GPIOA_OSPEEDR	OSPEED15[1:0]	OSPEED14[1:0]	OSPEED13[1:0]	OSPEED12[1:0]	OSPEED11[1:0]	OSPEED10[1:0]	OSPEED9[1:0]	OSPEED8[1:0]	OSPEED7[1:0]	OSPEED6[1:0]	OSPEED5[1:0]	OSPEED4[1:0]	OSPEED3[1:0]	OSPEED2[1:0]	OSPEED1[1:0]	OSPEED0[1:0]																	
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																
0x08	GPIOx_OSPEEDR (where x = B..H)	OSPEED15[1:0]	OSPEED14[1:0]	OSPEED13[1:0]	OSPEED12[1:0]	OSPEED11[1:0]	OSPEED10[1:0]	OSPEED9[1:0]	OSPEED8[1:0]	OSPEED7[1:0]	OSPEED6[1:0]	OSPEED5[1:0]	OSPEED4[1:0]	OSPEED3[1:0]	OSPEED2[1:0]	OSPEED1[1:0]	OSPEED0[1:0]																	
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																
0x0C	GPIOA_PUPDR	PUPD15[1:0]	PUPD14[1:0]	PUPD13[1:0]	PUPD12[1:0]	PUPD11[1:0]	PUPD10[1:0]	PUPD9[1:0]	PUPD8[1:0]	PUPD7[1:0]	PUPD6[1:0]	PUPD5[1:0]	PUPD4[1:0]	PUPD3[1:0]	PUPD2[1:0]	PUPD1[1:0]	PUPD0[1:0]																	
	Reset value	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0																
0x0C	GPIOB_PUPDR	PUPD15[1:0]	PUPD14[1:0]	PUPD13[1:0]	PUPD12[1:0]	PUPD11[1:0]	PUPD10[1:0]	PUPD9[1:0]	PUPD8[1:0]	PUPD7[1:0]	PUPD6[1:0]	PUPD5[1:0]	PUPD4[1:0]	PUPD3[1:0]	PUPD2[1:0]	PUPD1[1:0]	PUPD0[1:0]																	
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																
0x0C	GPIOx_PUPDR (where x = C..I)	PUPD15[1:0]	PUPD14[1:0]	PUPD13[1:0]	PUPD12[1:0]	PUPD11[1:0]	PUPD10[1:0]	PUPD9[1:0]	PUPD8[1:0]	PUPD7[1:0]	PUPD6[1:0]	PUPD5[1:0]	PUPD4[1:0]	PUPD3[1:0]	PUPD2[1:0]	PUPD1[1:0]	PUPD0[1:0]																	
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																
0x10	GPIOx_IDR (where x = A..I)																	IDR15	IDR14	IDR13	IDR12	IDR11	IDR10	IDR9	IDR8	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
	Reset value																	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

STM32 documentation

errata sheet

- Errata sheet contains main information for software and hardware developers:
  - Detected issues within current silicon revision for the core with suggested workaround
  - Detected issues within current silicon revision for peripherals with suggested workaround



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STM32L476xx STM32L486xx
Errata sheet

STM32L476xx/STM32L486xx device limitations

Applicability

This document applies to the part numbers of STM32L476xx and STM32L486xx devices listed in *Table 1* and their variants shown in *Table 2*.

Section 1 gives a summary and *Section 2* a description of workarounds for device limitations, with respect to the device datasheet and reference manual RM0351.

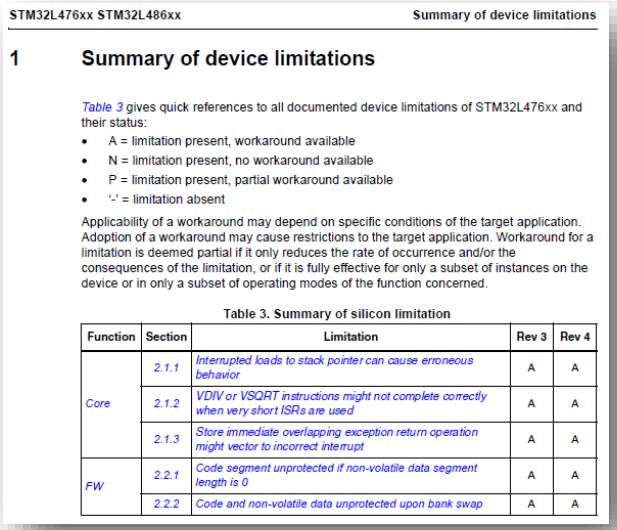
Table 1. Device summary

Reference	Part numbers
STM32L476xx	STM32L476RC, STM32L476VC STM32L476JE, STM32L476ME, STM32L476QE, STM32L476RE, STM32L476VE, STM32L476ZE STM32L476JG, STM32L476MG, STM32L476QG, STM32L476RG, STM32L476VG, STM32L476ZG
STM32L486xx	STM32L486JG, STM32L486QG, STM32L486RG, STM32L486VG, STM32L486ZG

Table 2. Device variants

Reference	Silicon revision codes	
	Device marking(1)	REV_ID(2)
STM32L476xx STM32L486xx	3 or 4	0x1003 or 0x1007

1. Refer to the device datasheet for details on how to identify this code on different types of package.
2. The REV_ID[15:0] bit field of DBGMCU_IDC register (refer to the reference manual RM0351).



STM32L476xx STM32L486xx — Summary of device limitations

1 Summary of device limitations

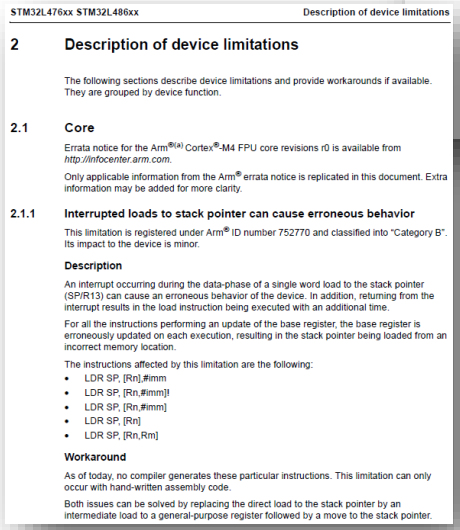
Table 3 gives quick references to all documented device limitations of STM32L476xx and their status:

- A = limitation present, workaround available
- N = limitation present, no workaround available
- P = limitation present, partial workaround available
- '-' = limitation absent

Applicability of a workaround may depend on specific conditions of the target application. Adoption of a workaround may cause restrictions to the target application. Workaround for a limitation is deemed partial if it only reduces the rate of occurrence and/or the consequences of the limitation, or if it is fully effective for only a subset of instances on the device or in only a subset of operating modes of the function concerned.

Table 3. Summary of silicon limitation

Function	Section	Limitation	Rev 3	Rev 4
Core	2.1.1	*Interrupted loads to stack pointer can cause erroneous behavior*	A	A
	2.1.2	*VDIV or VSQRT instructions might not complete correctly when very short ISRs are used*	A	A
	2.1.3	*Store immediate overlapping exception return operation might vector to incorrect interrupt*	A	A
FW	2.2.1	*Code segment unprotected if non-volatile data segment length is 0*	A	A
	2.2.2	*Code and non-volatile data unprotected upon bank swap*	A	A



STM32L476xx STM32L486xx — Description of device limitations

2 Description of device limitations

The following sections describe device limitations and provide workarounds if available. They are grouped by device function.

2.1 Core

Errata notice for the Arm®(a) Cortex®-M4 FPU core revisions r0 is available from *http://infocenter.arm.com*.

Only applicable information from the Arm® errata notice is replicated in this document. Extra information may be added for more clarity.

2.1.1 Interrupted loads to stack pointer can cause erroneous behavior

This limitation is registered under Arm® ID number 752770 and classified into "Category B". Its impact to the device is minor.

Description

An interrupt occurring during the data-phase of a single word load to the stack pointer (SP/R13) can cause an erroneous behavior of the device. In addition, returning from the interrupt results in the load instruction being executed with an additional time.

For all the instructions performing an update of the base register, the base register is erroneously updated on each execution, resulting in the stack pointer being loaded from an incorrect memory location.

The instructions affected by this limitation are the following:

- LDR SP, [Rn],#imm
- LDR SP, [Rn,#imm]!
- LDR SP, [Rn,#imm]
- LDR SP, [Rn]
- LDR SP, [Rn,Rm]

Workaround

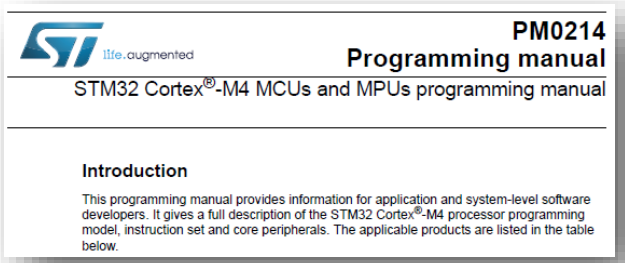
As of today, no compiler generates these particular instructions. This limitation can only occur with hand-written assembly code.

Both issues can be solved by replacing the direct load to the stack pointer by an intermediate load to a general-purpose register followed by a move to the stack pointer.

STM32 documentation

core programming manual

- Errata sheet contains main information for low level software developers concerning the core:
  - Core structure and its registers
  - Interrupt handling scheme
  - Assembler instructions set
  - Handling low level operations within the core



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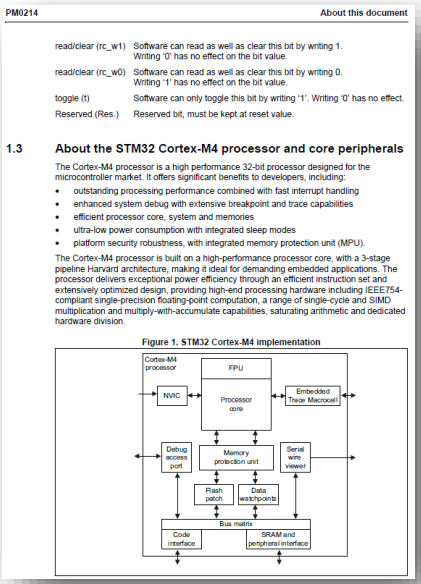
PM0214
Programming manual

STM32 Cortex®-M4 MCUs and MPUs programming manual

Introduction

This programming manual provides information for application and system-level software developers. It gives a full description of the STM32 Cortex®-M4 processor programming model, instruction set and core peripherals. The applicable products are listed in the table below.



read/clear (rc_w1)	Software can read as well as clear this bit by writing 1. Writing '0' has no effect on the bit value.
read/clear (rc_w0)	Software can read as well as clear this bit by writing 0. Writing '1' has no effect on the bit value.
toggle (t)	Software can only toggle this bit by writing '1'. Writing '0' has no effect.
Reserved (Res.)	Reserved bit, must be kept at reset value.

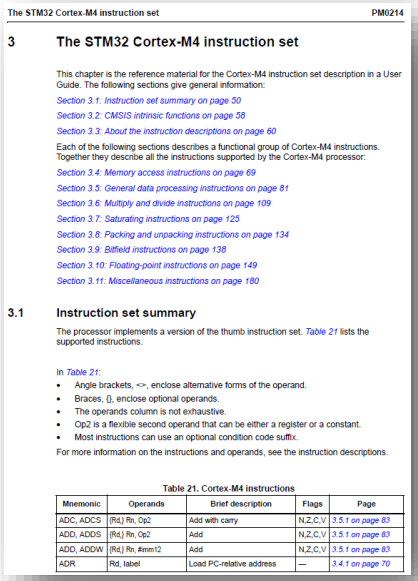
1.3 About the STM32 Cortex-M4 processor and core peripherals

The Cortex-M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- outstanding processing performance combined with fast interrupt handling
- enhanced system debug with extensive breakpoint and trace capabilities
- efficient processor core, system and memories
- ultra-low power consumption with integrated sleep modes
- platform security robustness, with integrated memory protection unit (MPU).

The Cortex-M4 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division.

Figure 1. STM32 Cortex-M4 implementation



3 The STM32 Cortex-M4 instruction set

This chapter is the reference material for the Cortex-M4 instruction set description in a User Guide. The following sections give general information:

Each of the following sections describes a functional group of Cortex-M4 instructions. Together they describe all the instructions supported by the Cortex-M4 processor:

3.1 Instruction set summary

The processor implements a version of the thumb instruction set. *Table 21* lists the supported instructions.

In *Table 21*:

- Angle brackets, <>, enclose alternative forms of the operand.
- Braces, {}, enclose optional operands.
- The operands column is not exhaustive.
- Op2 is a flexible second operand that can be either a register or a constant.
- Most instructions can use an optional condition code suffix.

For more information on the instructions and operands, see the instruction descriptions.

Table 21. Cortex-M4 instructions

Mnemonic	Operands	Brief description	Flags	Page
ADC, ADCS	{Rd,} Rn, Op2	Add with carry	N,Z,C,V	*3.5.1 on page 83*
ADD, ADDS	{Rd,} Rn, Op2	Add	N,Z,C,V	*3.5.1 on page 83*
ADD, ADDW	{Rd,} Rn, #imm12	Add	N,Z,C,V	*3.5.1 on page 83*
ADR	Rd, label	Load PC-relative address	—	*3.4.1 on page 70*

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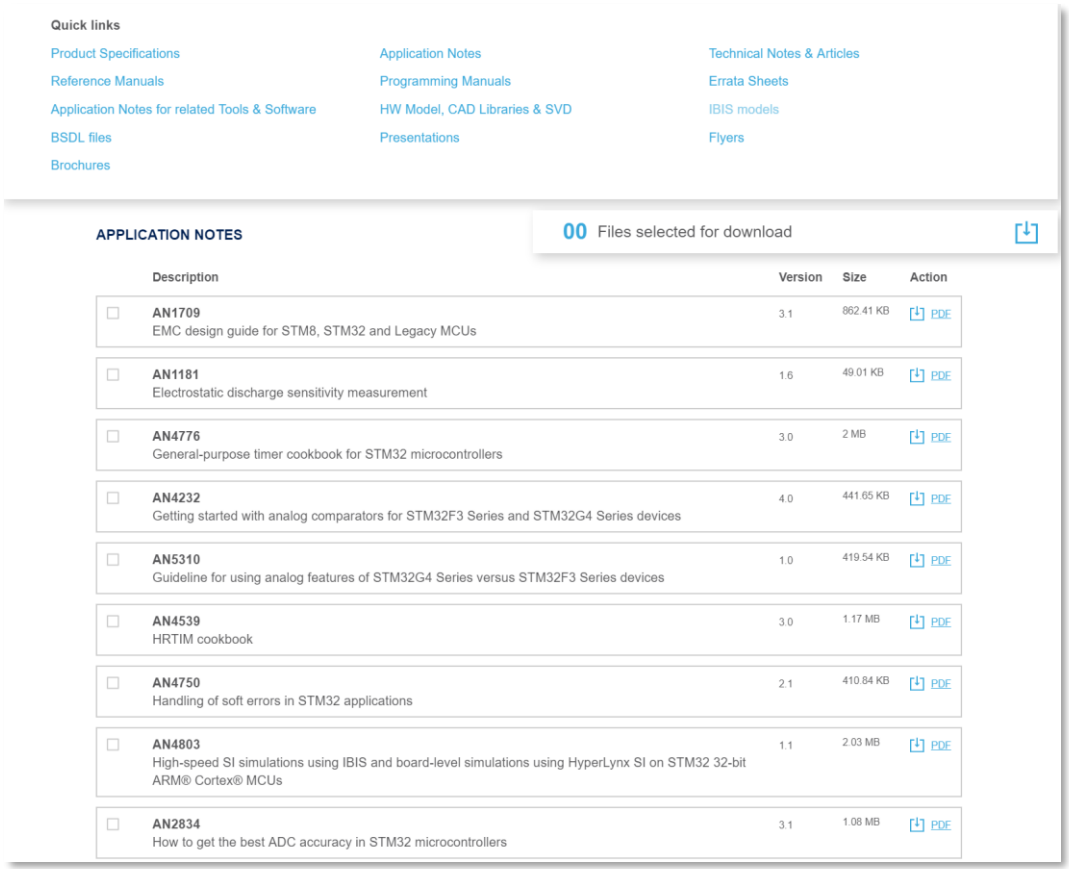
STM32 documentation

application notes

- Complete sets of application notes can be found on the web page dedicated for selected device.
- Below there is a part of the list of available documents for STM32G4 devices:



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Application Notes for related Tools & Software | HW Model, CAD Libraries & SVD | IBIS models
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APPLICATION NOTES

00 Files selected for download

Description	Version	Size	Action
AN1709 EMC design guide for STM8, STM32 and Legacy MCUs	3.1	862.41 KB	PDF
AN1181 Electrostatic discharge sensitivity measurement	1.6	49.01 KB	PDF
AN4776 General-purpose timer cookbook for STM32 microcontrollers	3.0	2 MB	PDF
AN4232 Getting started with analog comparators for STM32F3 Series and STM32G4 Series devices	4.0	441.65 KB	PDF
AN5310 Guideline for using analog features of STM32G4 Series versus STM32F3 Series devices	1.0	419.54 KB	PDF
AN4539 HRTIM cookbook	3.0	1.17 MB	PDF
AN4750 Handling of soft errors in STM32 applications	2.1	410.84 KB	PDF
AN4803 High-speed SI simulations using IBIS and board-level simulations using HyperLynx SI on STM32 32-bit ARM® Cortex® MCUs	1.1	2.03 MB	PDF
AN2834 How to get the best ADC accuracy in STM32 microcontrollers	3.1	1.08 MB	PDF

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