STM32G4 Technique Training

- HRTIMER v2

life.augmented

HRTIMER v2

- Additional features and improvements vs HRTIMER v1

Agenda

- Addition of a 6th timing unit
- Built-in slope compensation
- Valley skipping counter (event counter-based blanking)
- Enhanced protections
  - Blanking on fault signals
  - Stop on over-current before PWM start (short-circuit protection)
  - Fault after multiple pulses
- Push-pull mode improvements
- Classical PWM mode
- Up/Down counting mode
- ADC triggers extended to 10 channels, with post-scaler
- Others
    - No-overhead duty cycle zeroing
    - Easier interleaved schemes handling
    - Balanced Idle resuming automatically
    - Re-synchronized update mode
    - Swap mode
    - Triggerred half mode
    - Events propagation across timer

“HRTIMERv2”: Additional features

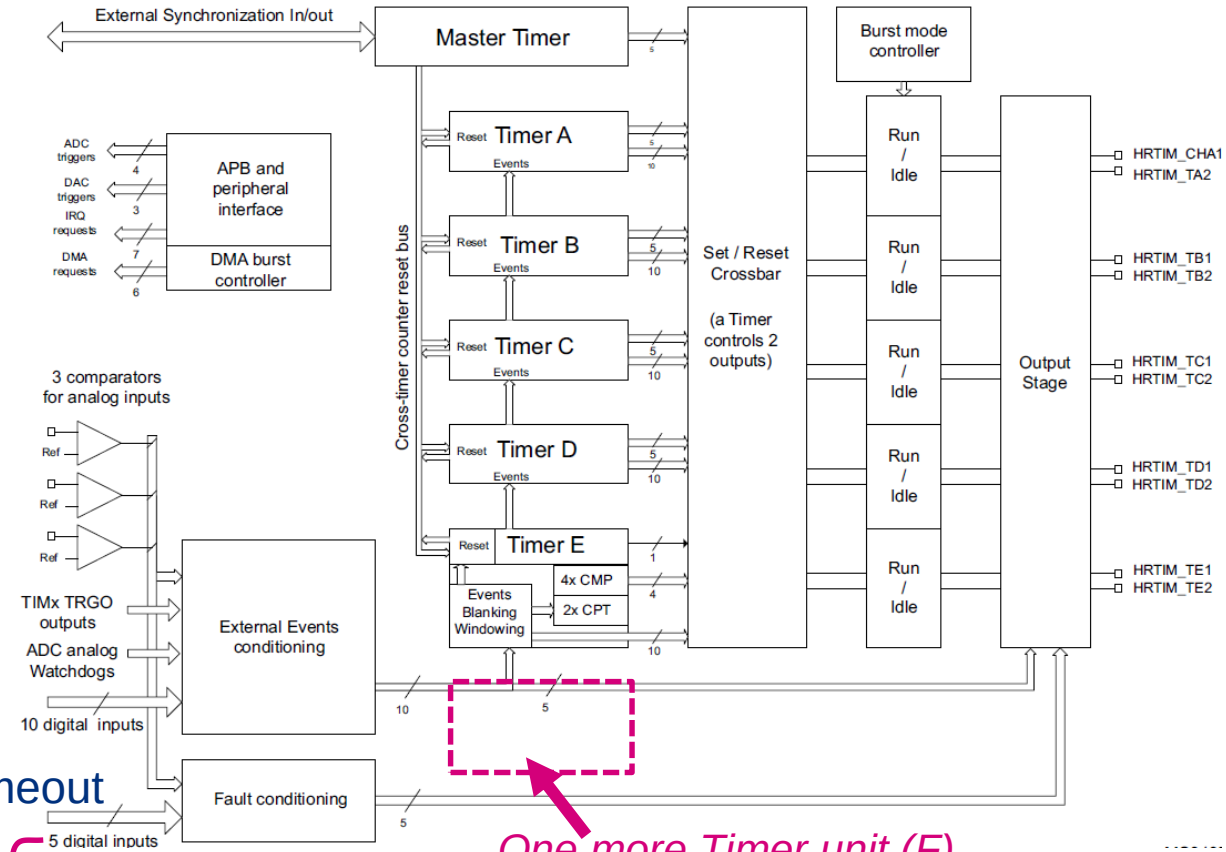
G4 series

- Feature list
  - **Valley skipping** counter (event counter-based blanking)
  - **Slope compensation** (High-speed DAC triggering unit)
  - **Zero duty cycle** forced when CMP = 0 (developer’s friendliness)
  - **6th timing unit** (for triple interleaved LLC) → 12 outputs
  - **Re-synchronized update** mode → Special mechanism for **interleaved LLC** (Synchronous rectification control with phase-shift advance), with asynchronous update option
  - **New protection schemes**
    - Blanking on fault signals
    - Stop on over-current before PWM start (short-circuit protection)
    - Fault after multiple pulses
  - HW re-enable of balanced idle
  - Push-Pull
    - Counter reset mode
    - Deadtime (safety feature)
  - “Greater than” PWM mode (CNT<CMP should be active otherwise inactive)
  - Up/down counting mode for direct ADC sampling at middle on T_{ON}
  - **Multi phase support** for triple and quad interleaved solution (1 register set by user → 3, 4 registers updated automatically)

HRTIM Overview

F3 and G4 series

- Modular architecture: one master and 6 timer sub-units that can be cross-synchronized
- Digital@170MHz followed by analog DLL
- High-resolution
  - 184 ps on all Outputs
- Self-compensated
  - No Temp/Vdd drift
- Up to 12 PWMs outputs
- Multiple faults/events In
- Minimizes SW overhead
- Complex event handling
  - Blanking / windowing / timeout



6th timing unit

- The timer F unit has been added to have a total of 12 outputs available, together with a 6th FAULT input
- Rational: possibility to address larger converters
  - Triple-interleaved half-bridge LLC, requiring 3 x 4 outputs
    - 2x at primary for half-bridge control and 2x at secondary for synchronous rectification
  - Dual interleaved full-bridge LLC (2x 6 outputs)
  - Dual phase-shift full bridge converter (2x 6 outputs)
- Implementation
  - Timer F New control / status bits have been added in reserved areas, to maintain partial compatibility whenever possible
  - Still, as many registers were full, the option was chosen to maintain all bits in single 32-bit registers, but breaking compatibility
  - When bit position was changed, this is managed transparently by the HAL / LL

Compatibility loss v1 to v2

- Events mapping across timers
  - source events that can be used in a destination timer to set or reset the outputs
  - In most cases, 2 combinations are left out of the 3 were available on the v1

Table 174. Events mapping across timer A to F

Source		Timer A				Timer B				Timer C				Timer D				Timer E				Timer F			
		CMP1	CMP2	CMP3	CMP4	CMP1	CMP2	CMP3	CMP4	CMP1	CMP2	CMP3	CMP4	CMP1	CMP2	CMP3	CMP4	CMP1	CMP2	CMP3	CMP4	CMP1	CMP2	CMP3	CMP4
Destination	TA	-	-	-	-	1	2	-	⊠	-	3	4	-	5	6	-	-	-	-	7	8	-	-	-	9
	TB	1	2	-	⊠	-	-	-	-	-	-	3	4	-	-	5	6	7	8	-	-	-	-	9	-
	TC	-	1	2	-	-	3	4	-	-	-	-	-	-	5	-	6	-	⊠	7	8	-	9	-	-
	TD	1	-	-	2	-	3	-	4	⊠	-	⊠	5	-	-	-	-	6	-	-	7	8	-	9	-
	TE	-	-	⊠	1	-	-	2	3	4	5	-	-	6	7	-	⊠	-	-	-	-	-	-	8	9
	TF	-	-	1	-	2	-	-	3	4	-	-	5	-	-	6	7	-	8	9	-	-	-	-	-

New Removed on v2

Compatibility loss v1 to v2

- Blanking and windowing
  - source that can be used in a destination timer to condition the external events
  - In most cases, 2 combinations are left out of the 3 were available on the v1
  - Coupling between adjacent timers are privileged

Table 182. Filtering signals mapping per timer

Source		Timer A				Timer B				Timer C				Timer D				Timer E				Timer F			
		CMP1	CMP2	CMP4	TA2	CMP1	CMP2	CMP4	TB2	CMP1	CMP2	CMP4	TC2	CMP1	CMP2	CMP4	TD2	CMP1	CMP2	CMP4	TE2	CMP1	CMP2	CMP4	TF2
Destination	Timer A	-	-	-	-	1	-	2	3	4	-	5	X	7	-	-	-	-	8	-	-	6	-	-	-
	Timer B	1	-	2	3	-	-	-	-	4	5	-	X	-	7	-	-	8	-	-	-	-	6	-	-
	Timer C	-	1	-	-	2	-	3	X	-	-	-	-	5	-	6	7	-	-	8	-	4	-	-	-
	Timer D	1	-	-	-	-	2	-	-	3	4	-	5	-	-	-	-	6	-	7	X	-	-	8	-
	Timer E	-	1	-	-	2	-	-	-	3	-	X	X	6	-	7	8	-	-	-	-	-	-	4	5
	Timer F	-	-	1	-	-	2	-	-	-	-	3	-	-	4	5	-	6	-	7	8	-	-	-	-

New

Removed on v2

Table 183. Windowing signals mapping per timer (EEFLTR[3:0] = 1111)

Destination	Timer A	Timer B	Timer C	Timer D	Timer E	Timer F
TIMWIN (source)	Timer B CMP2	Timer A CMP2	Timer D CMP2	Timer C CMP2	Timer F CMP2	Timer E CMP2

Timer D CMP2 on HRTIMv1

Compatibility loss v1 to v2

- ADC triggers 1 to 4
  - 5 and 4 Timer F sources replacing previous events, spread among all timers

20.5.66 HRTIM ADC trigger 1 register (HRTIM_ADC1R)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADC3 TEPER	ADC3 TEC4	ADC3 TEC3	ADC3 TFRST	ADC3 TDPER	ADC3 TDC4	ADC3 TDC3	ADC3 TFPER	ADC3 TCPER	ADC3 TCC4	ADC3 TCC3	ADC3 TFC4	ADC3 TBRST	ADC3 TBPER	ADC3 TBC4	ADC3 TBC3
rw	rw	rw	**TEC2**	rw	rw	rw	**TDC2**	rw	rw	rw	**TCC2**	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC3 TFC3	ADC3 TARST	ADC3 TAPER	ADC3 TAC4	ADC3 TAC3	ADC3 TFC2	ADC3 EEV5	ADC3 EEV4	ADC3 EEV3	ADC3 EEV2	ADC3 EEV1	ADC3 MPER	ADC3 MC4	ADC3 MC3	ADC3 MC2	ADC3 MC1
TBC2	rw	rw	rw	rw	**TAC2**	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

20.5.67 HRTIM ADC trigger 2 register (HRTIM_ADC2R)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADC4 TERST	ADC4 TEC4	ADC4 TEC3	ADC4 TEC2	ADC4 TDRST	ADC4 TDPER	ADC4 TDC4	ADC4 TFPER	ADC4T DC2	ADC4T CRST	ADC4T CPER	ADC4T CC4	ADC4 TFC4	ADC4T CC2	ADC4T BPER	ADC4T BC4
rw	rw	rw	rw	rw	rw	rw	**TDPER**	rw	rw	rw	rw	**TCC3**	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC4 TFC3	ADC4 TBC2	ADC4 TAPER	ADC4 TAC4	ADC4 TFC2	ADC4 TAC2	ADC4 EEV10	ADC4 EEV9	ADC4 EEV8	ADC4 EEV7	ADC4 EEV6	ADC4 MPER	ADC4 MC4	ADC4 MC3	ADC4 MC2	ADC4 MC1
TBC3	rw	rw	rw	**TAC3**	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

New (previous configuration mentioned below)

Compatible v1 to v2

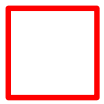
- Counter reset sources
  - The 2 new Timer F sources (CMP1, CMP2) are placed on previously reserved bit
  - Applies to the 6 registers: HRTIM_RSTAR..HRTIM_RSTFR

20.5.33 HRTIM timer A reset register (HRTIM_RSTAR)

Address offset: 0x0D4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIMF CMP2	TIME CMP4	TIME CMP2	TIME CMP1	TIMD CMP4	TIMD CMP2	TIMD CMP1	TIMC CMP4	TIMC CMP2	TIMC CMP1	TIMB CMP4	TIMB CMP2	TIMB CMP1	EXT EVNT 10	EXT EVNT9	EXT EVNT8
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXT EVNT7	EXT EVNT6	EXT EVNT5	EXT EVNT4	EXT EVNT3	EXT EVNT2	EXT EVNT1	MST CMP4	MST CMP3	MST CMP2	MST CMP1	MST PER	CMP4	CMP2	UPDT	TIMF CMP1
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw



New

Compatible v1 to v2

- Capture 1 and 2 trigger sources
  - The 4 new Timer F sources (CMP1, CMP2, SET and RESET) are placed on previously reserved bit

20.5.40 HRTIM timer A capture 1 control register (HRTIM_CPT1ACR)

Address offset: 0x0DC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TE CMP2	TE CMP1	TE1 RST	TE1 SET	TD CMP2	TD CMP1	TD1 RST	TD1 SET	TC CMP2	TC CMP1	TC1 RST	TC1 SET	TB CMP2	TB CMP1	TB1 RST	TB1 SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TF CMP2	TF CMP1	TF1 RST	TF1 SET	EXEV10CPT	EXEV9 CPT	EXEV8 CPT	EXEV7 CPT	EXEV6 CPT	EXEV5 CPT	EXEV4 CPT	EXEV3 CPT	EXEV2 CPT	EXEV1 CPT	UPD CPT	SW CPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

New

FAULT6 Control bits

- Very same programming as FAULT1..FAULT5
  - Control bits placed in HRMTIM_FLTINR2

20.5.72 HRTIM fault input register 2 (HRTIM_FLTINR2)

Address offset: 0x3D4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	FLTSD[1:0]		Res.	Res.	FLT6 SRC[1]	FLT5 SRC[1]	FLT4 SRC[1]	FLT3 SRC[1]	FLT2 SRC[1]	FLT1 SRC[1]
						rw	rw			rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLT6 LCK	FLT6F[3:0]				FLT6 SRC[0]	FLT6P	FLT6E	FLT5 LCK	FLT5F[3:0]				FLT5 SRC[0]	FLT5P	FLT5E
rwo	rw	rw	rw	rw	rw	rw	rw	rwo	rw	rw	rw	rw	rw	rw	rw

New

Current mode power supplies

- Peak current mode control technique features advantages vs voltage mode, among them:
  - Better line regulation
  - Easier to parallel
  - Current limitation comes for free
- …but:
  - current sensor is difficult
  - Requires a slope compensation

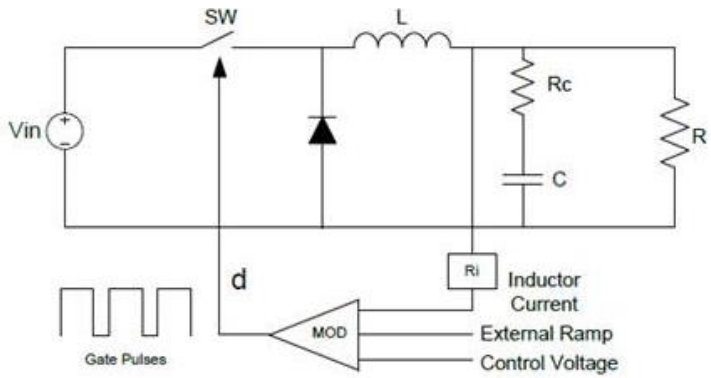
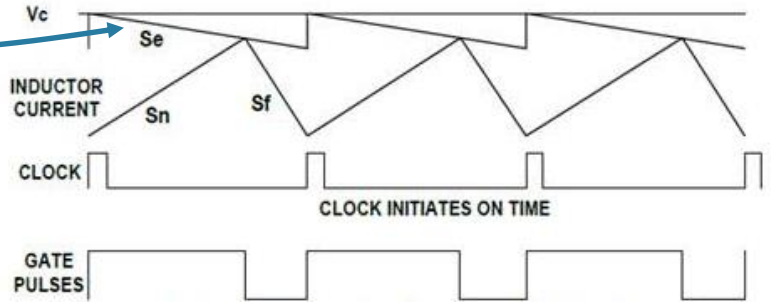
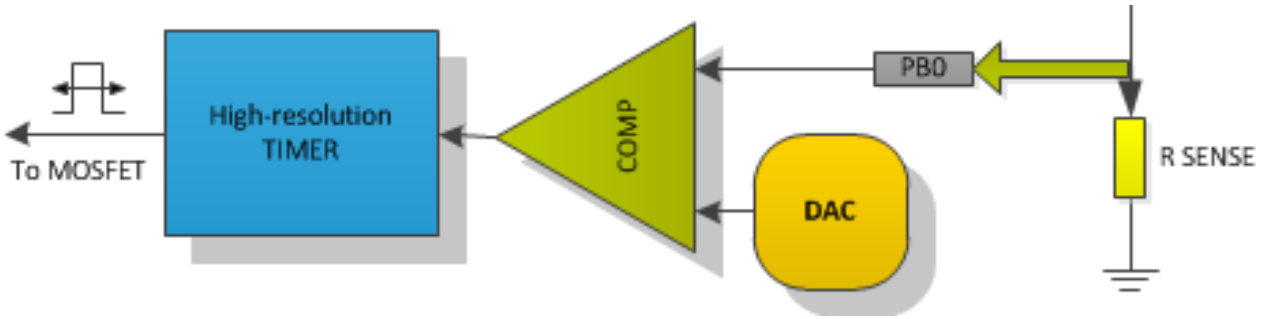


Figure 1. Buck converter with peak current mode control



Slope Compensation (context)

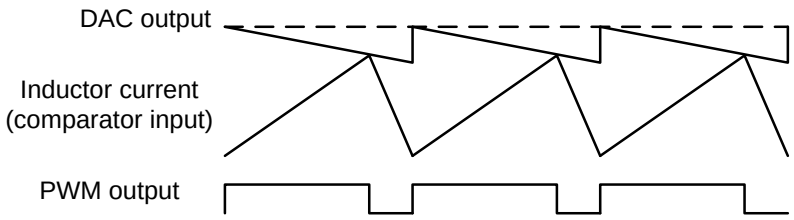
- Implemented for stabilizing peak current-mode PWM converters when duty cycle is above 50% (inverted buck demo on F334-DSICO)



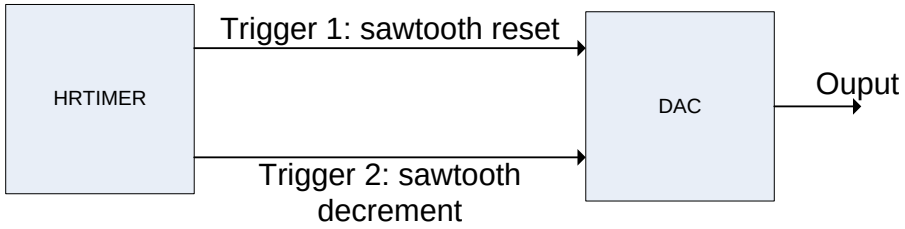
- Managed using DMA or using few CMP registers on HRTIMERv1
- Now built-in the HRTIMERv2 itself
  - Lower resources consumption (no DMA channel, used, no DMA traffic)
  - Possibility to have a much higher number of steps

Slope compensation

- This is done by applying a negative saw tooth shape (slope) on the current comparator, using the DAC
  - This sawtooth must be synchronized with the PWM



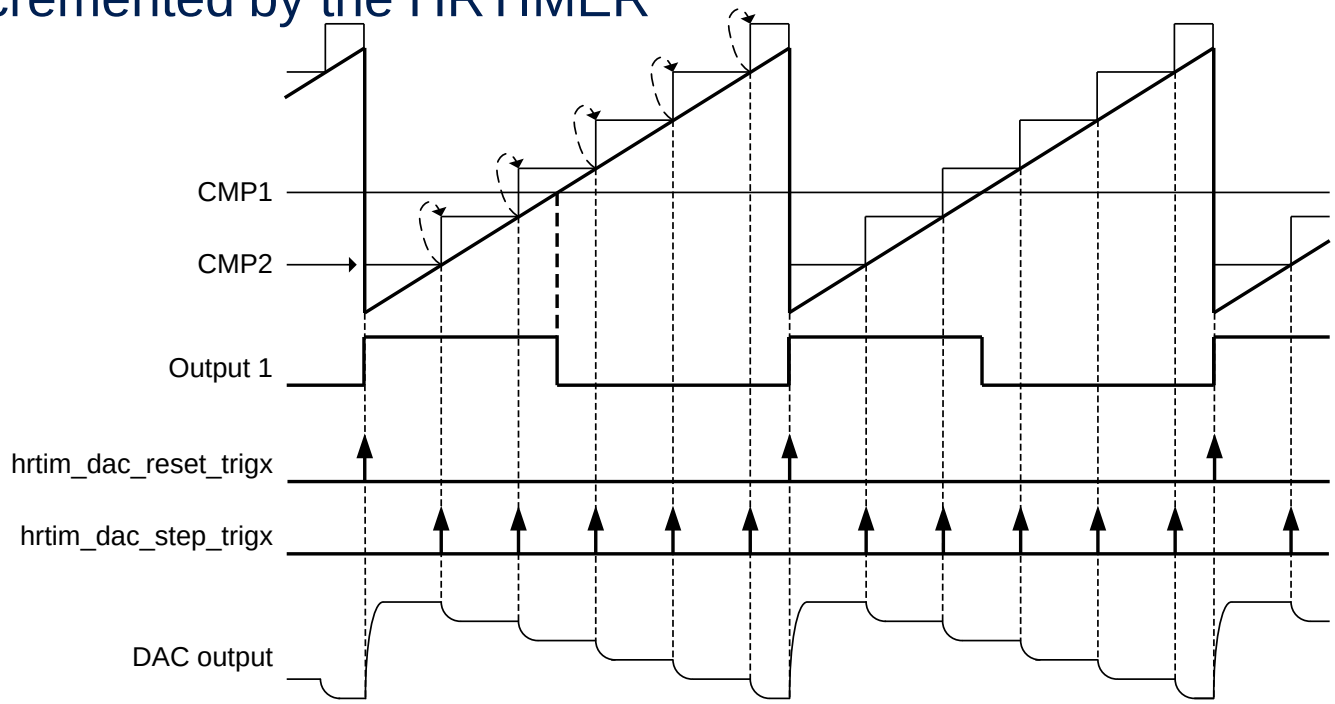
- The HRTIMERv2 features two DAC output triggers
  - For resetting (synchronizing) the sawtooth
  - For decrementing the DAC values



Using Slope compensation

- 2 control bits allows to program the DAC reset and DAC step events
  - Usually, DAC reset on period and DAC steps on CMP2
  - Other option possible (DAC square wave for hysteretic control)

- The CMP2 defines the number of steps and is automatically incremented by the HRTIMER

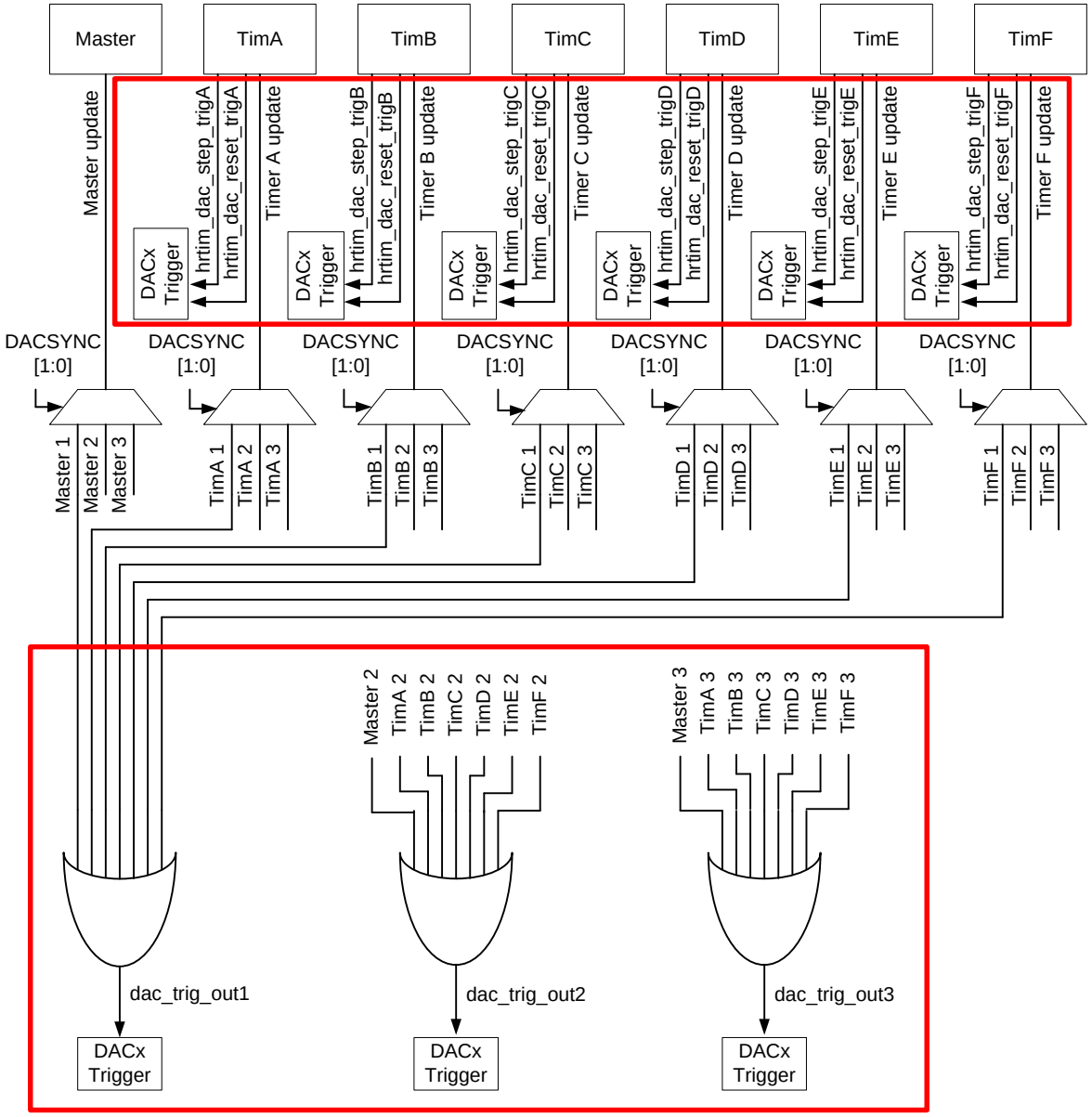


DAC triggers circuitry update

New triggers

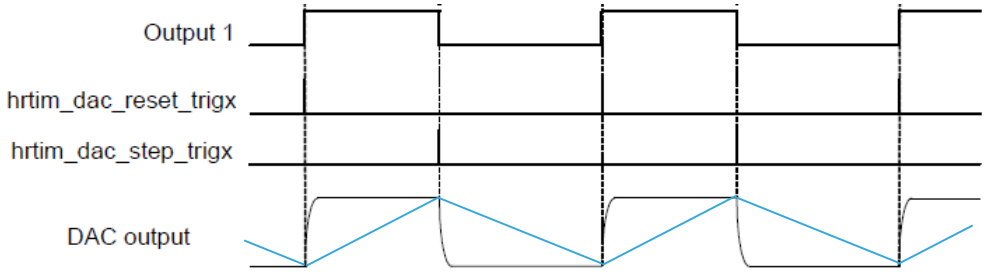
The triggers are redirect to all DAC with dual trigger capability

Legacy triggers



Configuring Dual channel DAC triggers

- The Reset and step triggers can be configured with 2 programming bits, in the 4 following modes:
  - Edge-aligned slope compensation: the sawtooth starts on PWM period beginning and multiple triggers are generated during the period
  - Center-aligned slope compensation: the sawtooth starts on the output set event and multiple triggers are generated during the period
  - Hysteretic controller: the DAC values are just changed twice per period, when the output state changes (2 triggers are generated per PWM period). In edge-aligned mode, the triggers are generated on counter reset or rollover. In center-aligned mode, the triggers are generated when the output is set.



Slope compensation pitfalls

- The CMP2 value cannot be programmed with a value below 3 f_{HRTIM} clock (anyway gives a max sampling rate above DAC spec)
- The rounding error can bring unnecessary triggers
  - Example: TIMxPER= 8192 and 6 triggers yields 1365.3

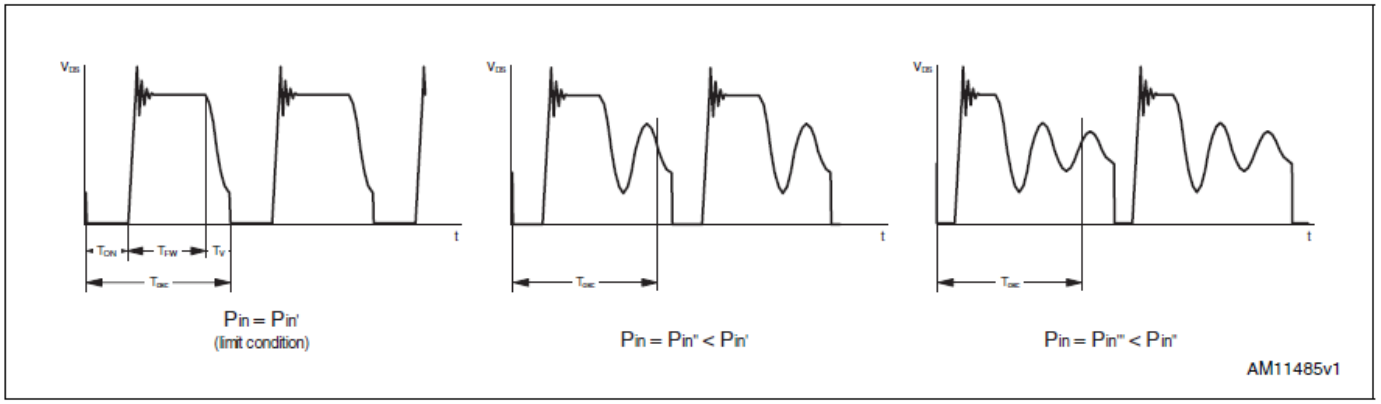
-	CMP2 = 1365	dac_trg	dac_step_trg	CMP2 = 1366	dac_trg	dac_step_trg
Counter value	1365	-	1	1366	-	1
	2730	-	2	2732	-	2
	4095	-	3	4098	-	3
	5460	-	4	5464	-	4
	6825	-	5	6830	-	5
	8190	-	6	8192	6	-
	8192	7	-	1366	-	1
	1365	-	1	2732	-	2
	...	-	-	...	-	-

- The final CMP2 value must not be equal to 0x0000
- In centered-pattern mode, it is mandatory to have an even number of triggers per switching period, to avoid unevenly spaced triggers

External Event counter (1/2)

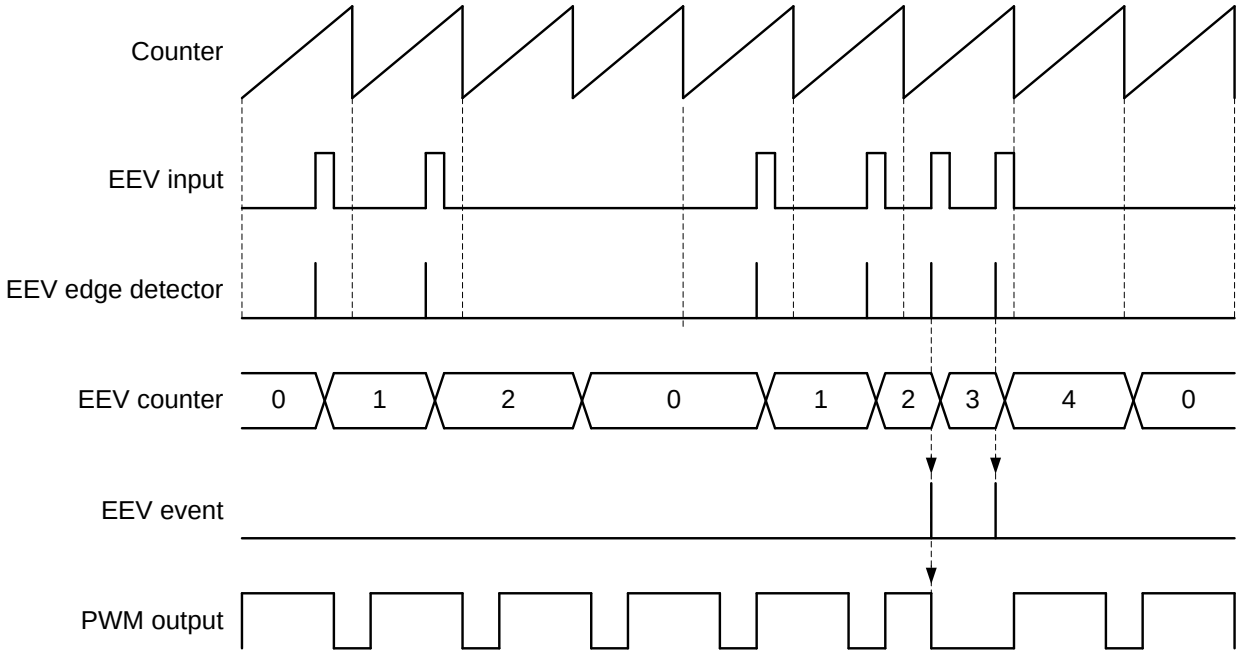
- The HRTIM v1 offers many options for *timing-driven filtering* (blanking and windowing)
  - Typical use case: leading edge blanking (LEB)
- The HRTIM v2 features event-based filtering: an external event must have occurred a given number of times before being considered valid
  - Typical use case: valley skipping mode for flyback converters
    - At low-load, the next PWM cycle must start after N cycles of ringing (the lower the laod, the higher N)

Figure 9. Drain ringing cycle skipping as the load is gradually reduced

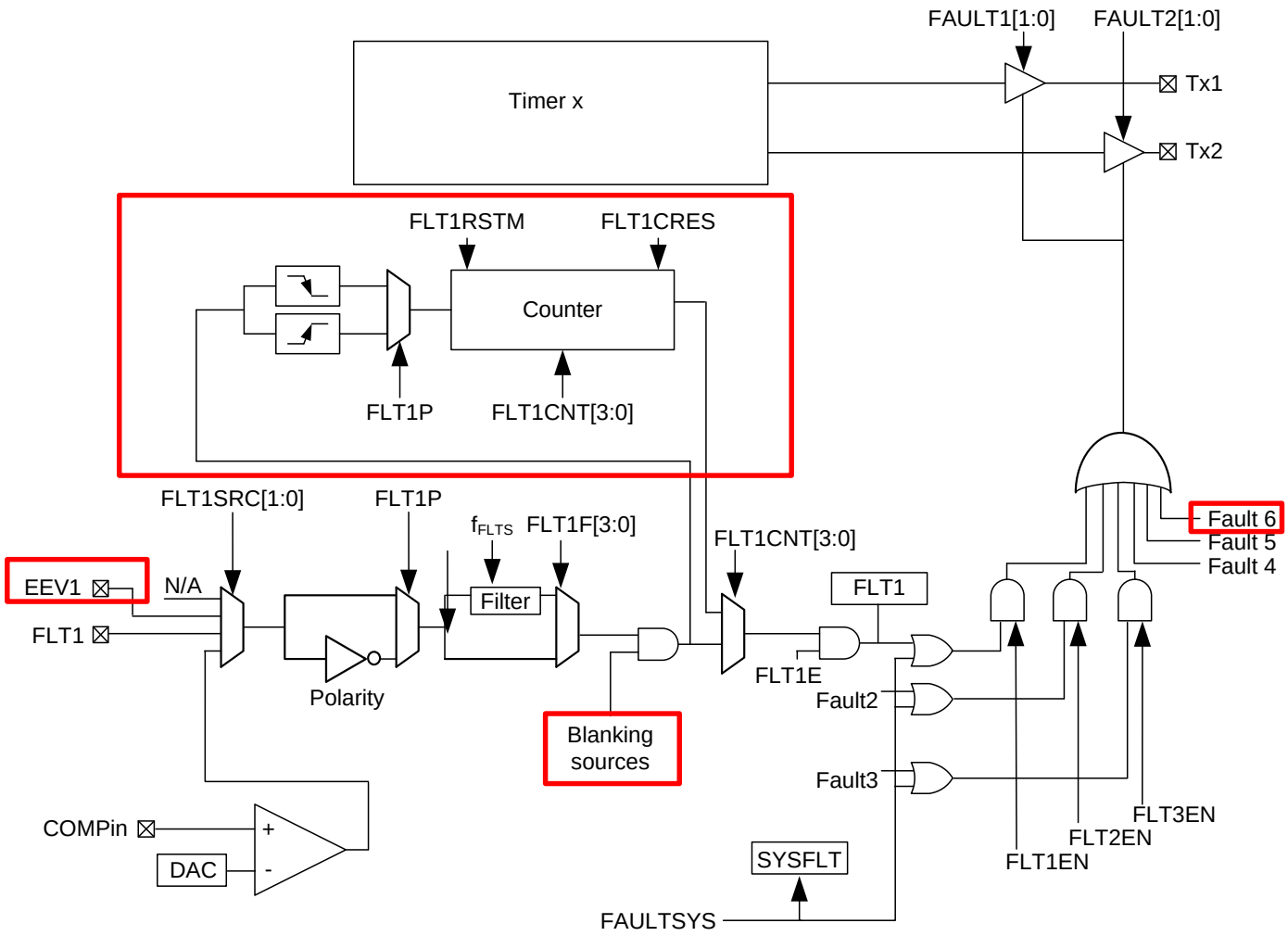


External Event counter (2/2)

- Immediate mode
  - Event is generated as soon as N consecutive events are occurring during a PWM period
    - Event counter is reset on each and every new PWM period
- Cumulative mode (figure below)
  - event must occur at least once during multiple PWM period
    - counter is reset only if the event did not appear during the last PWM period



Extended FAULT features



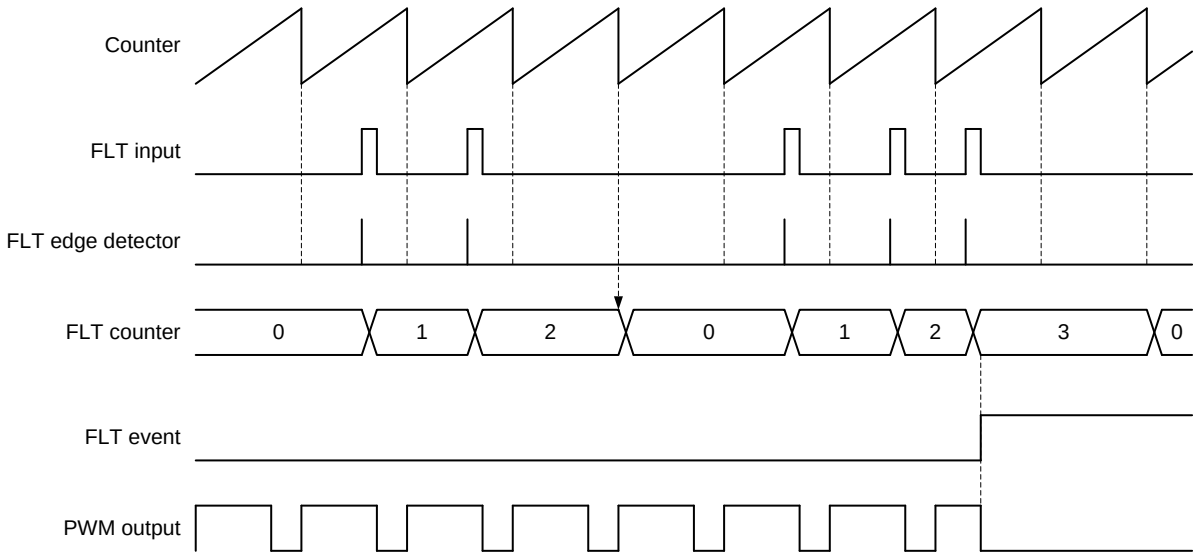
FAULT blanking

- Possibility to add blanking with 2 options:
  - At turn-on (leading-edge blanking)
  - In between CMP3 and CMP4 events
- Each FLTx blanking window is associated with one timer

Fault Input	Blanking window source
FLT1	Timer A
FLT2	Timer B
FLT3	Timer C
FLT4	Timer D
FLT5	Timer E
FLT6	Timer F

Fault counter 1/2

- The fault counter have 2 operating modes
  - Immediate mode
    - The fault is generated as soon as N consecutive faults are occurring during a PWM period
      - Event counter is reset on each and every new PWM period
  - Cumulative mode (figure below, counter = 2)
    - The fault must occur at least once during multiple PWM period
      - counter is reset only if the event did not appear during the last PWM period



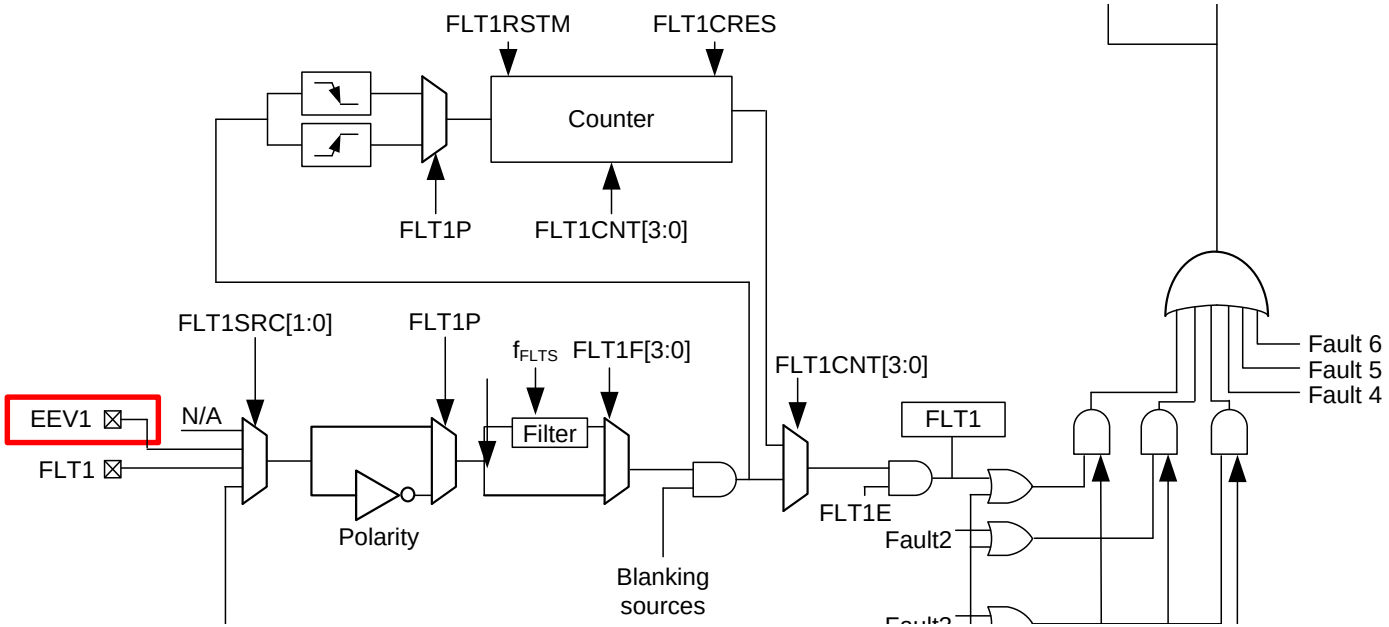
Fault counter 2/2

- A FLTx input on which the counter is applied can be connected to several timing units
- A given FLTx input counter can be reset by a single source

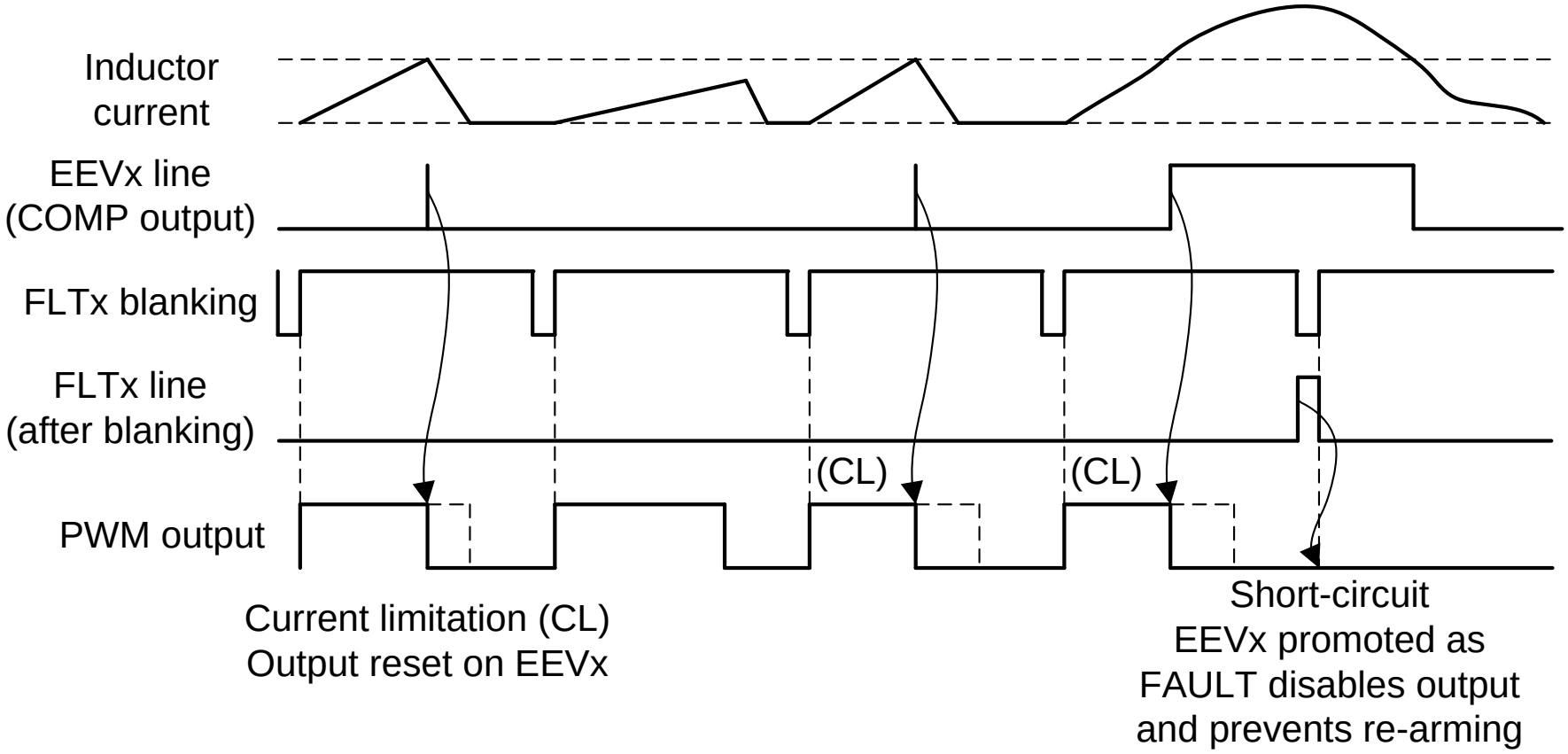
Fault Input	Fault counter Reset source
FLT1	Timer A reset/roll-over
FLT2	Timer B reset/roll-over
FLT3	Timer C reset/roll-over
FLT4	Timer D reset/roll-over
FLT5	Timer E reset/roll-over
FLT6	Timer F reset/roll-over

Extended FAULT features

- Possibility to have an event converted into fault
  - If the over-current is present before the start of the pulse (output set, it is promoted as a Fault and shut-down the system)



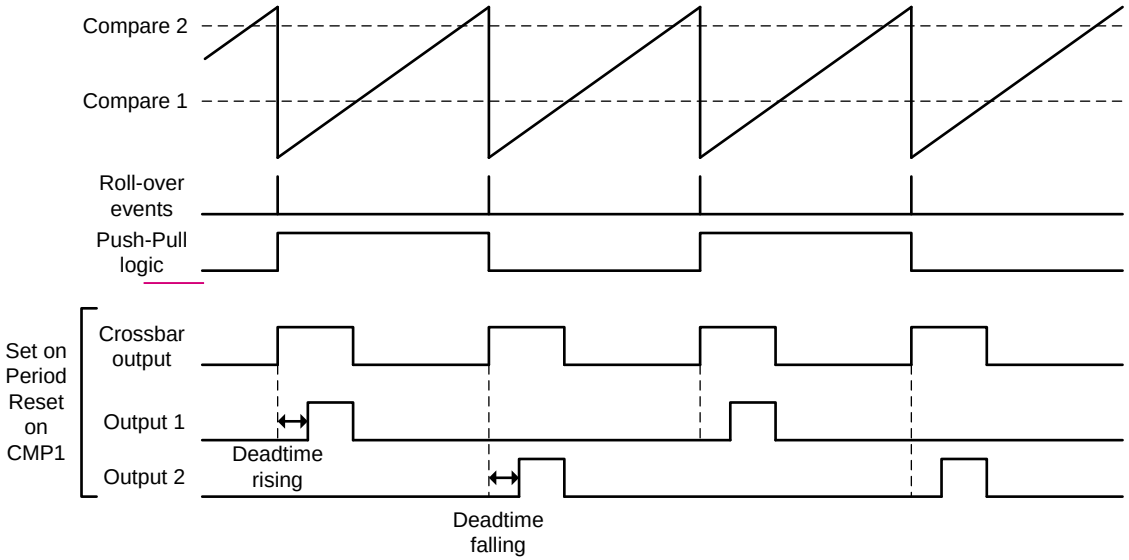
Short-circuit protection



For simplicity, the Ton min on PWM is not represented here

Push-Pull improvements

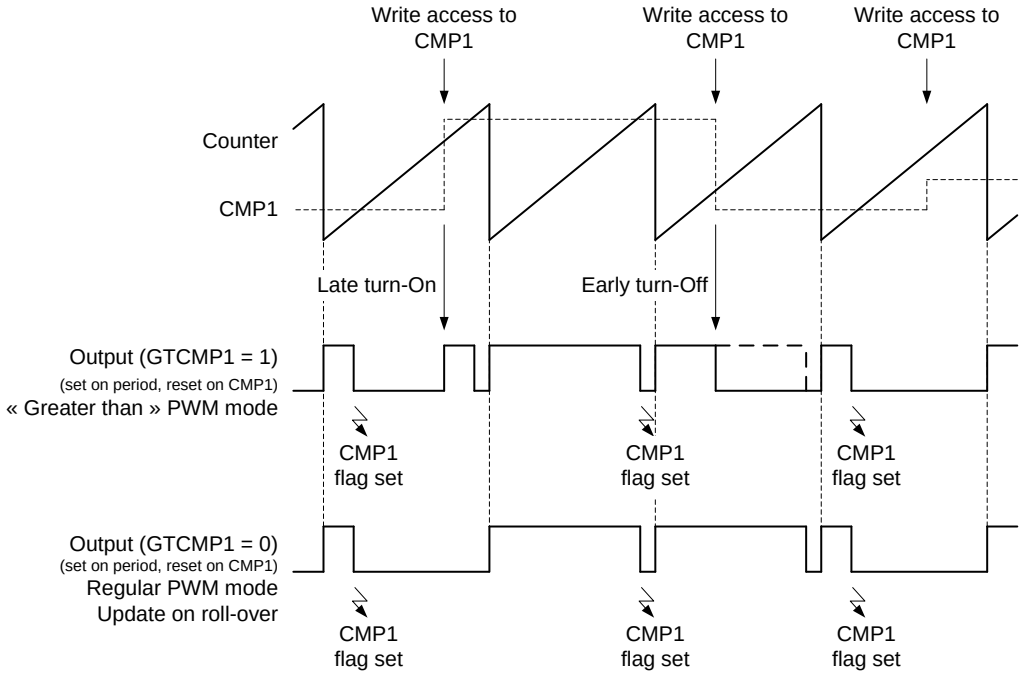
- Possibility to enable the deadtime mode together with push-pull
  - Hardware protection against erroneous 100% duty cycle setting (risk of shoot-through when controlling half-bridges)



- Possibility to use the push-pull mode with counter reset
  - Allows to use the push-pull mode for topologies with variable frequency PWM (LLC)

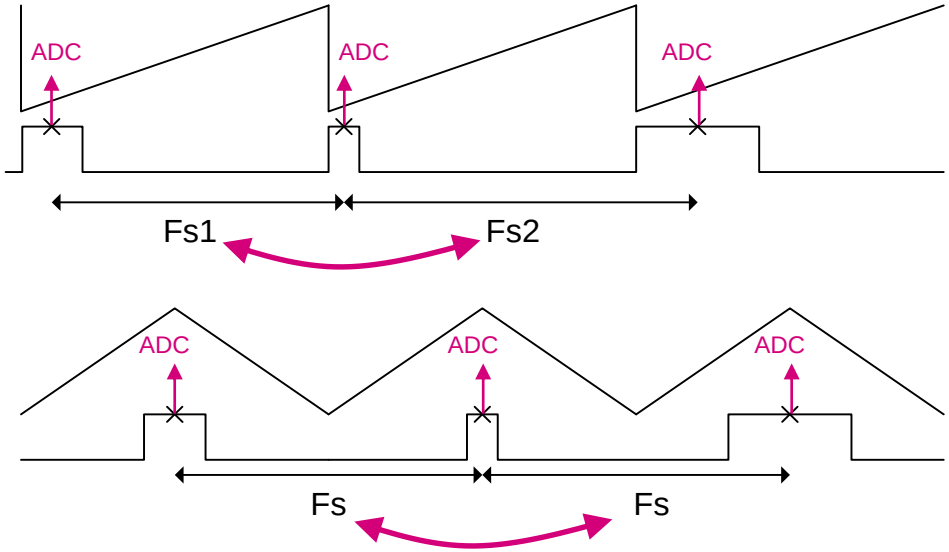
Classical PWM mode

- For CNT<CCR1 the output must be active otherwise inactive
- Rationale: possibility to work without any preload and force the state at the time the CMP1 is written
  - Early turn-off, late turn-on
- One single compare register (CMP1)



Up/Down mode(1/2)

- Useful for power supplies or motor-control applications, for instance:
  - Two 3-phase brushless motor
  - Three DC or stepper motors with full-bridges
- Simplifies the ADC sampling
  - Constant sampling frequency
  - Sampling at the middle of the pulse

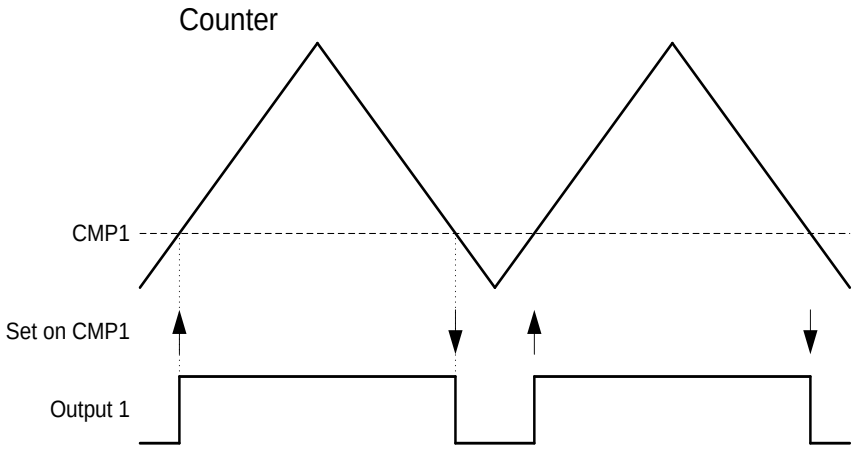


Up/Down mode(2/2)

- The following features are supported in up-down counting mode:
  - Half mode
  - Deadtime insertion
  - Push-pull mode, push-pull toggle done when counter = 0
  - Delayed Idle
  - Burst mode
- The following features are not supported in up-down counting mode:
  - Auto-delayed mode
  - Balanced Idle
- The capture function is supported with the following differences:
  - the capture value is referred to counting start, when up-counting
  - the capture value is referred to the PER event when down counting
  - the bit 16 of the capture register holds the counting direction status

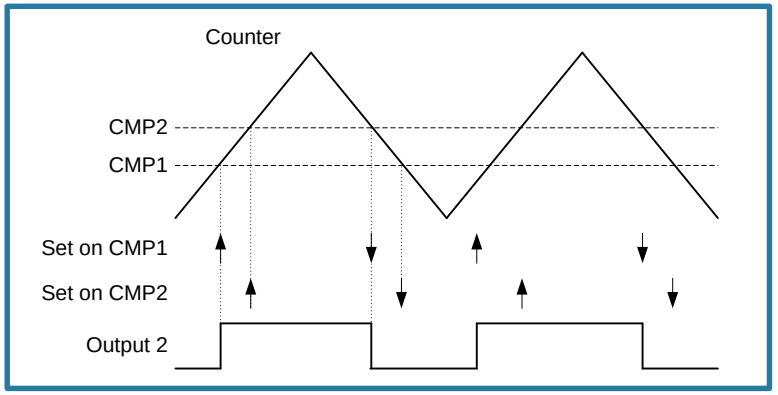
Using the Up/Down mode

- The UDM bits allows to select Up-only and Up/Down mode
- The set/reset crossbar programming differs:
  - An event enabled in HRTIM_SETxyR will set the output during up-counting and reset the output during down-counting
  - An event enabled in HRTIM_RSTxyR will reset the output during up-counting and set the output during down-counting

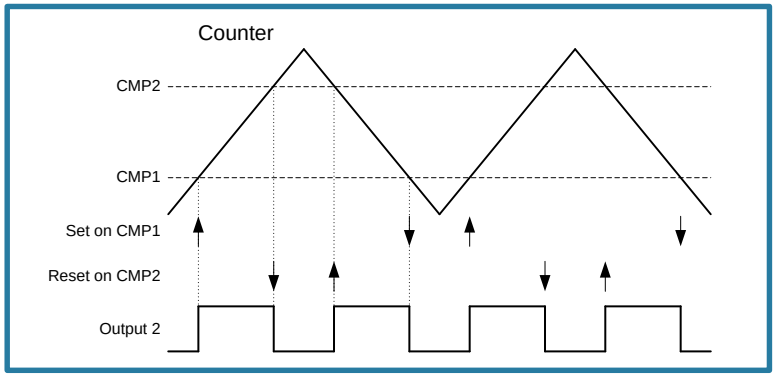


Other possibilities with Up/Down mode

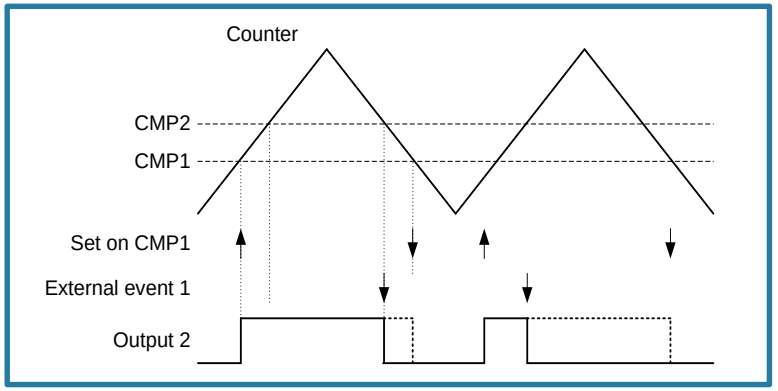
Asymmetric waveform
(CMP2 must be > CMP1)



Double frequency
(or zero voltage vector insertion for single-shunt motor control)

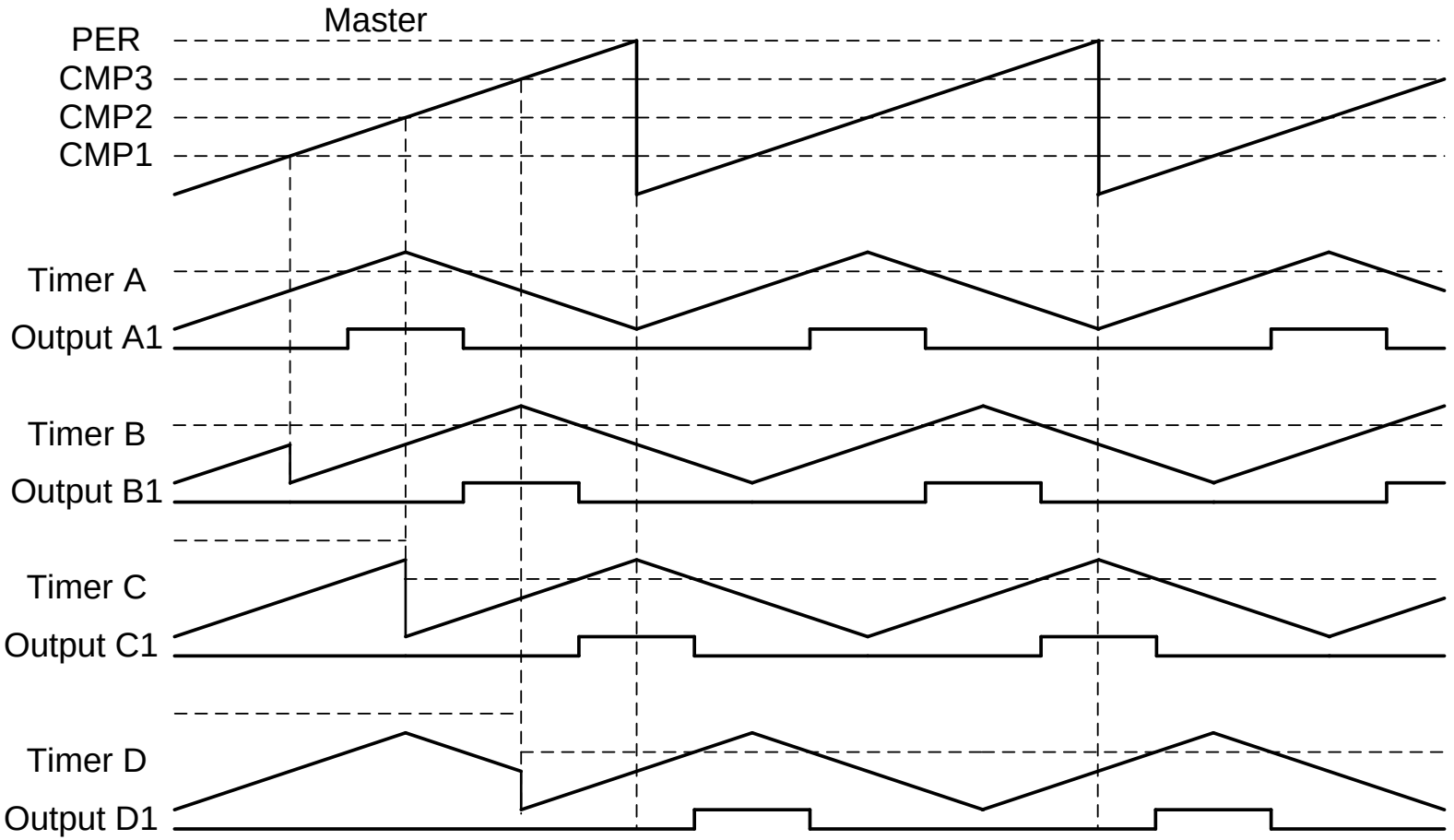


Cycle-by-cycle current control also supported
(EEVx always reset regardless of up/down)



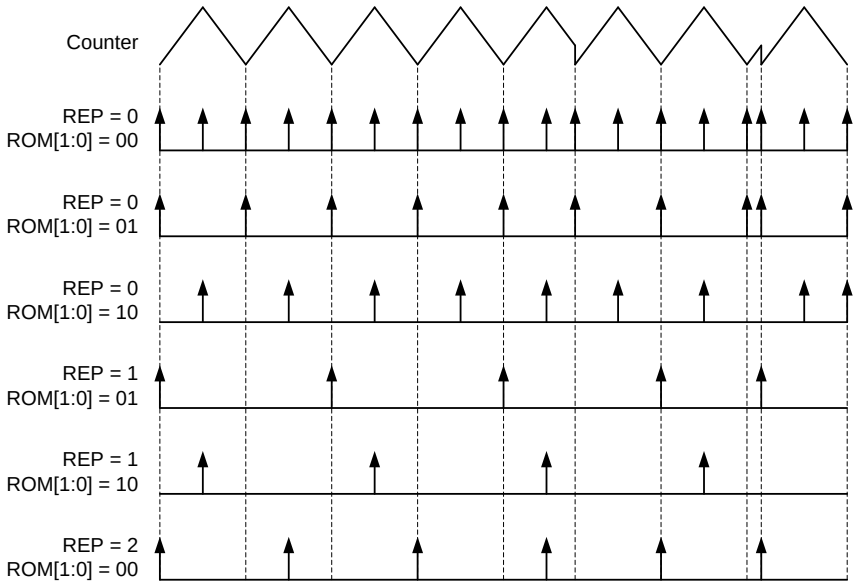
Up/Down mode

- Multi-phase up-down mode



Roll-over event in Up/Down mode 1/2

- The Roll-over definition changes in Up/Down mode. It can be generated either:
  - When the counter is equal to 0 (“valley” mode)
  - When the counter reaches the period (“crest” mode)
- Several programming bits are available for defining when it has to be generated, for output set/reset, IRQ/DMA, ADC, repetition counter,…

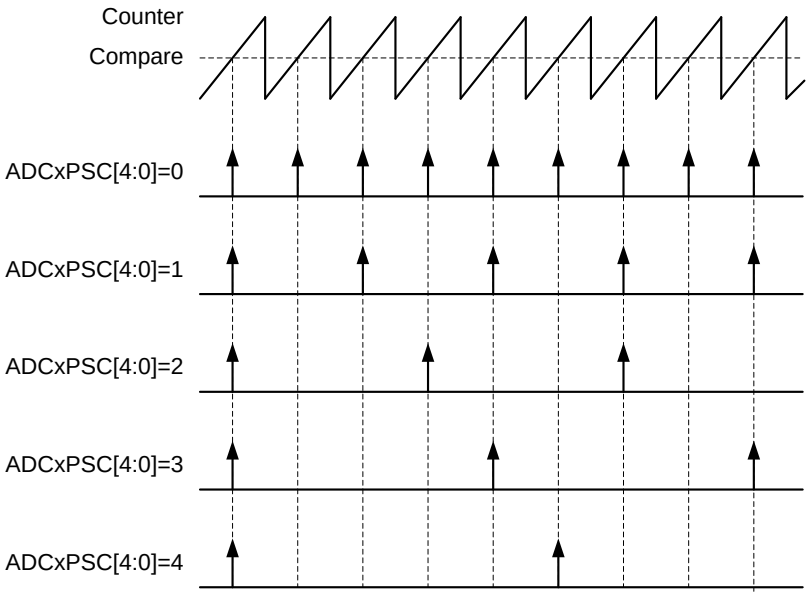


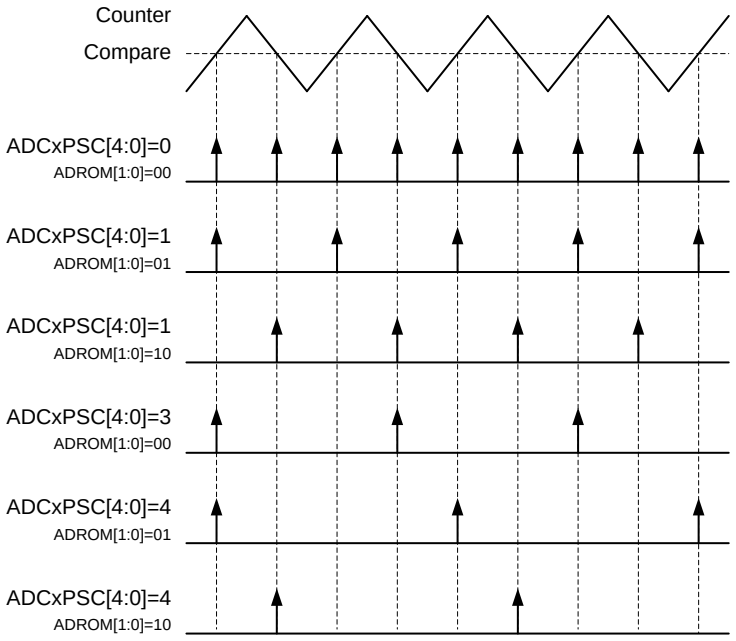
ADC triggers extended for 5 ADCs

- The number of ADC triggers is extended from 4 to 10 triggers
- The triggers 1..4 (legacy) now include TimF trigger sources
- Triggers 5..10 are added, with standard setting
  - 5 control bits only
  - A single source out of 32 (no possibility for multiple sources per trigger)
- ADC trigger register update principle is maintained (one timer to be selected to update a given ADC trigger register)

ADC post-scaler

- For high switching-frequency application, it is possible to reduce the ADC triggering rate with the ADC post-scaler
- Each ADC trigger can be individually adjusted down to 1 out of 32





No-overhead duty cycle zeroing

- It has been reported several times that zeroing duty cycle is cumbersome on the HRTIMv1 it
- On HRTIMv2, it is possible to force a null duty cycle by writing a null value in the Compare1 and/or Compare 3 register
- Only works in the following conditions
  - output SET event is generated by the PERIOD event
  - output RESET if generated by the compare 1 (respectively compare 3) event
  - the compare 1 (compare 3) event is active within the timer unit itself, and not used for other timing units

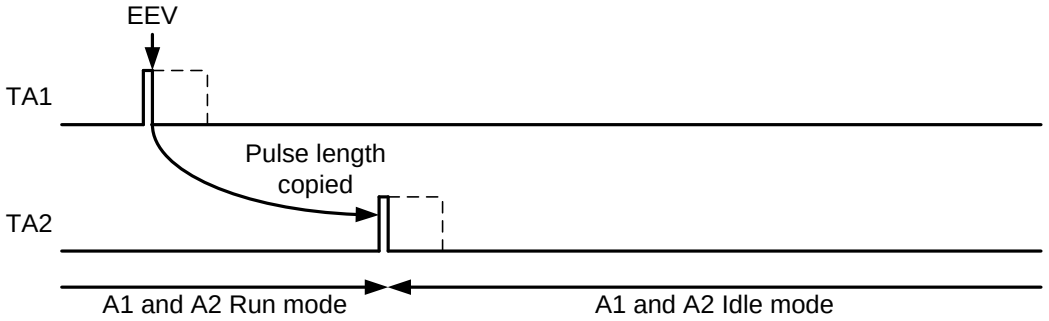
Easier interleaved schemes handling

- Complements existing half mode
  - Useful for having 50% duty cycle and for dual interleaved topologies
- 2 new interleaved modes have been added for triple and quad interleaved or multiphase converters
  - CMP1, CMP2 and CMP3 values are automatically calculated when the new period is written into PERxR

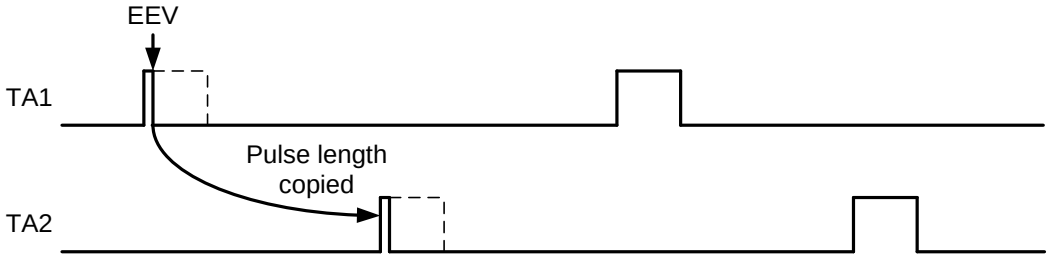
Mode	Dual interleaved 180° HALF=1, INTLVD[1:0]=xx	Triple interleaved 120° HALF=0, INTLVD[1:0]=01	Quad interleaved 90° HALF=0, INTLVD[1:0]=10
CMP1 value	PERxR / 2	PERxR / 3	PERxR / 4
CMP2 value	Not affected	2 * (PERxR / 3)	PERxR / 2
CMP3 value	Not affected	Not affected	3 * (PERxR / 4)

Balanced Idle resuming automatically

- Possibility to have a self re-start in balanced idle mode
  - By default, the PWM is stopped after the balanced idle entry

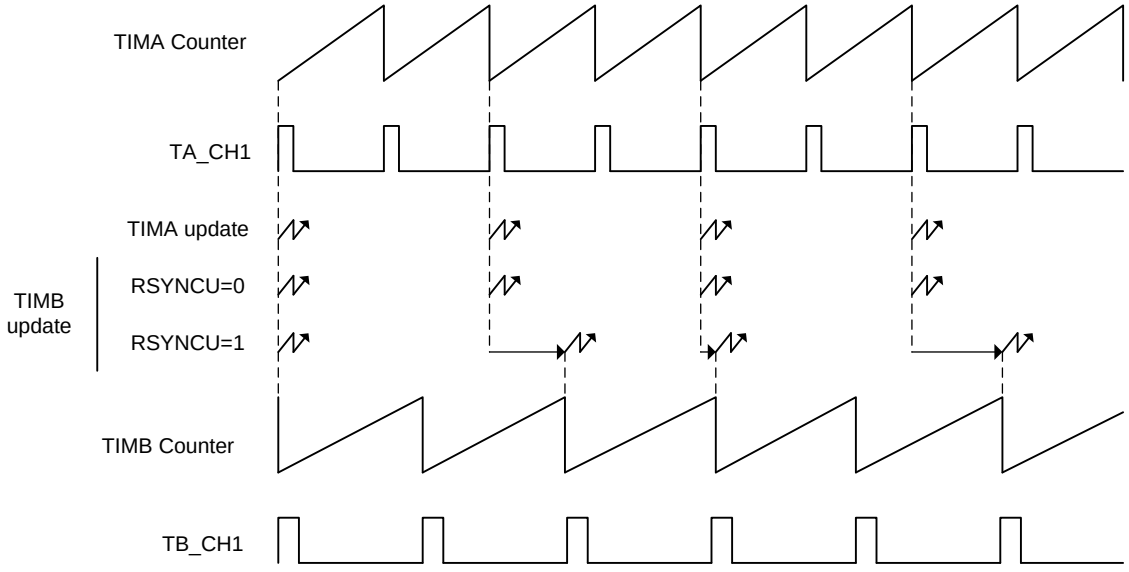


  - If the Balanced Idle Automatic Resume mode is enabled, the PWM resumes normal operation on the cycle following pulse balancing sequence



Re-synchronized update mode

- Useful when multiple timers are combined for a single converter
  - Typically for interleaved LLC
- When a reference timer provides the update event to (multiple) slave timer(s), this event can be either taken into account immediately or delayed up to the next reset / roll-over event. The update from adjacent timers



Swap mode

- Allows to swap 2 outputs in a single register access
  - SET1 and RST1 control registers acting on output 2
  - SET2 and RST2 control registers acting on output 1
- Benefits: reduces CPU burden
  - no need to reprogram the output crossbars
- All control bits located in the same register
  - Possibility to swap multiple PWM pairs simultaneously

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