STM32G4 Technique Training

- Power
- Reset and Clock Control

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STM32G4 - PWR

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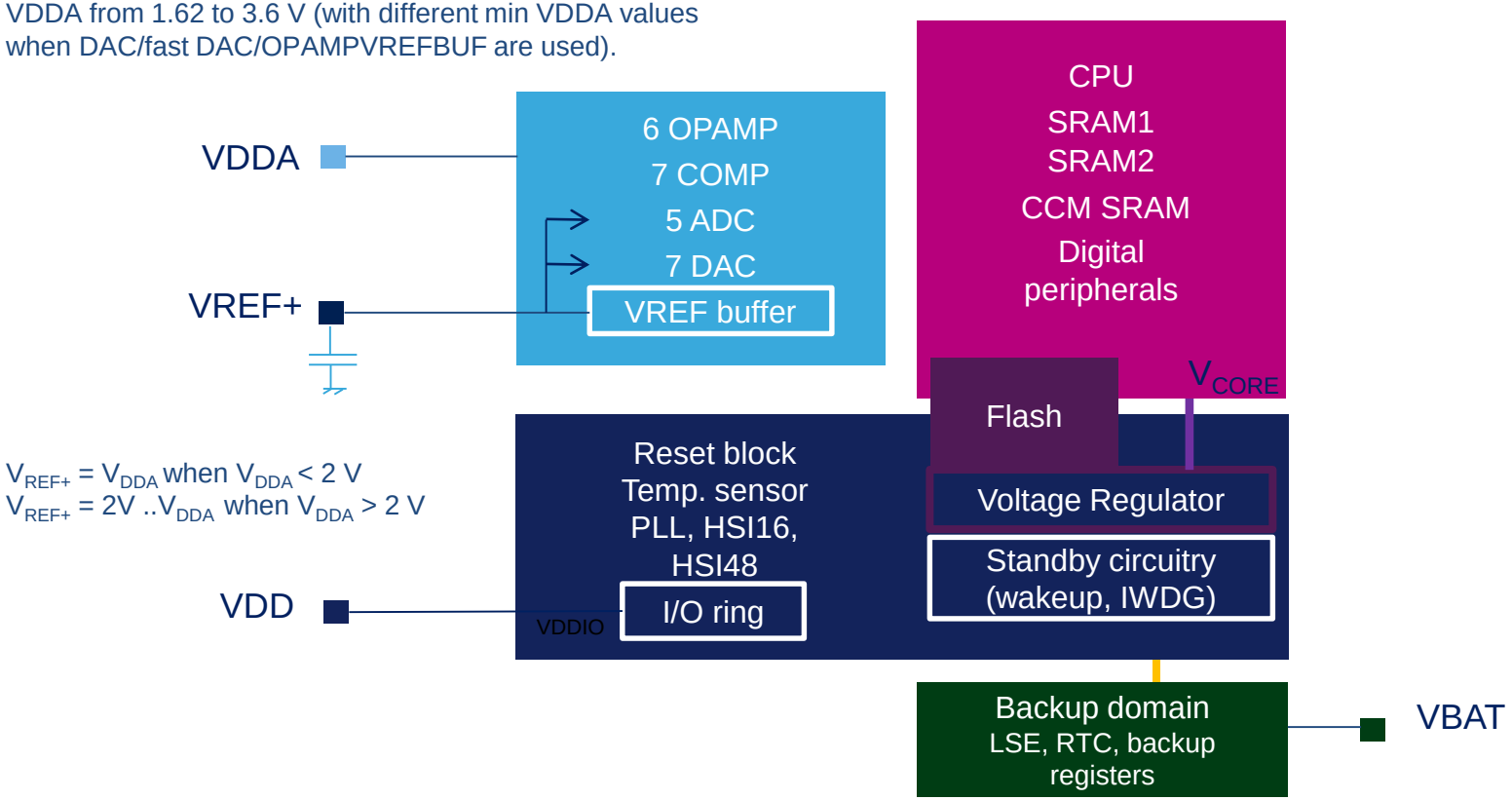
Power schemes

VDDA from 1.62 to 3.6 V (with different min VDDA values when DAC/fast DAC/OPAMPVREFBUF are used).



$V_{REF+} = V_{DDA}$ when $V_{DDA} < 2$ V
$V_{REF+} = 2V .. V_{DDA}$ when $V_{DDA} > 2$ V

Power schemes

- **Optimized power and performance thanks to independent power supplies**

- V_{DD} from 1.71 to 3.6 V
  - VDD must be set if any other independent supply is provided
- V_{DDA} from 1.62 to 3.6 V
- V_{REF+} = V_{DDA} when V_{DDA} < 2 V and from 2V to V_{DDA} when V_{DDA} > 2 V
- V_{BAT} from 1.55 to 3.6V including the RTC and 128-byte backup registers

Power schemes

- **Independent voltage reference supplies**
- **for analog performance**

- VREF+: reference voltage for ADCs and DACs
  - It can be provided either by an external reference voltage or by the internal voltage reference buffer.
  - VREF+ pin, and thus the internal voltage reference, is available in most of packages even in the 64-pin and 48-pin.
  - VREF+ pin, and thus the internal voltage reference, is not available on the 32-pin package.
    - Double-bonded with VDDA which can be connected to an external reference.
    - The internal voltage reference buffer is not available and must be kept disabled.
  - Two VREF+ pins in the LQFP128 package.

Power supply supervisor

- **Safe and ultra-low-power reset management**

- POR & PDR

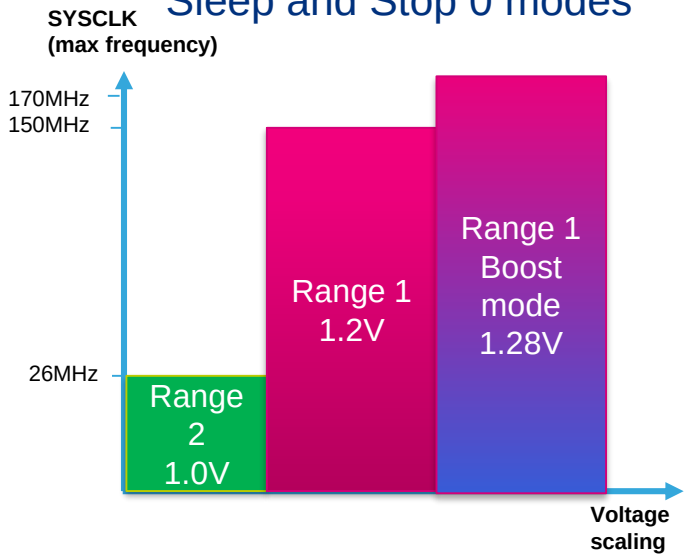
- Brown-out reset is always enabled in all modes except Shutdown mode
  - Ensure reset as soon as MCU drops below selected threshold, regardless of the VDD slope.
  - 5 thresholds selected by option byte **BOR_LEV[2:0],** from V_{BOR0} = 1.7 V to V_{BOR4} = 2.8 V.

- Power voltage detector active in all modes except Standby and Shutdown
  - 7 thresholds + external pin, selectable by software

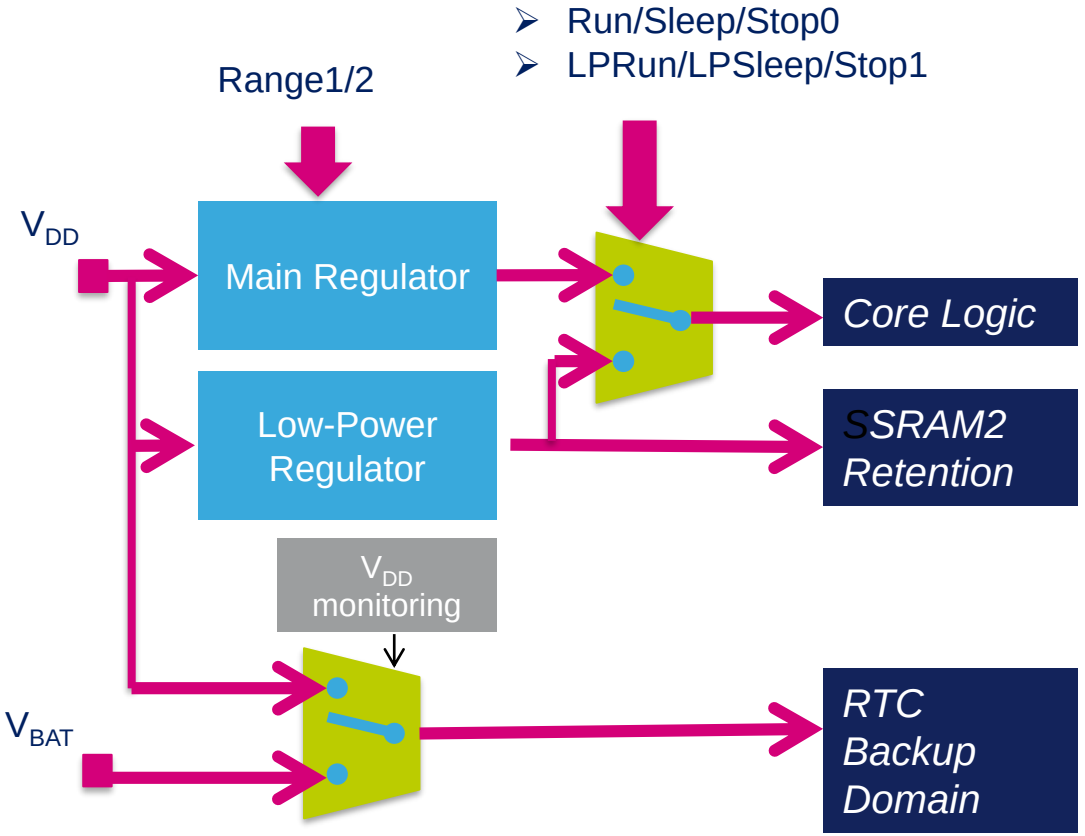
- Peripheral Voltage Monitor PVM
  - 2 PVM thresholds to monitor the VDDA min voltage for analog peripherals (COMP/DAC/OPAMP/VREFBUF)

Voltage regulators

- Two Voltage Regulators
  - One Main regulator with two voltage ranges for Dynamic Voltage Scaling; used in Run, Sleep and Stop 0 modes



  - One Low-power regulator for Low-power run, Low-power sleep and Stop 1 modes as well as for RAM retention in Standby

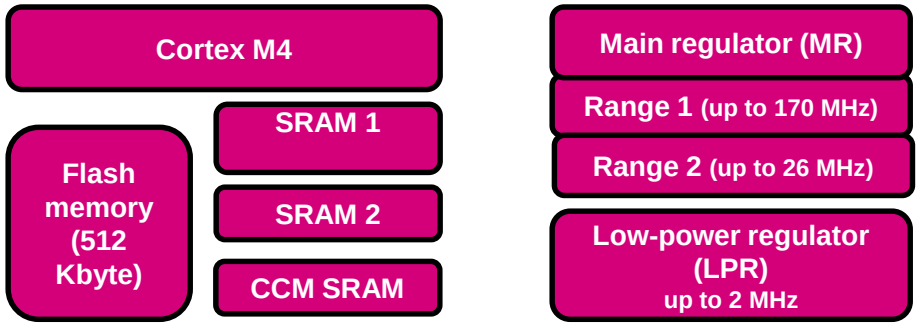


Run mode: Range 1

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- UCPD
- USB device
- USART
- LPUART
- I2C
- SPI
- CAN
- SAI
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- IWDG
- WWDG
- Systick Timer
- RNG
- AES
- CRC

Ex: Execution from Flash memory



Available clocks

- HSI16
- HSE
- LSI
- LSE

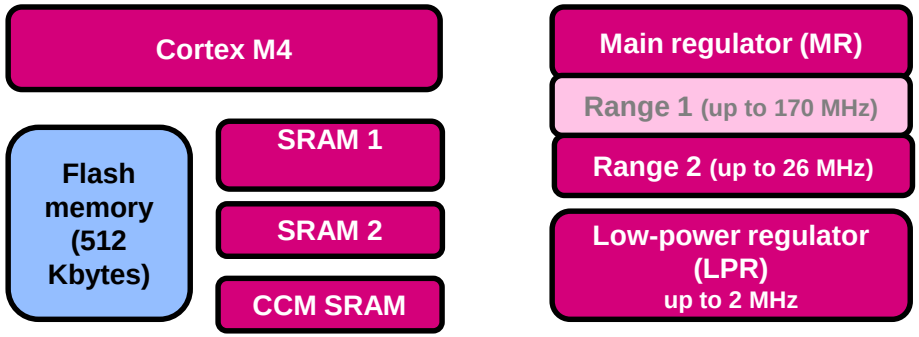
Active cell | Clocked-off cell | Cell in power-down | Available Periph and clock

Run mode: Range 2

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- UCPD
- USB device
- USART
- LP UART
- I2C
- SPI
- CAN
- SAI
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- IWDG
- WWDG
- Systick Timer
- RNG
- AES
- CRC

Ex: Execution from SRAM



Available clocks

- HSI16
- HSE
- LSI
- LSE

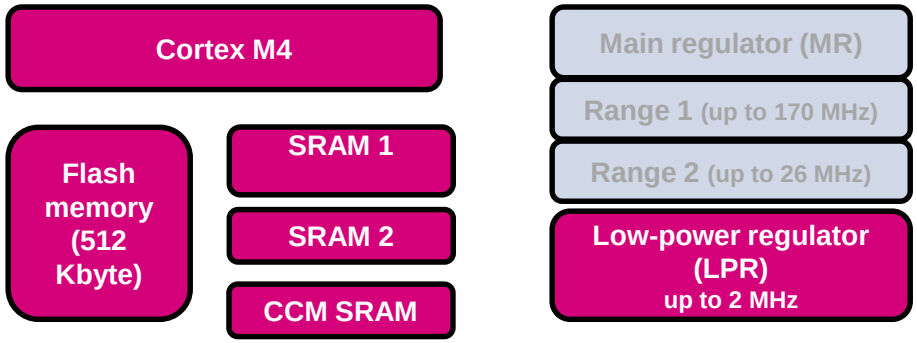
Active cell | Clocked-off cell | Cell in power-down | Available Periph and clock

Low-power run mode

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- UCPD
- USB device
- USART
- LP UART
- I2C
- SPI
- CAN
- SAI
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- IWDG
- WWDG
- Systick Timer
- RNG
- AES
- CRC

Ex: Execution from Flash memory



Available clocks

- HSI16
- HSE
- LSI
- LSE

Active cell | Clocked-off cell | Cell in power-down | Available Periph and clock

Run and Low-power run modes

- Each peripheral clock can be configured to be ON or OFF
  - After reset, all peripheral clocks are OFF, except Flash interface clock
  - SRAM1, SRAM2 and CCM SRAM clocks always ON in Run mode
- When running from SRAM1 or SRAM2 or CCM SRAM (in Run or Low-power run):
  - Flash can be put in Power-down mode
  - Flash clock can be switched off

Sleep mode: Range 1

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- UCPD
- USB device
- USART
- LP UART
- I2C
- SPI
- CAN
- SDMMC
- SAI
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- IWDG
- WWDG
- Systick Timer
- RNG
- AES
- CRC

Ex: Flash memory ON

Zzz

Cortex M4

Flash memory (1512 Kbyte)

SRAM 1

SRAM 2

CCM SRAM

Main regulator (MR)

Range 1 (up to 170 MHz)

Range 2 (up to 26 MHz)

Low Power regulator (LPR) up to 2 MHz

Available clocks

- HSI16
- HSE
- LSI
- LSE

Active cell

Clocked-off cell

Cell in power-down

Available Periph and clock

Low-power sleep mode

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- UCPD
- USB device
- USART
- LP UART
- I2C
- SPI
- CAN
- SDMMC
- SAI
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- IWDG
- WWDG
- Systick Timer
- RNG
- AES
- CRC

Ex: Flash memory OFF

Zzz

Cortex M4

Flash memory (512K byte)

SRAM 1

SRAM 2

CCM SRAM

Main regulator (MR)

Range 1 (up to 170 MHz)

Range 2 (up to 26 MHz)

Low Power regulator (LPR) up to 2 MHz

Available clocks

- HSI16
- HSE
- LSI
- LSE

Active cell

Clocked-off cell

Cell in power-down

Available Periph and clock

Stop modes

Lowest power modes with full retention

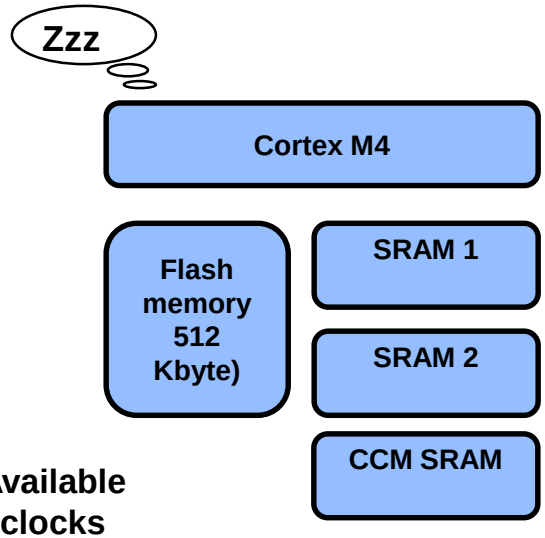
- SRAM1, SRAM2 and CCM SRAM and all peripheral registers retention
- All high-speed clocks are stopped
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop modes
- System clock at wakeup is the **HSI16**

Stop1 mode

Available peripherals

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- UCPD
- USB device
- USART
- LP UART
- I2C
- SPI
- CAN
- SAI
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- IWDG
- WWDG
- Systick Timer
- RNG
- AES
- CRC

I/Os kept, and configurable



Available clocks

- HSI16
- HSE
- LSI
- LSE

- Main regulator (MR)
  - Range 1 (up to 170 MHz)
  - Range 2 (up to 26 MHz)
- Low Power regulator (LPR) up to 2 MHz
- Backup domain
  - Backup Register (32x32 bits)
  - RTC

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- USB device
- USART
- LP UART
- I2C
- COMP
- LPTIM 1
- IWDG
- GPIOs

Active cell | Clocked-off cell | Cell in power-down | Available cell

Standby mode

Lowest power mode with SRAM2 retention, switch to VBAT and I/O control

- By default: no SRAM2 nor registers retention (voltage regulators in power down). **128-byte backup registers** always retained.
- Possibility to **retain SRAM2 16 Kbytes.**
- Ultra Low Power **BOR** always ON: safe reset regardless of VDD slope.
- Configurable **pull-up** or **pull-down** or none for each I/O

  PWR_PUCRx / PWR_PDCRx registers (x = A,B,…H), applied when **APC** is set in PWR_CR3 register

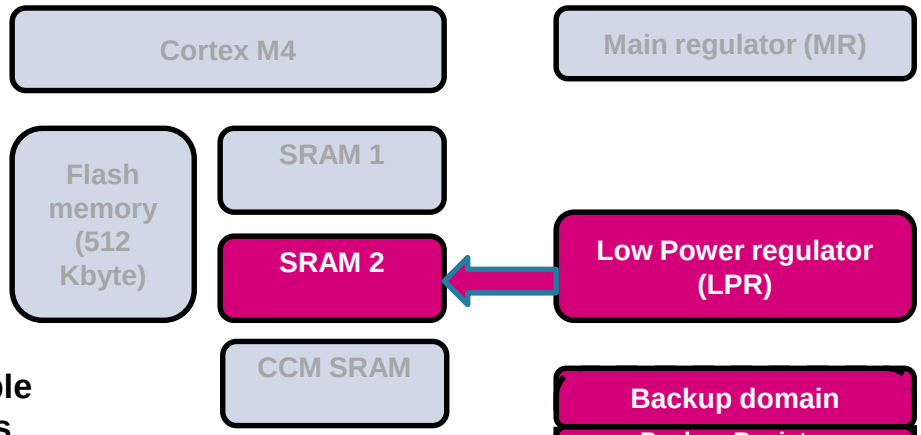
  => **Allows to control external component inputs state**
- **5 wakeup pins**: the polarity of each of the **5** wakeup pins is configurable
- Wakeup clock is **HSI16 at 16MHz**.

Standby mode with SRAM2

Available peripherals

GPIO
DMA
FSMC
OSPI
BOR
PVD, PVM
UCPD
USB OTG
USART
LP UART
I2C
SPI
CAN
SAI
ADC
DAC
OPAMP
COMP
Temp Sensor
Timers
LPTIM 1
IWDG
WWDG
Systick Timer
RNG
AES
CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down



Wake-up event

NRST
BOR
RTC + Tamper
IWDG
5 WKUP pins

Available clocks

HSI16
HSE
LSI
LSE

Active cell | **Clocked-off cell** | Cell in power-down | **Available cell**

Standby mode

Available peripherals

GPIO
DMA
FSMC
OSPI
BOR
PVD, PVM
UCPD
USB device
USART
LP UART
I2C
SPI
CAN
SAI
ADC
DAC
OPAMP
COMP
Temp Sensor
Timers
LPTIM 1
IWDG
WWDG
Systick Timer
RNG
AES
CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down

Cortex M4

Main regulator (MR)

Flash memory (1 Mbyte)

SRAM 1

SRAM 2

CCM SRAM

Low Power regulator (LPR)

Wake-up event

NRST
BOR
RTC + Tamper
IWDG
5 WKUP pins

Available clocks

HSI16
HSE
LSI
LSE

Backup domain
Backup Register (32x32 bits)
RTC

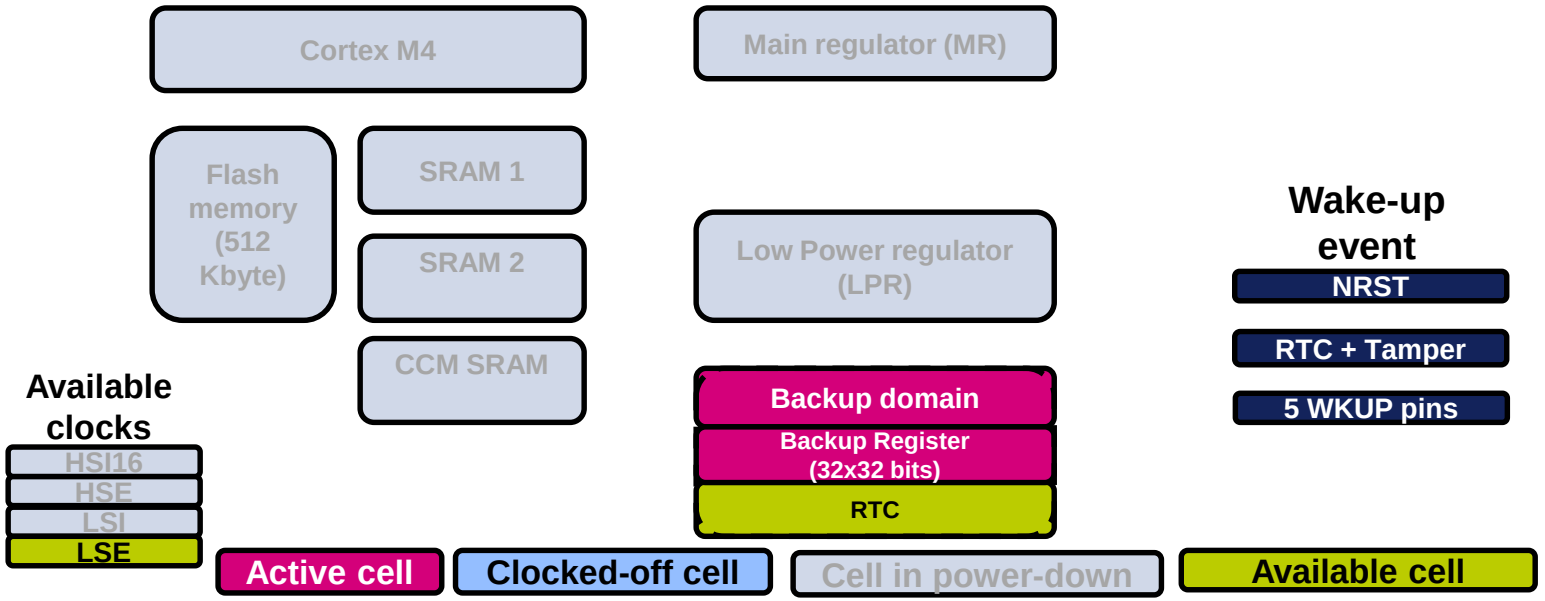
Active cell | Clocked-off cell | Cell in power-down | Available cell

Shutdown mode

Available peripherals

- GPIO
- DMA
- FSMC
- OSPI
- BOR
- PVD, PVM
- UCPD
- USB device
- USART
- LP UART
- I2C
- SPI
- CAN
- SAI
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- IWDG
- WWDG
- Systick Timer
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down
But floating when exit from Shutdown

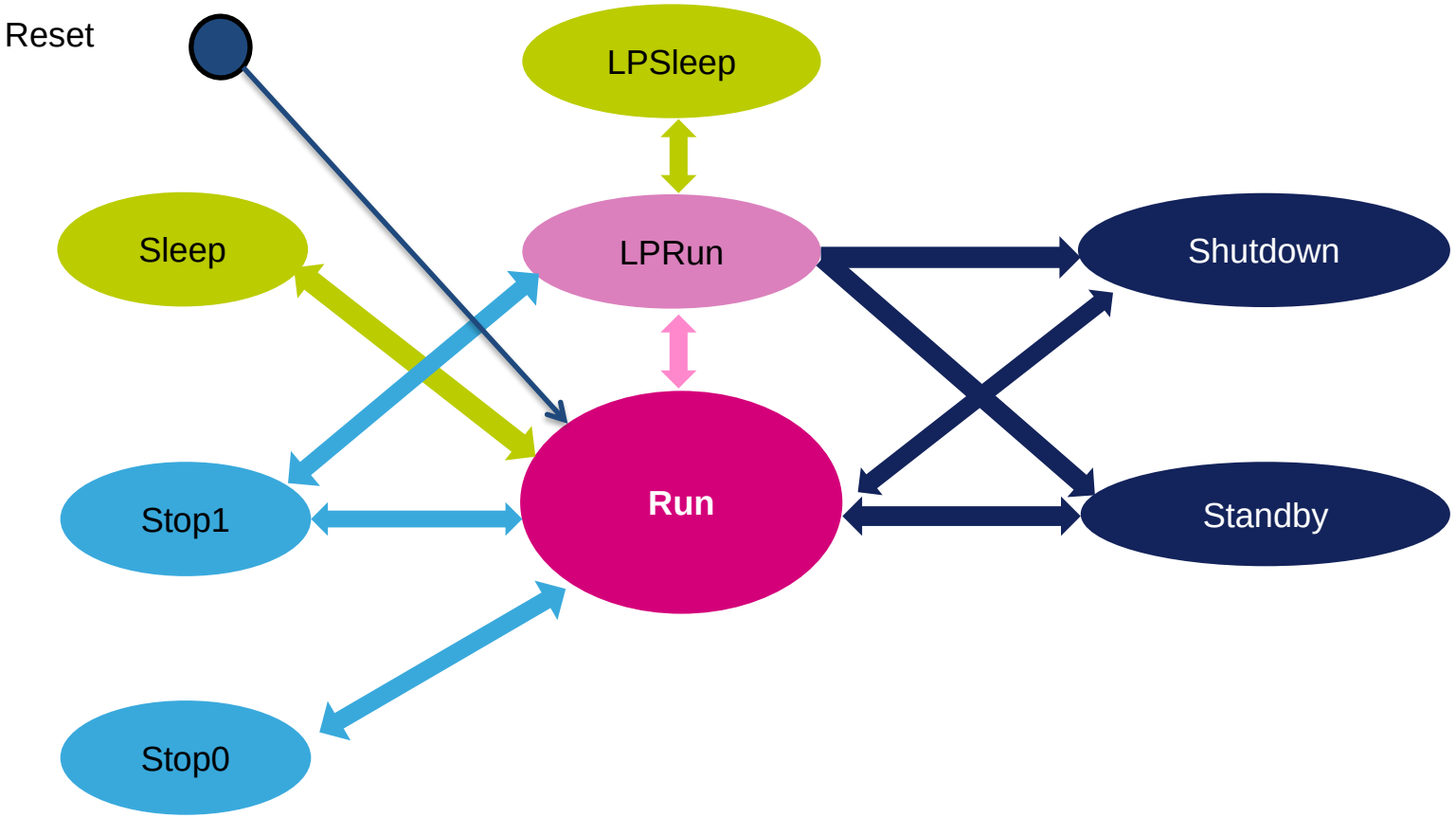


Low-power modes summary

Mode	Regulator	CPU	Flash	SRAM	Clocks	Peripherals
Run	R1	**Yes**	**ON**(1)	**ON**	Any	All
	R2					All except USB, RNG
LPRun	LPR	**Yes**	**ON**(1)	**ON**	Any except PLL	All except USB, RNG
Sleep	R1	No	**ON**(1)	**ON**(2)	Any	All Any IT or event
	R2					
LPSleep	LPR	No	**ON**(1)	**ON**(2)	Any except PLL	All except USB, RNG Any IT or event
Stop1	LPR (or MR)	No	OFF	**ON**	LSE/LSI	Reset pin, all I/Os BOR,PVD,PVM,RTC,IWDG, COMPx,DACx,OPAMPx,USARTx, LPUART,I2Cx,LPTIM1,USB
Standby	LPR	DOWN	OFF	**SRAM2 ON**	LSE/LSI	Reset pin, 5 WKUPx pins BOR, RTC, IWDG
	OFF			DOWN		
Shutdown	OFF	DOWN	OFF	DOWN	LSE	Reset pin, 5 WKUPx pins RTC

1. Can be put in power-down and clock can be gated off
2. SRAM1, SRAM2 and CCM SRAM can be gated off independently

Low-power modes transitions



VBAT backup domain

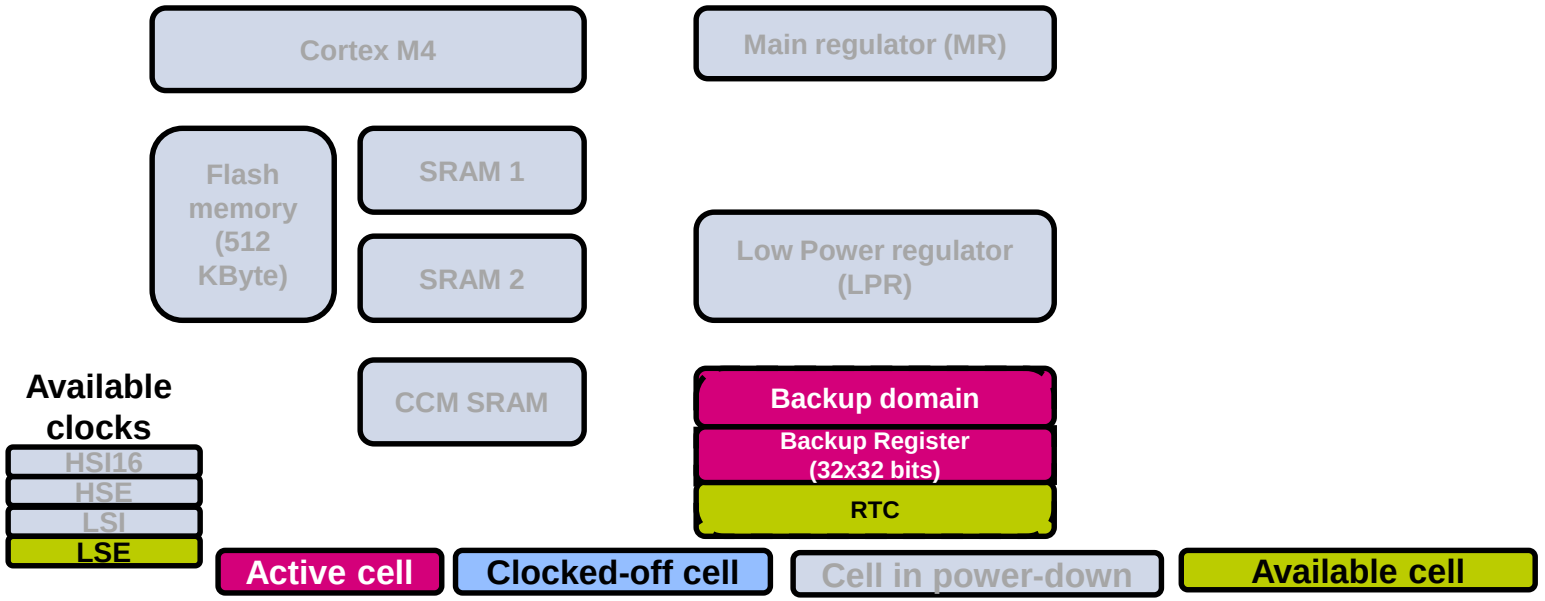
RTC still running and backup registers preserved in case of V_{DD} loss

- Backup domain contains:
  - RTC clocked by 32.768 kHz LSE oscillator, including **3 tamper pins**
  - **128 bytes backup registers**
  - RCC_BDCR register
- Automatic internal switch between V_{BAT} and V_{DD} when V_{DD} is powered down and powered on
- Internal connection to ADC for voltage monitoring ($V_{BAT}/3$)

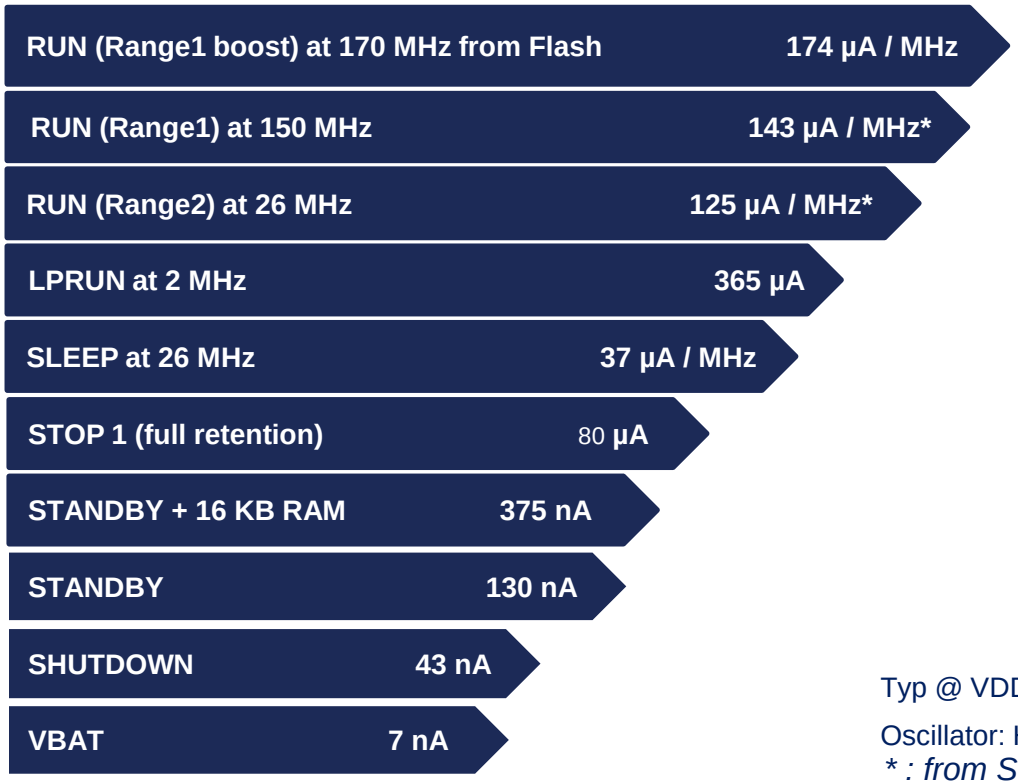
VBAT mode

Available peripherals

- GPIO
- DMA
- FSMC
- OSPI
- BOR
- PVD, PVM
- UCPD
- USB device
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SAI
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- IWDG
- WWDG
- Systick Timer
- RNG
- AES
- CRC



Some preliminary consumption figures (G474)



Typ @ VDD = 1.8V @ 25 °C

Oscillator: HSE Bypass for LPRUN

** : from SRAM1*

Option bytes

- 3 option bits can be configured in Flash options bytes to prohibit a given low-power mode:
  - nRST_SHDWN: When cleared, a Reset is generated when entering Shutdown mode
  - nRST_STDBY: When cleared, a Reset is generated when entering Standby mode
  - nRST_STOP: When cleared, a Reset is generated when entering Stop modes

Debug information

- 3 bits in DBGMCU_CR register allows to debug in Sleep, Stop, Standby and Shutdown modes:
  - DBG_STANDBY: When set, the digital part is not unpowered in Standby and Shutdown modes, and HCLK and FCLK remain ON, provided by internal RC. In addition, the MCU in under system reset during Standby/Shutdown.
  - DBG_STOP: When set, HCLK and FCLK remain ON in Stop modes, provided by internal RC.
  - DBG_SLEEP: When set, HCLK and FCLK remain ON in Sleep and Low-power sleep modes.
- When those bits are set, the connection with debugger is kept during the low-power mode. After wakeup, the debug is still possible.

STM32G4 - RCC

Reset and clock controller

life.augmented

Overview

- The STM32G4 reset and clock controller manages system and peripheral clocks
  - 3 internal oscillators
  - 2 external oscillators (crystal or resonator)
  - One PLL
  - Many peripherals have independent clocks
- The RCC manages the various system and peripheral resets.

Application benefits

- High flexibility in choice of clock sources to meet consumption and accuracy requirements.
- Many independent peripheral clocks allow for adjusting power consumption without impacting communication baud rates, and to keep some peripherals active in low-power modes.
- Safe and flexible reset management

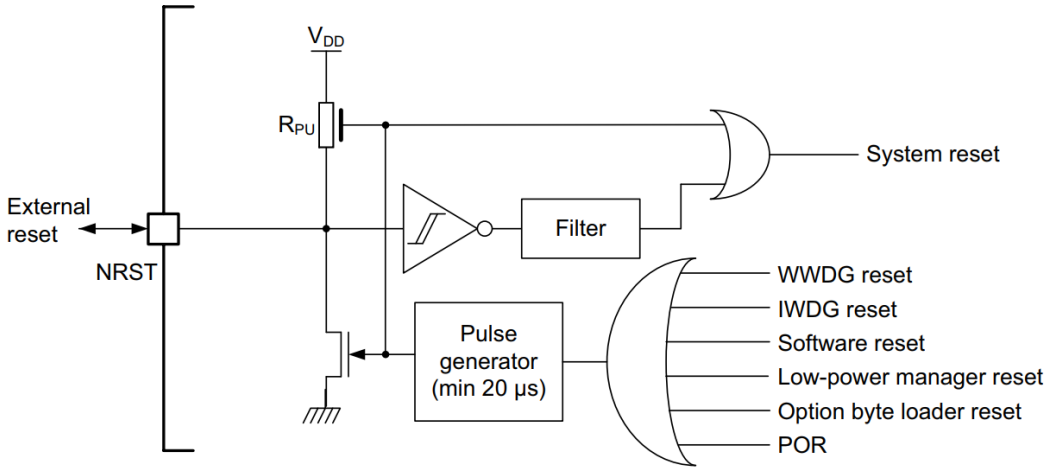
Reset key features

Safe and flexible reset management without external components

- Manages three types of reset:
  - System reset
  - Power reset
  - Backup domain reset
- Peripherals have individual reset control bits

Reset sources

- System reset
  - Resets all registers except the reset flags in the RCC_CSR register, PWR registers, and the Backup domain
  - Reset sources
    - Low level on the NRST pin (external reset)
    - WWDG event
    - IWDG event
    - A software reset (through NVIC)
    - Low-power-mode security reset
    - Option byte loader reset
    - Brown-out reset



Reset sources

- NRST Pin new design => PG10-NRST
  - The configuration of the Reset circuitry is done through the option bytes NRST_MODE[1:0] and IRHEN (Internal reset holder option bit)

Mode	Configuration		Behavior
	NRST_MODE	IRHEN	
Input/Output (Legacy)	11	0	20 us Output pulse generated on NRST pin in case of Internal Reset
		1	Output pulse maintained until NRST voltage reach Vil threshold (~0.3VDD)
Input only	01	x	Internal Reset are not propagated outside of the part (PU always ON)
GPIO	10	x	PG10 only, No Reset Pin

Reset sources

- Power reset
  - Sources
    - Power-on reset (POR) or Brown-out reset (BOR) => resets all registers except those in the Backup domain
    - Exit from Standby => resets all registers in VCORE domain
      - Registers outside the VCORE domain (RTC, WKUP, IWDG, and Standby/Shutdown mode control) are not impacted.
    - Exit from Shutdown generates a BOR reset.
- Backup domain reset
  - Resets Backup domain RTC registers, Backup registers, and the RCC BDCR register
  - Sources
    - Software reset triggered by setting BDRST bit in RCC BDCR register
    - VDD or VBAT power on, if both supplies have previously been powered off

Clock key features

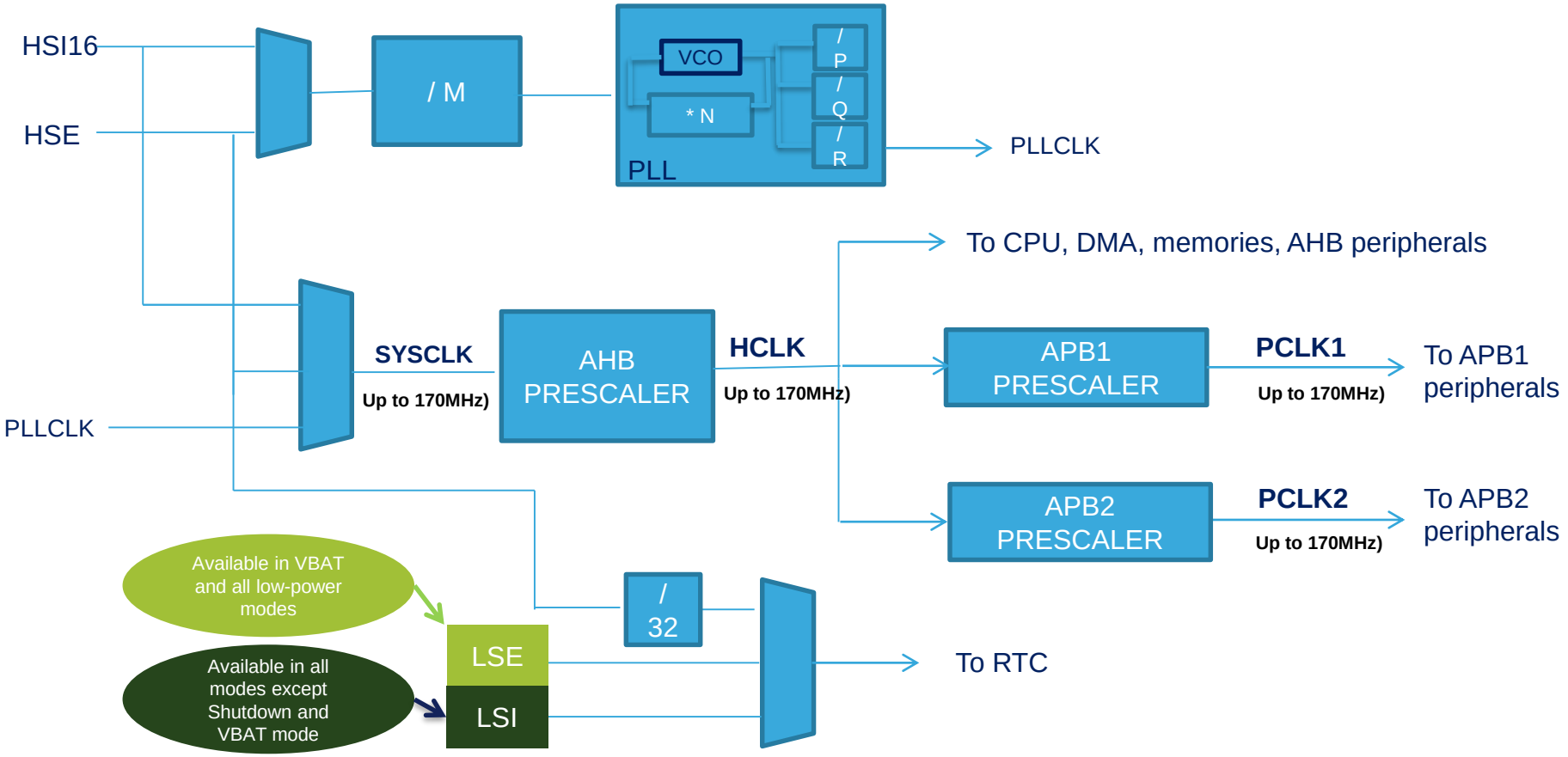
- **Choice of clock sources for low-power, accuracy, and performance**

- Three internal clock sources
  - High-speed internal 16 MHz RC oscillator (HSI16)
  - High-speed internal 48 MHz RC oscillator (HSI48)
  - Low-speed internal 32 kHz RC oscillator (LSI)
- Two external oscillators
  - High-speed external 4 to 48 MHz oscillator (HSE) with clock security system
  - Low-speed external 32.768 kHz oscillator (LSE) with clock security system
- One PLL, with three independent outputs

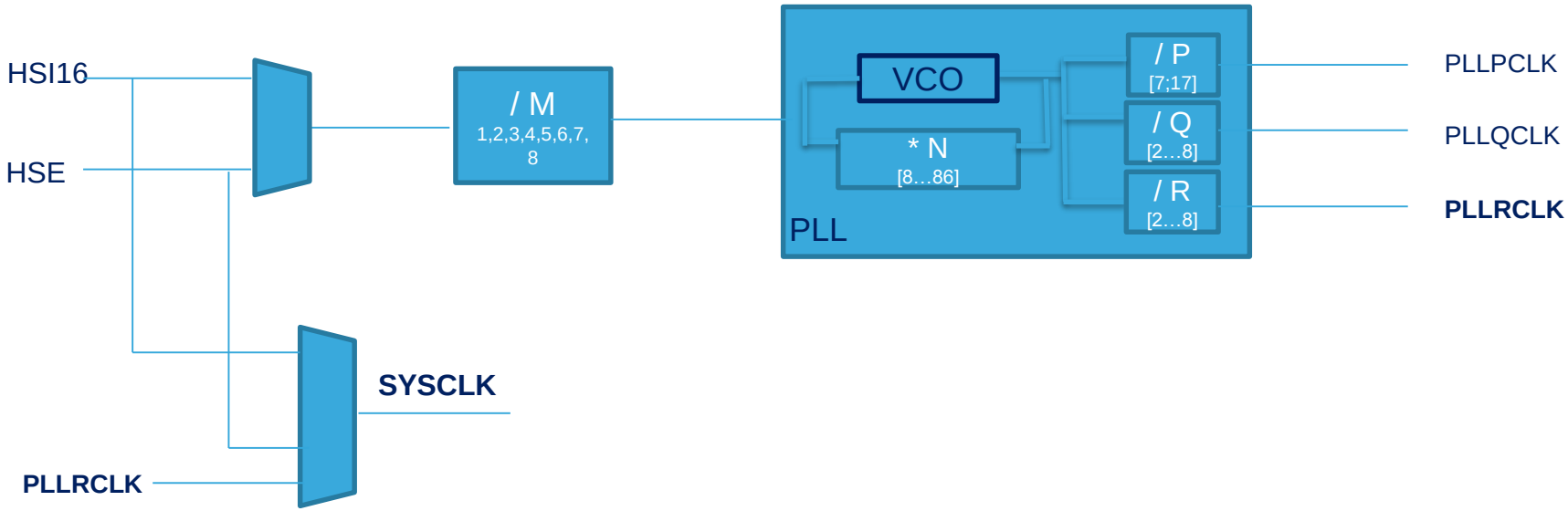
Clock key features

	STM32F3	STM32G4
Internal clock sources	High-speed internal 16 MHz RC oscillator (HSI16)	
	Low-speed internal 40 kHz RC oscillator (LSI)	Low-speed internal 32 kHz RC oscillator (LSI)
	NA	High-speed internal 48 MHz RC oscillator (HSI48)
External clock sources	High-speed external 4 to 32 MHz oscillator (HSE) with clock security system	High-speed external 4 to 48 MHz oscillator (HSE) with clock security system
	Low-speed external 32.768 kHz oscillator (LSE) with clock security system	
PLL	One PLL with a single output	One PLL with three independent outputs

Simplified clock tree



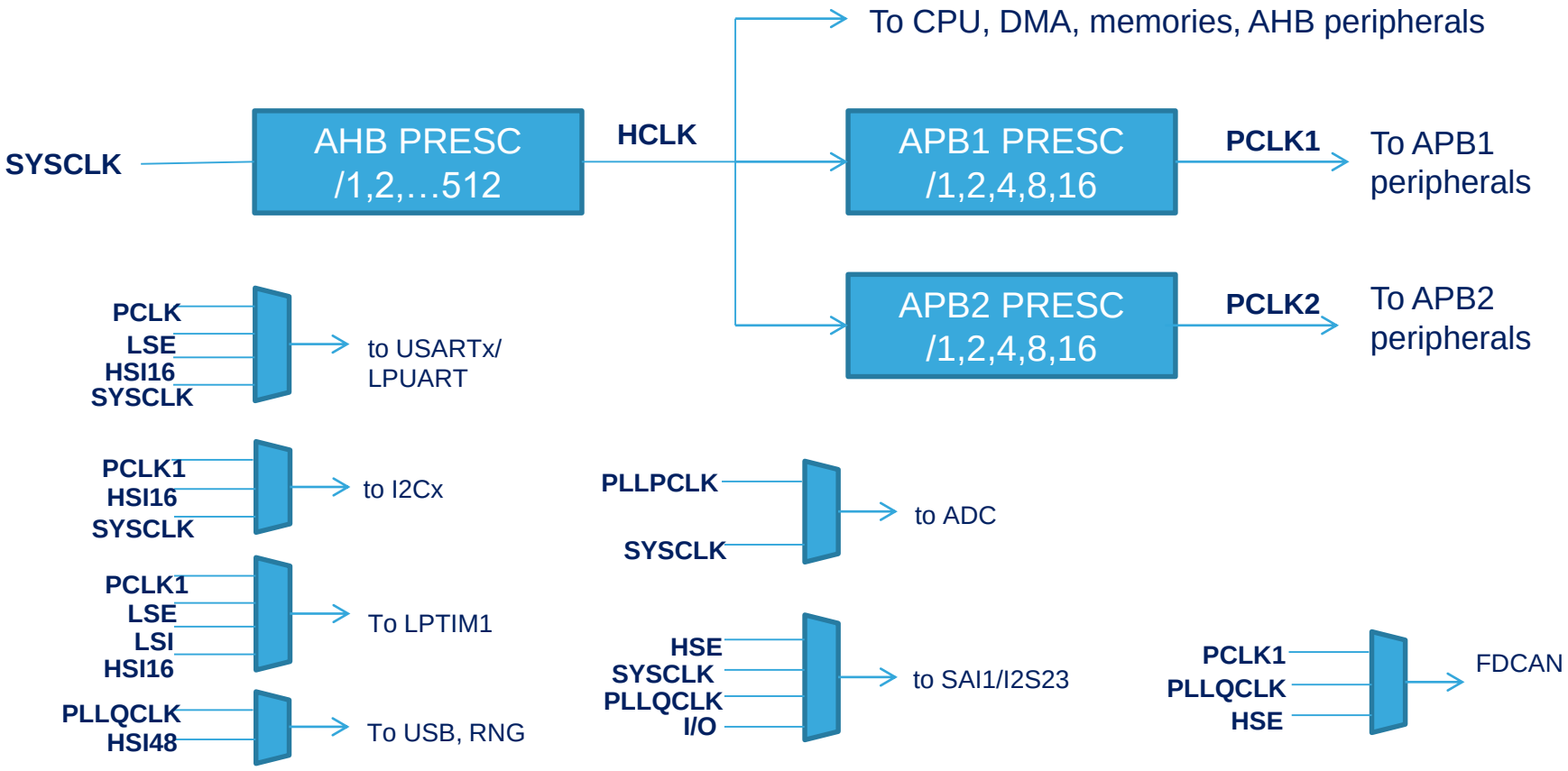
PLL clock


HSI16
HSE
/ M
1,2,3,4,5,6,7,
8
VCO
* N
[8…86]
/ P
[7;17]
/ Q
[2…8]
/ R
[2…8]
PLL
PLLPCLK
PLLQCLK
PLLRCLK
SYSCLK
PLLRCLK

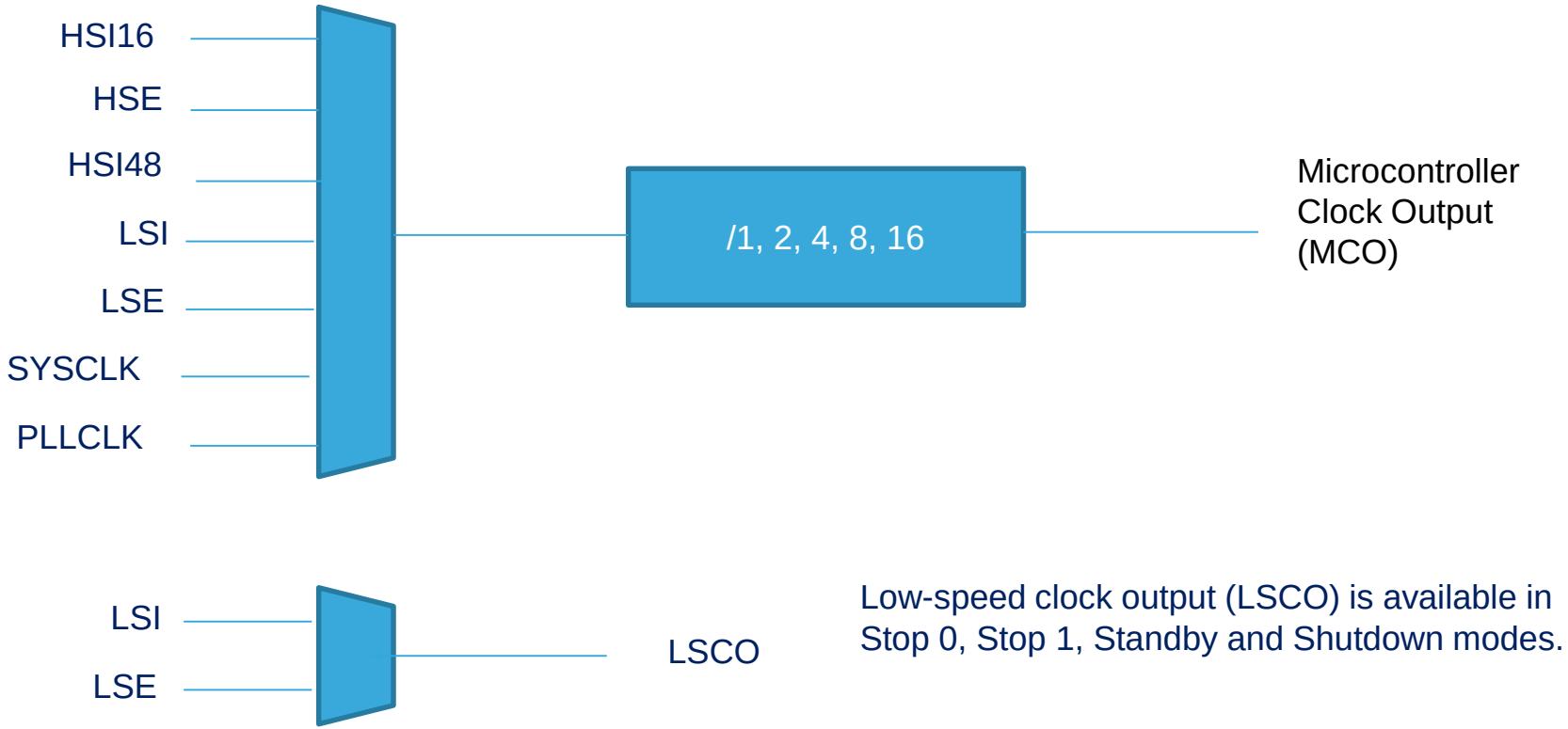
System Clock Selection

- Switching from Low to High speed or from High to Low speed system clock, it is recommended to use a transition state with a medium speed clock for at least 1us.
- Clock source switching conditions:
  - Switching from HSE or HSI to PLL with AHB frequency (HCLK) higher than 80MHz.
  - Switching from PLL with HCLK higher than 80MHz to HSE or HSI.
- Transition state:
  - Set the AHB prescaler HPRE[3:0] bits to divide System frequency by 2
  - Switch system clock to PLL
  - Reconfigure AHB prescaler bits to needed HCLK frequency

Clock tree

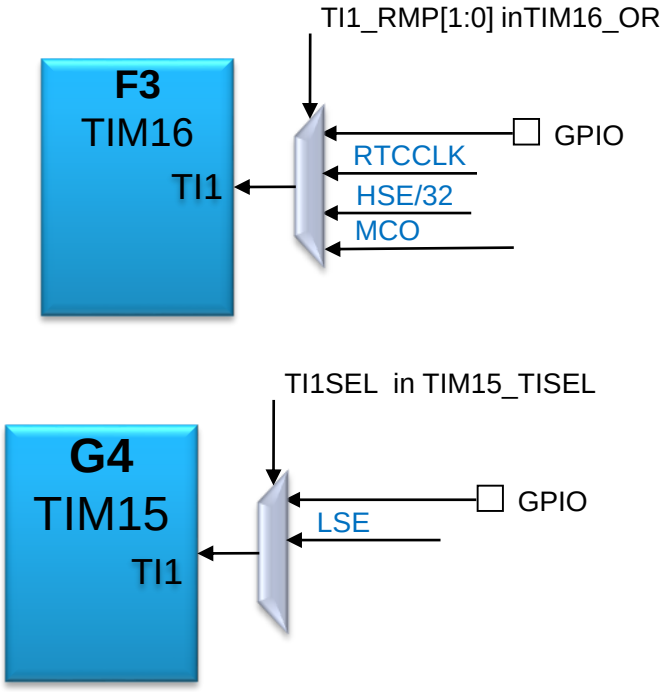

To CPU, DMA, memories, AHB peripherals
SYSCLK
AHB PRESC
/1,2,…512
HCLK
APB1 PRESC
/1,2,4,8,16
PCLK1
To APB1
peripherals
APB2 PRESC
/1,2,4,8,16
PCLK2
To APB2
peripherals
PCLK
LSE
HSI16
SYSCLK
to USARTx/
LPUART
PCLK1
HSI16
SYSCLK
to I2Cx
PLLPCLK
SYSCLK
to ADC
PCLK1
LSE
LSI
HSI16
To LPTIM1
HSE
SYSCLK
PLLQCLK
I/O
to SAI1/I2S23
PCLK1
PLLQCLK
HSE
FDCAN
PLLQCLK
HSI48
To USB, RNG

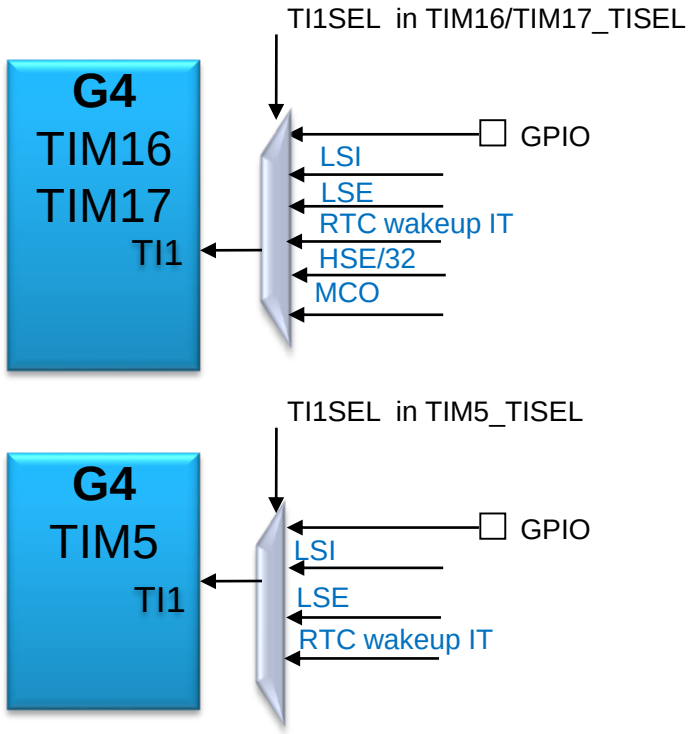
Clock-out capability



Low-speed clock output (LSCO) is available in Stop 0, Stop 1, Standby and Shutdown modes.

Internal/external clock measurement with Timers





Clock gating

- **Dynamic consumption optimization in (LP)Run and (LP)Sleep modes**

- Peripheral clock enable registers
  - Peripherals clocks disabled by default (except Flash)
  - Registers read and write access not supported when clock is disabled.
  - Caution: SRAM1/SRAM2/CCM SRAM do not have enable bit (always enabled in Run/LPRun modes)

- Peripheral clock enable registers in Sleep and Stop modes
  - Enables or disables the peripheral clocks in Sleep, LPSleep, Stop 0/1 modes
    - No effect if corresponding peripheral clock enable is cleared
    - Affects Sleep and Stop modes (for peripheral with independent clock active in Stop mode)
  - Caution: SRAM1/SRAM2/CCM SRAM clocks are enabled by default in Sleep/LPSleep modes

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