STM32G4 Technique Training

- ADC
- DAC
- OPAMP
- VREFBUF
- COMP

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STM32 G4 - Analog peripherals improved

New design

Op-Amp	F3 (today)	L4 (today)	Target G4	Comment
Power supply (V)	2.4 .. 3.6	1.8 .. 3.6	1.8 .. 3.6 @ functional 2.7..3.6 @ full perf.	
GBW (MHz)	8.2	1.6	**13 MHz**	
Slew rate (V/µs)	4.7	0.7	**15 V/µs** (min) coupled with ADC	
Offset (full temp range) (mV)	3	3	3	1.5mV = design target
	Rail to rail input/output	Rail to rail input/output	Rail to rail input/output	
Gain	x 2, x4, x8, x 16		x 2, x4, x8, x 16, x32, x64, x-1,…, x-15	1% accuracy (2% for x 32, x64)

New design

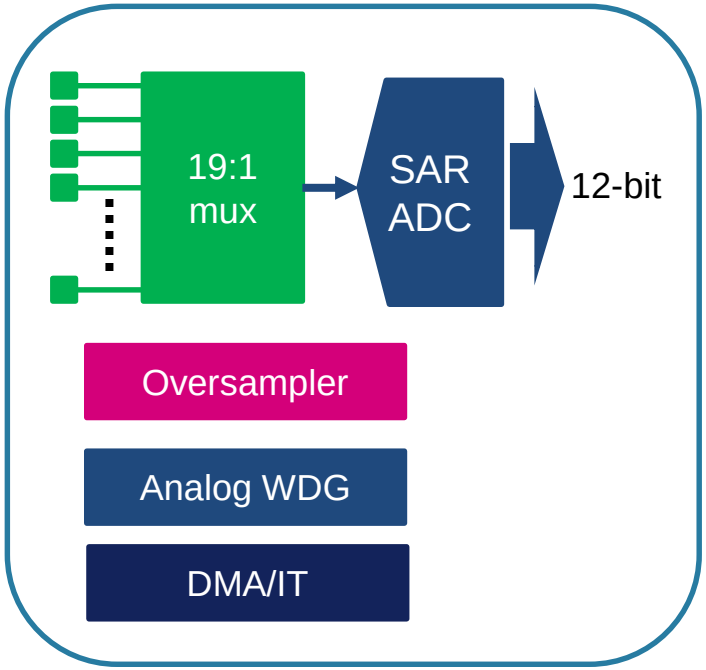
Comparator	F3 (today)	L4 (today)	Target G4	Comment
Power supply (V)	1.8 .. 3.6	1.8 .. 3.6	1.8 .. 3.6 @ functional 2.7..3.6 @ full perf.	
Propagation delay	25ns	50ns	**16.7ns**	Very challenging
Offset (mV)	4	5	4	3mV = design target
Hyteresis	No (except 256, 128KB version)		25mV	Step programmable (25mV target)

New concept

DAC	F3 (today)	L4 (today)	Target G4	Comment
Power supply (V)	2.4 .. 3.6	1.8 .. 3.6	1.8 .. 3.6 @ functional 2.7..3.6 @ full perf.	
Sampling rate	1MSps	1MSps	**15MSps** (internal use only → DAC connected to COMP input)	13Msps usefull for slope compensation

STM32G4 - ADC

Overview



- Provides analog-to-digital conversion
  - Five ADC instances with up to 42 input channels
  - 12-bit resolution, 16-bit with oversampling
  - 4 Msamples/s max. (12-bit)
  - Three analog watchdogs per ADC
  - DMA request generation
  - Interrupt generation

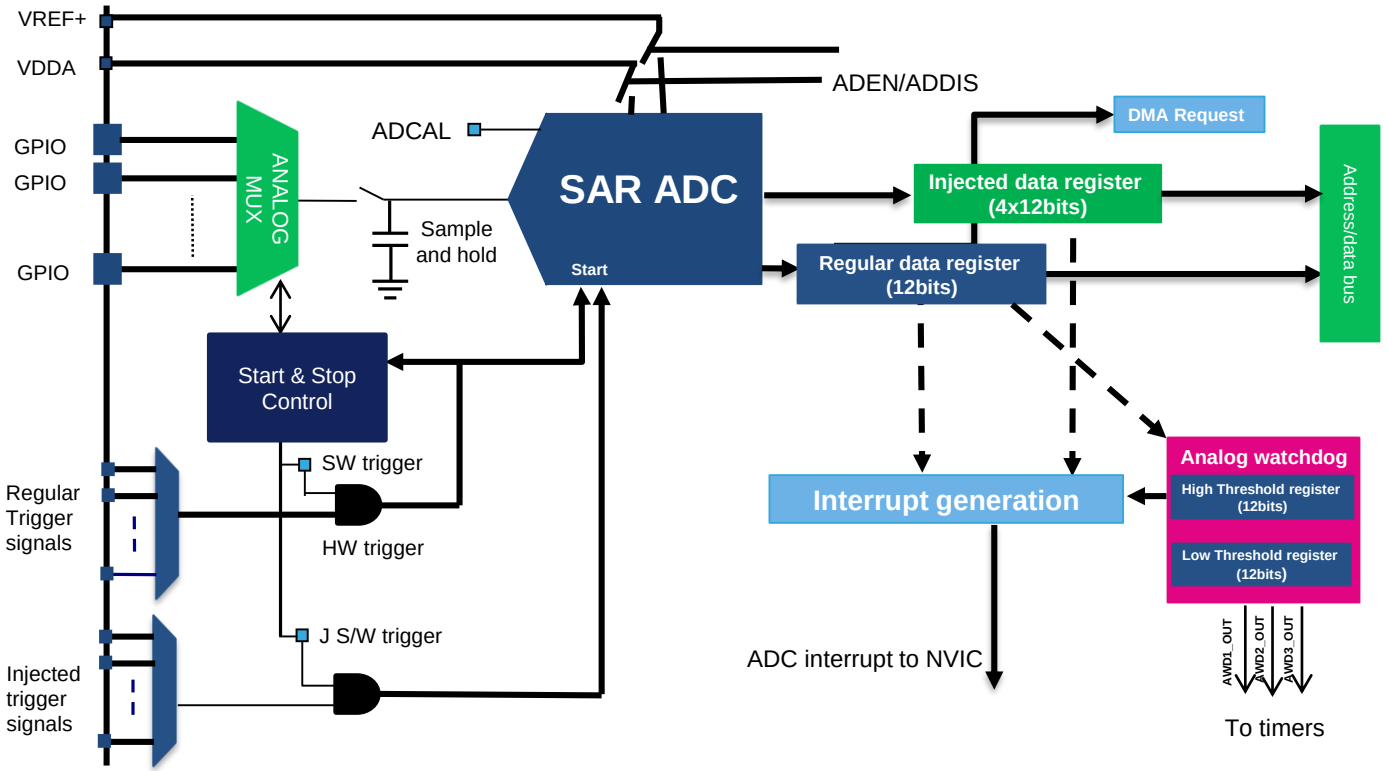
Application benefits

- Ultra-low power consumption
- Flexible trigger, data management to offload CPU

Key features

ADC units	5 modules
Input channel	42 external channels (GPIOs), single/differential (23 for G431)
Technology	12-bit successive approximation
Conversion time	250 nS, 4 Msamples/s (when f_{ADC_CLK} = 60 MHz)
Functional mode	Single, Continuous, Scan, Discontinuous, or Injected
Triggers	Software or external trigger (from Timers & IOs)
Special functions	Hardware oversampling, Analog watchdogs (+filter), Data preconditioning (Offset and Gain compensation), Flexible Sampling time
Data processing	Interrupt generation, DMA requests
Low-power modes	Deep power-down, auto delay, power consumption dependent on speed

Block diagram



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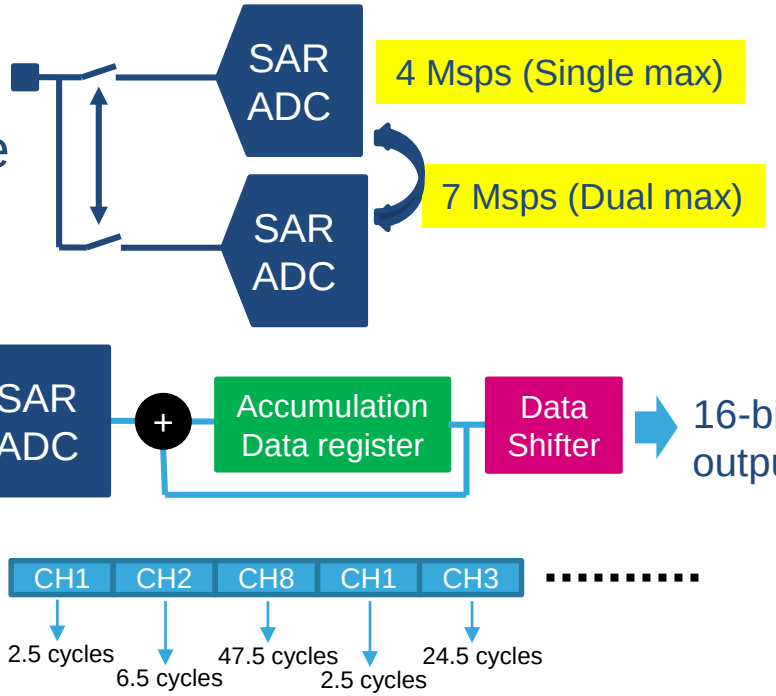
High performance features

- **Several high performance features are implemented**

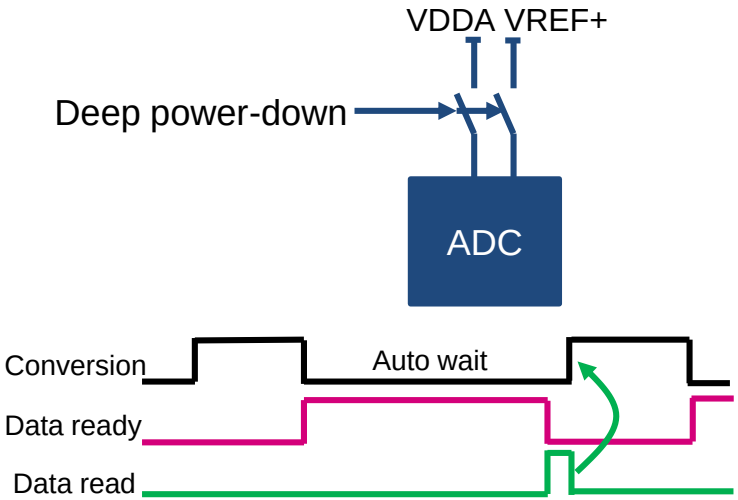
- 4 Msamples/s for 60 MHz ADC clock
- Up to 7 Msamples/s in interleaved mode
- Flexible sequencer (up to 16 channels)
- Hardware oversampling
- Flexible sampling time control
  - New: Bulb mode (quasi-continuous sampling)
    Timer controlled sampling duration
- Auto-calibration to reduce offset



Low-power features

- **Several low-power features are implemented**

- Deep power-down mode
  - Internal supply for ADC can be disabled by power switch for leakage current reduction
- Auto-delayed conversion
  - ADC can automatically wait until last data is read
- Power consumption depends on sampling rate



ADC conversion speeds

- **Conversion speed is resolution dependent**

- ADC needs minimum 2.5 ADC clock cycles for sample period and 12.5 ADC clock cycles for conversion (for 12-bit resolution)

- 60 MHz maximum ADC clock with 15 cycles results in maximum speed for a single ADC 4 Msamples/s

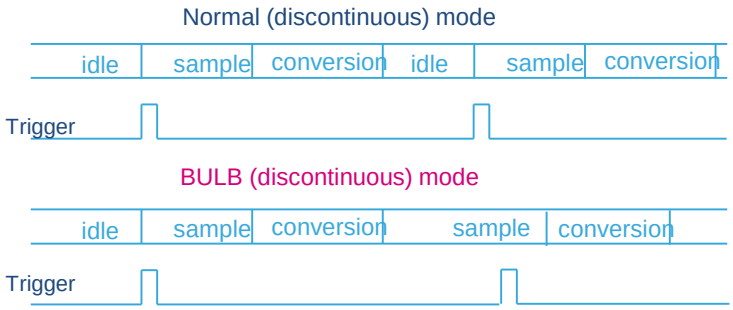
- Speed-up by lowering resolution
  - 10-bit : 10.5 cycles (+2.5) => 4.61 Msamples/s
  - 8-bit : 8.5 cycles (+2.5) => 5.45 Msamples/s
  - 6-bit : 6.5 cycles (+2.5) => 6.66 Msamples/s

Resolution	$t_{Conversion}$
12 bits	12.5 Cycles
10 bits	10.5 Cycles
8 bits	8.5 Cycles
6 bits	6.5 Cycles

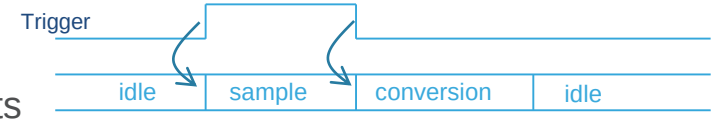
Sampling times

Flexible sampling time control

- Channel-wise programmable sampling time. Different sampling time available (2.5, 6.5, 12.5, 24.5, 47.5, 92.5, 247.5, 640.5 cycles)
- Flexible Sampling time
  - Bulb sampling mode
    - Available only in discontinuous mode
    - Sampling starts immediately after last conversion.
    - Less latency time from trigger to real sampling point
    - Useful with high impedance sources



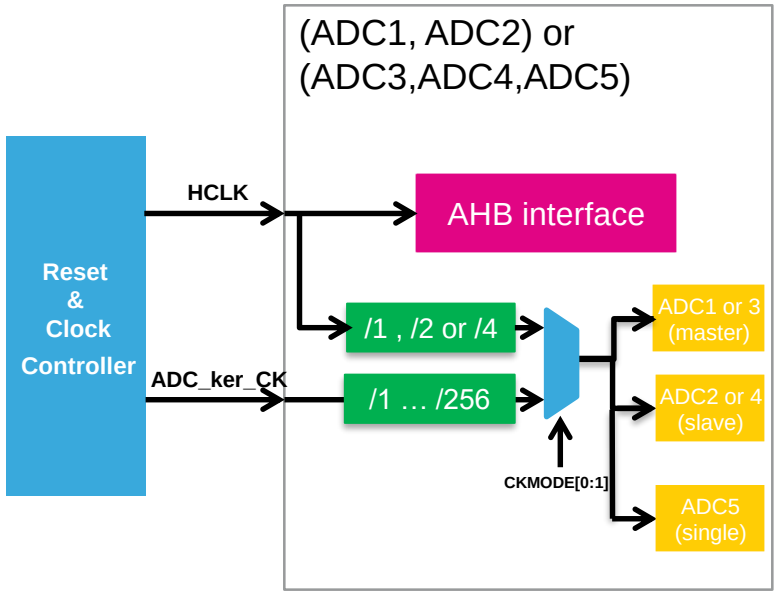
  - Sample time control trigger mode
    - Sampling time is fully controlled by trigger signal
    - Rising edge starts sampling
    - Falling edge stops sampling and the conversion starts



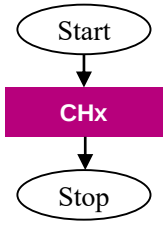
ADC clocks

Flexible clock selection

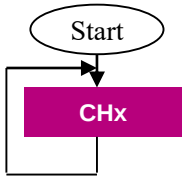
- ADC clock can be selected from
  1) AHB clock
     - If a trigger event depends on the AHB clock, latency between event and start of conversion is deterministic
     - Can be divided by 1, 2 or 4
  2) Independent ADC clock
     - Asynchronous to the system clock (AHB)
     - ADC can run full-speed even when CPU is running on slower frequency



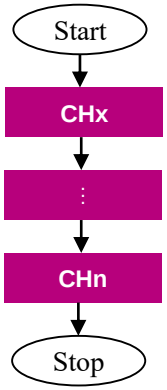
ADC conversion modes



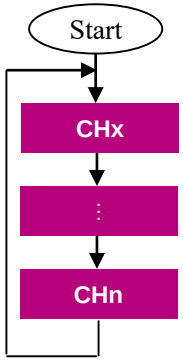
Single



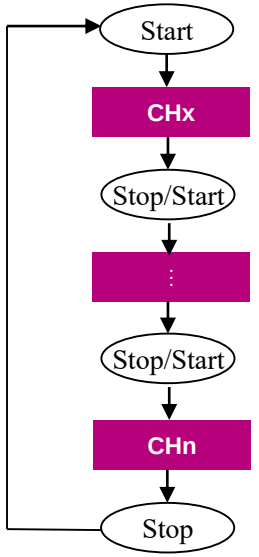
Single continuous



Scan: multi-channel



Scan: Continuous (multi-channel repeated)

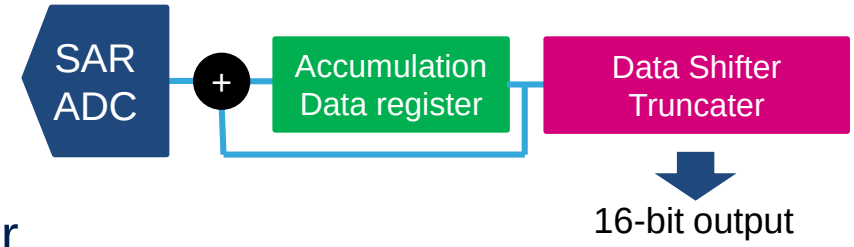


Discontinuous mode

Hardware oversampling

- **Data pre-processing to offload the CPU**

- Programmable oversampling ratios:
  x2, x4, x8, x16, x32, x64, x128, x256
- Programmable data shifter & truncater
  Right shift (division) of 0 to 8 bits
- Up to 16-bit ADC results
- Averaging, data rate reduction,
  SNR improvement and basic filtering



Oversampling ratio	Output resolution	Equivalent sampling frequency max
x4	13 bits	1.33 Msamples/s
x16	14 bits	333 ksamples/s
x64	15 bits	83 ksamples/s
x256	16 bits	20.8 ksamples/s

- Oversampling brings additional 1-bit when multiplying samples by 4

Gain Compensation

Improve ADC gain stability

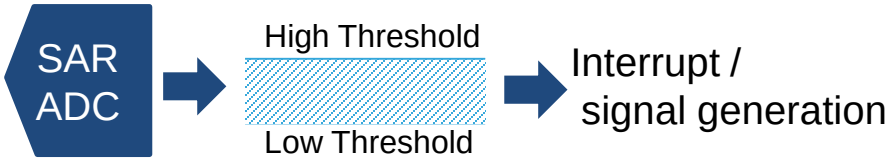
- Gain compensation
  - Improve the stability of the ADC gain by compensating for the reference voltage shift during operation.
  - Gain compensation is enabled by setting bit **ADCx_CFGR2.GCOMP**
  - It is applied on all converted data (all channels) after oversampling shift
  - Gain factor = (**ADC_GCOMP.GCOMPCOEFF[13:0]**)/4096
  - The gain factor can range from 0 to 3.999756.
  - After each conversion Data is computed with following formula
    - DATA = DATA(adc result) x (GCOMPCOEFF[13:0])/4096

Offset compensation

New Offset saturation control

- Offset compensation
  - Channel dependent offset compensation (up to 4 channels).
  - Channel selection set in **ADC_OFRy.OFFSETy_CH[4:0]**
  - Offset value is set by programming **ADC_OFRy.OFFSETy[11:0]**
  - Offset can be positive or negative (**ADC_OFRy.OFFSETPOS)**
  - Saturation control can be enabled by (**ADC_OFRy.SATEN**) to prevent overflow
    - Data will be unsigned and saturate at 0x000 for negative offset and at 0xFFF for positive offset
  - In case of signed data, sign is indicated by extended sign bit **SEXT** in **ADC_DR** and **ADCy_JDR**
  - Offset compensation is applied after gain compensation and data is calculated as follows
    - DATA = DATA(adc result) +/- OFFSETy[11:0]

Analog watchdog



More robust (glitch free) analog watchdog

- Each ADC has three analog watchdogs, which behave like window comparators
  - AWD1: 12-bit analog watchdog can monitor one selected channel or all enabled channels
  - AWD2 and AWD3: Two 8-bit analog watchdogs can monitor several selected channels
  - Continuously monitor an over- and/or under-threshold condition, then generates event
  - Analog watchdog threshold can be modified on the fly when conversion is ongoing
  - Comparison happens after gain and offset compensation
- Analog watchdog filter (only with AWD1)
  - Interrupt or signal generation only after programmable consecutive threshold detections **ADCx_TR1.AWDFILT**
  - DMA request is generated only when data is inside valid range.
- Update: Analog watchdog operates only in unsigned ADC output (SATEN bit set to 1)

Data transfers

Reduced software overhead

- Regular conversion data stored in a 16-bit data register ADCx_DR
  - Software polling, interrupts or DMA requests can be used to move data
- In Dual mode regular conversions data are stored in a 32-bit data register ADCx_CDR
- Injected conversion data stored in four dedicated 16-bit data registers
  - Regular data sequence can be kept even if injected conversion occurs

Injected conversions

Interruption during the ADC regular conversion

- ADC can accept injected triggers even if a regular conversion is running
  - Trigger stops regular conversion and starts injected conversion
  - Up to 4 injected conversions are available by a single trigger
  - Auto-resume occurs once the injected conversion finishes
  - Four dedicated 16-bit data registers are available for injected conversion results
  - Interrupt generation
  - Queue of injected conversion reprogrammable on-the-fly

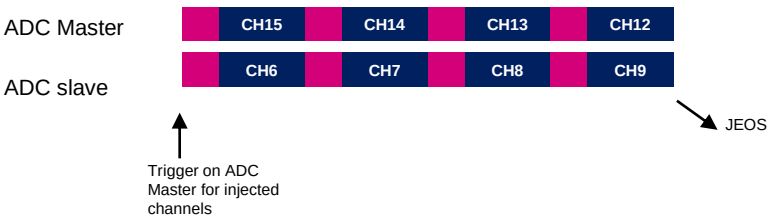
ADC Dual mode

Tightly coupled ADCs can work in Dual mode

- Dual mode implementation
  - ADC1 and ADC2 can operate in Dual mode (ADC1 is master)
  - ADC3 and ADC4 can operate in Dual mode (ADC3 is master)
  - ADC5 works in single mode
- Four possible modes:
  - Injected simultaneous mode
  - Regular simultaneous mode
  - Interleaved mode
  - Alternate trigger mode
- Dual combined modes
  - Injected simultaneous mode + Regular simultaneous mode
  - Regular simultaneous mode + Alternate trigger mode
  - Injected simultaneous mode + Interleaved mode

Injected simultaneous mode

- Converts an injected group of channels
- The external trigger source comes from the injected group multiplexer of the master ADC.
- JEOS event is generated at the end of all channels conversion.
- Results are stored on injected data registers ADCx_JDRy of each ADC.

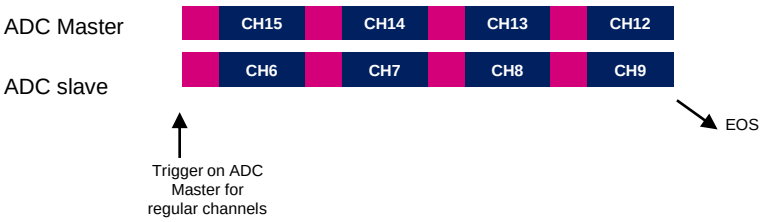


Note: Do not convert the same channel on the two ADCs.

- Conversion sequences must be equal on master and slave or must ensure that the interval between triggers is longer than both sequences.
- In discontinuous mode, every simultaneous conversion requires an injected trigger

Regular simultaneous mode

- Converts a regular group of channels
- The external trigger source comes from the regular group multiplexer of the master ADC.
- An EOS is generated at the end of all channels conversion.

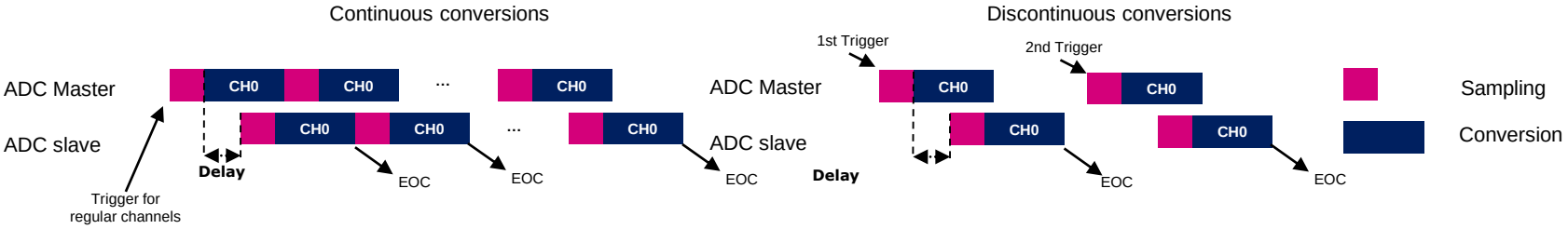


Note: Do not convert the same channel on the two ADCs.

- Results can be read by software after each EOC event.
- Or can be read by DMA:
  - Using 2 DMA channels reading from each ADCx_DR of Master and Slave
  - Using 1 DMA channel (of ADC Master) reading from common data register ADC_CDR (MDMA mode)

Interleaved mode

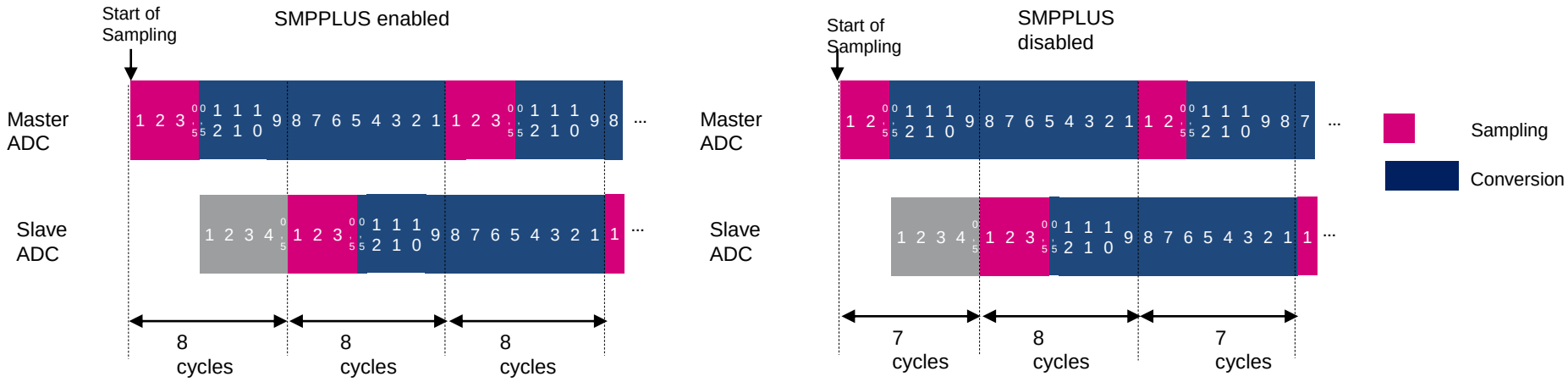
- Converts a regular channel group (usually one channel).
- The external trigger source which starts the conversion comes from ADC Master:
  - ADC Master starts immediately
  - ADC Slave starts after a configurable delay after the end of sampling of the master.
    Prevents an ADC from starting a conversion while the complementary ADC is still sampling the input.
- An EOC is generated at the end of each channel conversion.



- Data can be read by software from each ADCx_DR or from ADCx_CDR
- When using DMA, DMA Master channel must be used to read from the common data register ADC_CDR (only MDMA mode can be used).

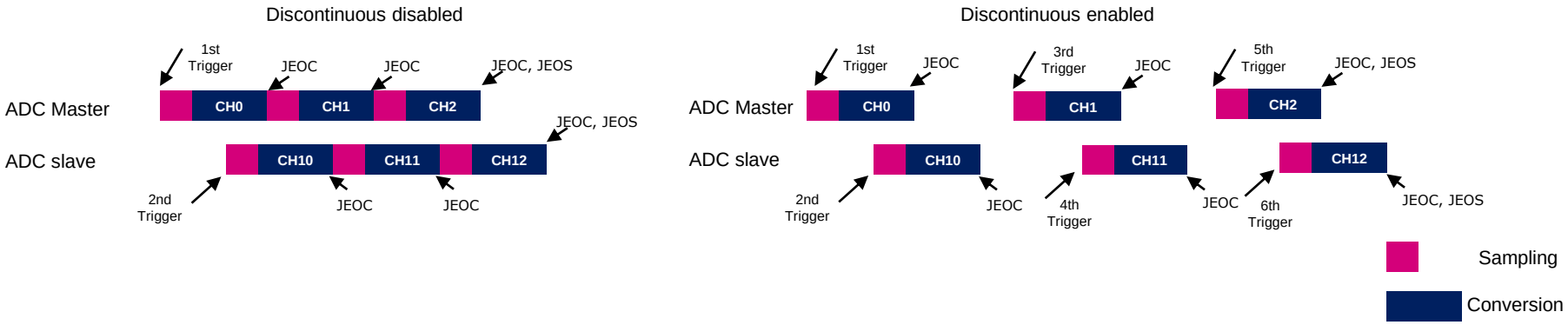
Interleaved Mode SMPPLUS bit

- **ADC_SMPR1.SMPPLUS** bit can be enabled in dual interleaved mode to have equally spaced conversions between master and slave.
- For 2,5 cycles sampling time, total conversion time is 15 cycles. So 1 cycle is added to the sampling time to have total 16 cycles conversion thus making possible to interleave every 8 cycles.



Alternate trigger mode

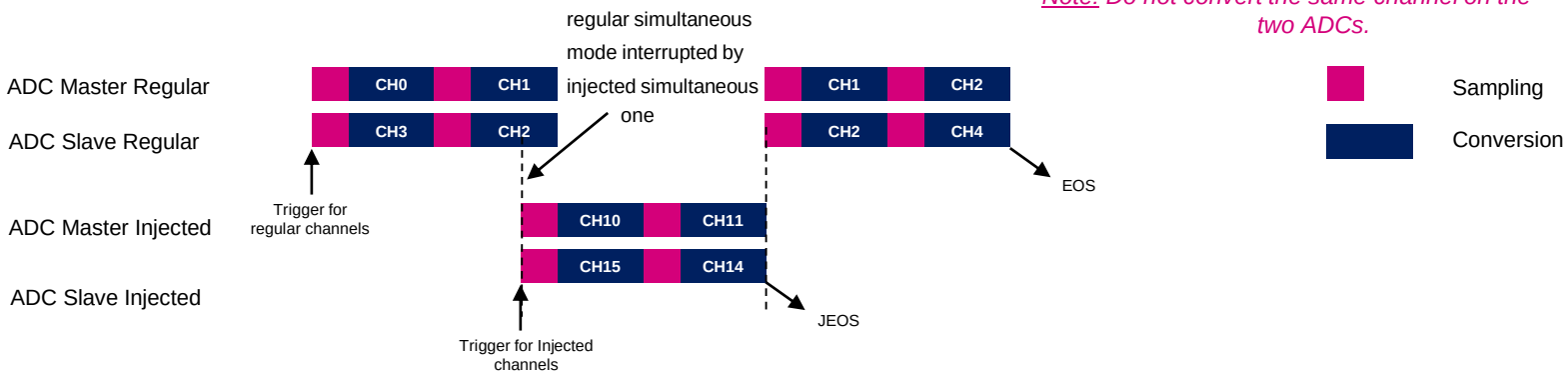
- This mode converts an injected group of channels.
- Conversions are started only using hardware triggers.
- The external trigger source comes from the injected group multiplexer of the master ADC



Injected simultaneous + Regular simultaneous

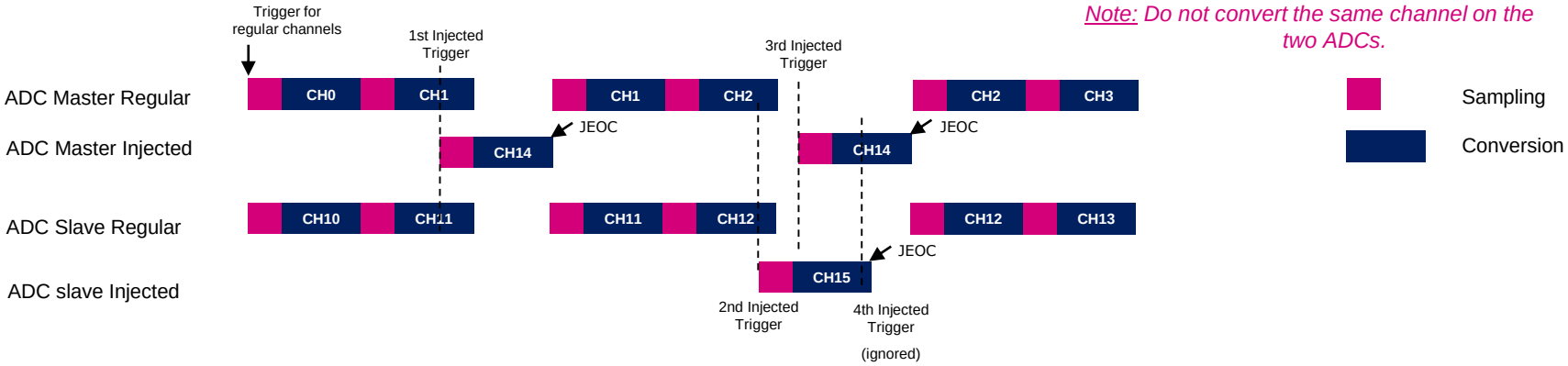
- This mode converts injected and regular groups of channels.
- The simultaneous conversion of a regular group can be interrupted to start the simultaneous conversion of an injected group.
- The external trigger source comes from the master ADC.
- Results of injected channels are stored on ADCx_JDRy registers, and results of regular channels are stored on each ADCx_DR register and on ADC_CDR register.

Note: Do not convert the same channel on the two ADCs.



Regular simultaneous + Alternate trigger

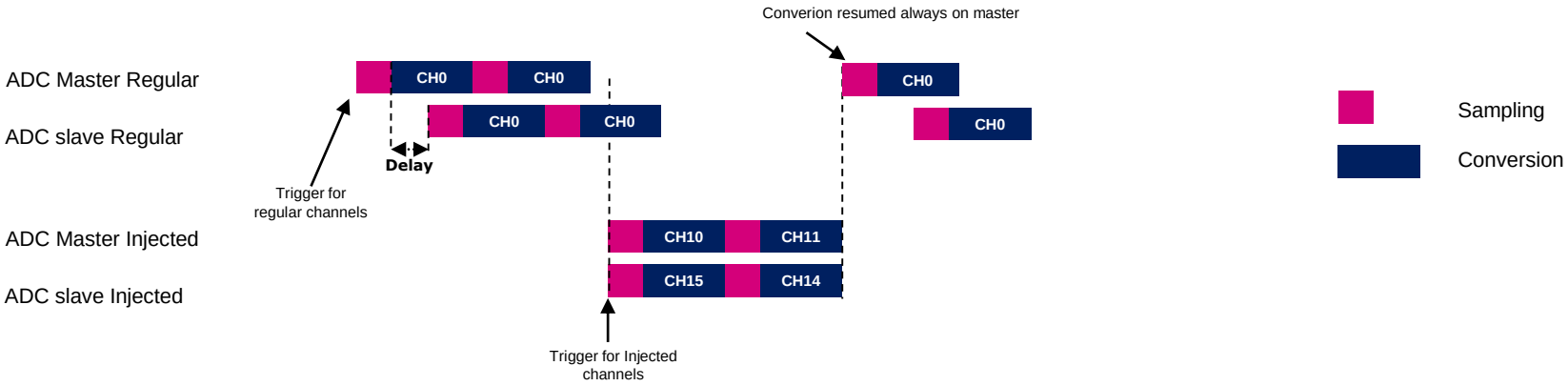
- This mode converts injected and regular groups of channels.
- The simultaneous conversion of a regular group can be interrupted to start the alternate trigger conversion of an injected group.
- The external trigger source comes from the master ADC.
- Results of injected channels are stored on ADCx_JDRy registers, and results of regular channels are stored on each ADCx_DR register and on ADC_CDR register.



Note: Do not convert the same channel on the two ADCs.

Injected simultaneous + Interleaved

- Regular interleaved conversion can be interrupted by simultaneous injected conversion.
- The interleaved conversion is resumed starting always by the master.
- It is mandatory to use the Common Data Register to read the regular data with a single read access (MDMA mode)



IO voltage booster

Decrease analog switch resistance

- IO analog switch voltage booster
  - Analog switch resistance increases when VDDA is decreasing.
  - For low VDDA, analog switch resistance can be minimized by enabling internal voltage booster to control the switch.
  - The recommended analog switch supply is as follows:

VDD	VDDA	BOOSTEN	ANASWVDD	Analog switch supply
-	>2.4 v	0	0	VDDA (default)
>2.4 v	<2.4 v	0	1	VDD
<2.4 v	<2.4 v	1	0	Voltage booster

ANASWVDD 1: I/O analog switches supplied by VDD. 0: I/O analog switches supplied by VDDA or booster
BOOSTEN 1: I/O analog switches are supplied by voltage booster 0: I/O analog switches are supplied by VDDA

Internal voltage reference VREFBUF

Internal reference up to 2v9

- Analog voltage reference Vref can be provided through internal voltage reference VREFBUF
- Three voltages are available: 2,048v ; 2,5v ; 2,9v
- Available only in packages with Vref+ pin available
- Even if VREFBUF is used, it is still needed to place decoupling capacitors to Vrefp pin

ADC internal channels

	ADC1	ADC2	ADC3	ADC4	ADC5
Temperature sensor	IN16	-	-	-	IN4
VBAT/3	IN17	-	IN17	-	IN17
VREFINT	IN18	-	IN18	IN18	IN18
OPAMPx internal output (*)	IN13 (x = 1)	IN16 (x = 2), IN18 (x = 3)	IN13 (x = 3)	IN17 (x = 6)	IN3 (x = 5), IN5 (x = 4)

(*) Internal OPAMP to ADC connection without external pin occupancy

Interrupts and DMA

Interrupt event	Description	Interrupt event	Description
ADRDY	ADC is ready to convert	**AWDx**	Analog watchdog threshold breach detection occurs
EOC	End of regular conversion	**EOSMP**	End of a sampling phase
EOS	End of sequence for regular conversion group	**OVR**	Data overrun occurred
JEOC	End of injected conversion	**JQOVF**	Injected sequence context queue overflows
JEOS	End of sequence of an injected conversion group		

- DMA request can be generated after conversion of each channel

Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Low-power run	Active.
Low-power sleep	Active. Peripheral interrupts cause the device to exit Low-power sleep mode.
Stop 0	Not available. Peripheral registers content is kept.
Stop 1	Not available. Peripheral registers content is kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.
Shutdown	Powered-down. The peripheral must be reinitialized after exiting Shutdown mode.

- In Deep power-down mode the analog part of each ADC is switched off by an on-chip power switch. Calibration data is kept.

STM32G4 Vs STM32F3

ADC features	STM32F3	STM32G4
Number of ADCs	4	5
Conversion time	0,19us (5,1Msps)	0.250us (4Msps) (1)
External Triggers	16	32
HW Oversmapling	-	yes
IO voltage booster	-	yes
Gain compensation	-	yes
Offset compensation	yes	yes + Saturation control
Bulb sampling	-	yes
Sampling time control trigger	-	yes
Internal reference Vref	-	yes (2,048v ; 2,5v ; 2,9v)
Analog Watchdog	yes	yes + Filter
Interleaved Mode SMPPLUS	-	yes

1. 0.268us (3.7Msps) in case of multiple ADCs parallel operation

References

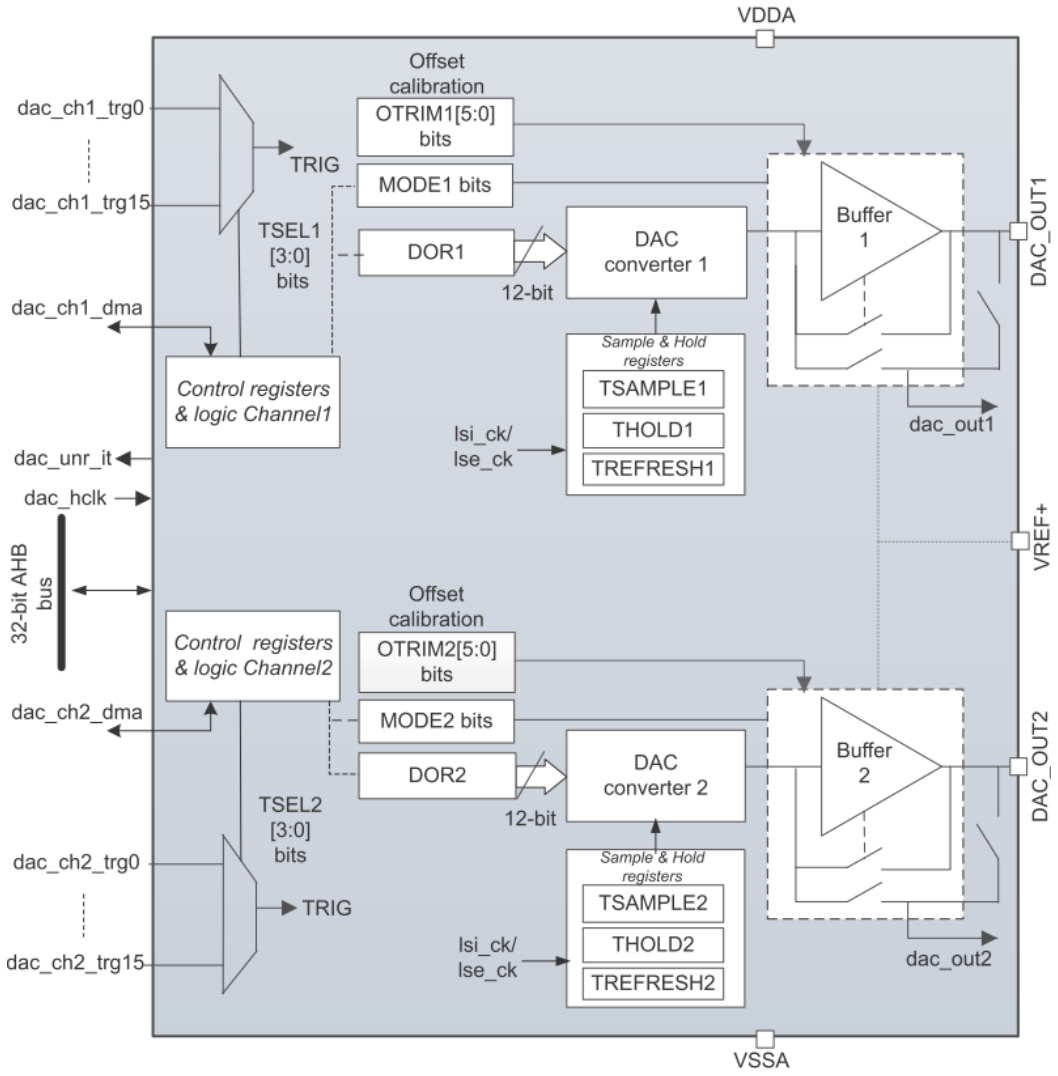
- For more details, please refer to following sources
  - AN2834: How to get the best ADC accuracy in STM32Fx Series and STM32L1 Series devices
  - AN4073: How to improve ADC accuracy when using STM32F2xx and STM32F4xx microcontrollers
  - AN2668: Improving STM32F1x and STM32L1x ADC resolution by oversampling
  - AN4629: ADC hardware oversampling for microcontrollers of the STM32 L0 and L4 series

DAC

DAC in STM32G4 – evolution

- DAC functionalities and target improvements/goals:
  - Evolution of STM32F3/ STM32L4 DACs
  - Speed: increase speed for internal usage to 15MHz (fast signal generation)
  - Number of DACs: increase to 7 DAC channels (to set more references for COMPs, OPAMPs, external outputs)
    - Internal channels are unbuffered, but speed = 15MHz
  - Speed up digital transfer (AHB bus, 2 samples per transfer)
  - Output buffer with offset calibration (for better precision with buffer)
  - New sawtooth wave generation (more complex to existing triangle wave generation) – for motor control usage
  - Add signed data format

DACx block diagram



- → **STM32G43x/ STM32G44x:**
  - **DAC1, DAC3**
- → **STM32G47x/ STM32G48x:**
  - **DAC1, DAC2 (1 channel only), DAC3, DAC4**

- 12-bit DAC converter stage
- Sources of triggers
- AHB bus (+DMA transfer)
- Buffer offset calibration
- Waveforms generation
- Sample & hold feature
- dac_outx signal for on chip peripheral
- VREF+ as reference voltage

DAC general overview

- DACs functionalities and target improvements:
  - Up to 4 DACs with 12-bit resolution
  - Up to 7 channels:
    - 3 external channels (available on pins):
      - DAC1_OUT1, DAC1_OUT2
      - DAC2_OUT1
    - 4 internal channels (fast):
      - DAC3_OUT1, DAC3_OUT2
      - DAC4_OUT1, DAC4_OUT2
  - Dual DAC channel feature
    - Independent or simultaneous conversions
  - Double data DMA capability – to reduce the bus activity
    - 2 consecutive samples transfers (2x 12-bit) in one transaction
  - VREF+ as reference voltage
    - VREF+ can be generated internally or externally (on VREF+ pin)
  - Sample and hold option
  - Waveform generation (Noise-wave, Triangular-wave, Sawtooth-wave)
  - Complex triggering system (Software, Timers, HRTIM, EXTI)
  - Unsigned or Signed data format input

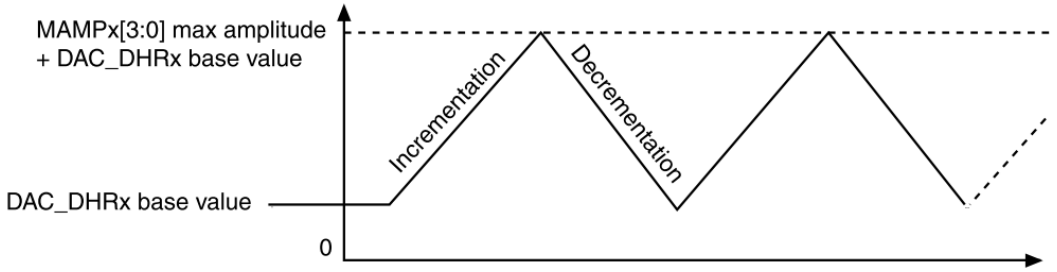
DAC channels configuration

DAC features	DAC1	DAC2	DAC3	DAC4
Maximum sampling time	1Msps		15Msps	
Output buffer	x	x		
Number of channels	2 (external)	1 (external)	2 (internal)	2 (internal)
IO connection	CH1 on PA4 CH2 on PA5	CH1 on PA6	No connection to GPIO	

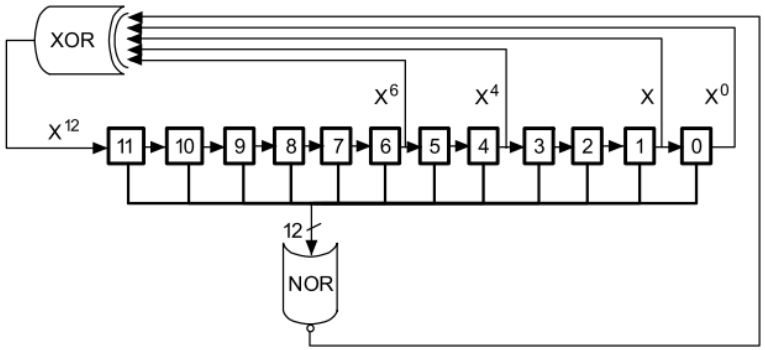
- DAC speeds:
  - 15MHz:
    - Internal channels only (DAC3_OUTx, DAC4_OUTx)
    - Unbuffered mode only
  - 1MHz:
    - 3 external channels (DAC1_OUTx, DAC2_OUT1)
    - Buffered/unbuffered mode
  - DAC mapped to AHB bus:
    - Higher speed, less latency
- Buffer:
  - Buffer offset calibration for each buffered channel

DAC wave generation (1)

- DAC autonomous waveform generation features
  - Triangle
    - Configurable base and amplitude
    - Increment = 1

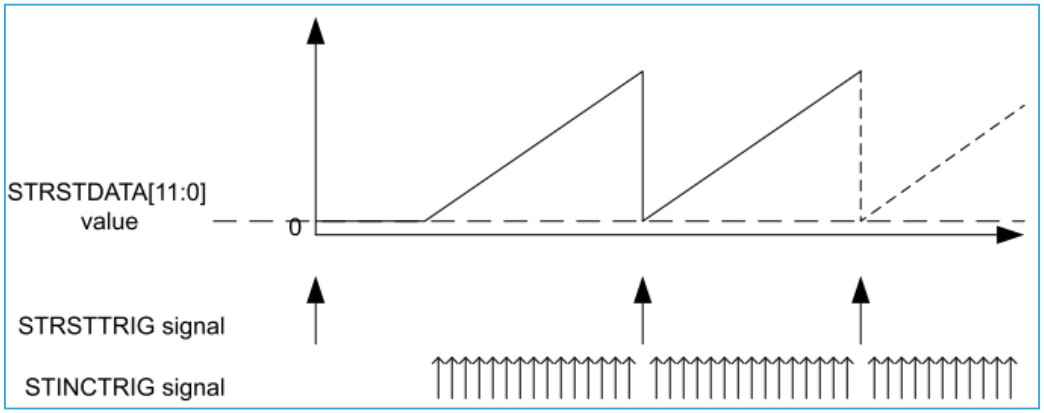


  - Noise
    - Configurable amplitude
    - Pseudo noise (linear feedback shift register)



DAC wave generation (2)

- DAC autonomous waveform generation features
  - Sawtooth
    - Configurable increment/decrement value and amplitude and base



    - Complex triggering system (for increment/decrement and for generation reset)

Table 159. DAC2 channel trigger and sawtooth reset trigger selection

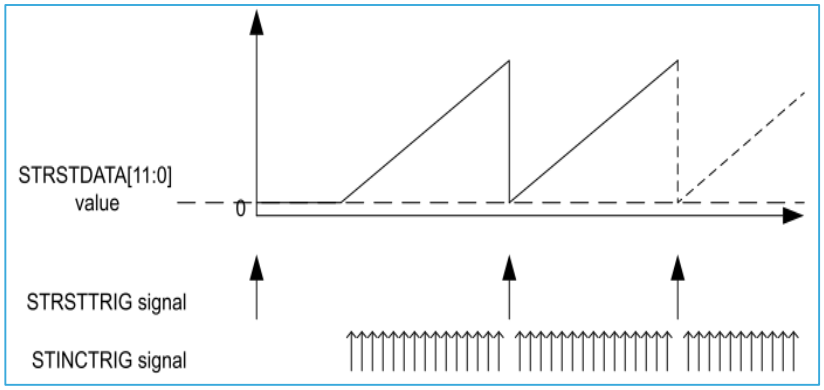
Source	Type	TSELx[3:0], STRSTTRIGSELx[3:0]
SWTRIG	Software control bit	0000
TIM8_TRGO	Internal signal from on-chip timers	0001
TIM7_TRGO	Internal signal from on-chip timers	
TIM15_TRGO	Internal signal from on-chip	

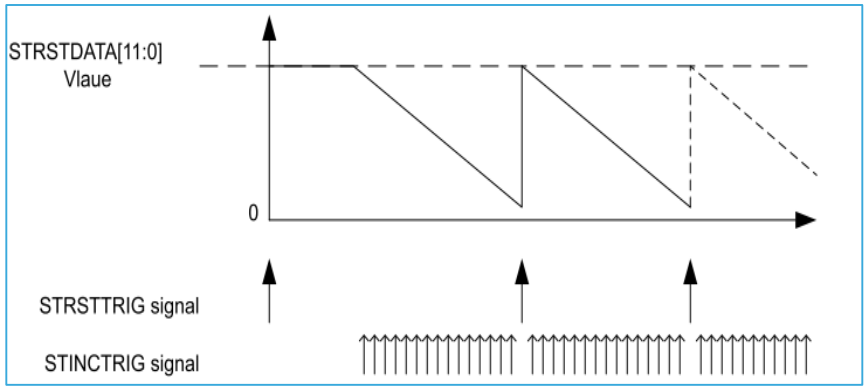
Table 160. DAC2 sawtooth increment trigger selection

Source	Type	STINCTRIGSELx[3:0]
SWTRIGB	Software control bit	0000
TIM8_TRGO	Internal signal from on-chip timers	0001
TIM7_TRGO	Internal signal from on-chip timers	0010
TIM15_TRGO	Internal signal from on-chip	0011

DAC sawtooth generation (1)

- Sawtooth generation properties

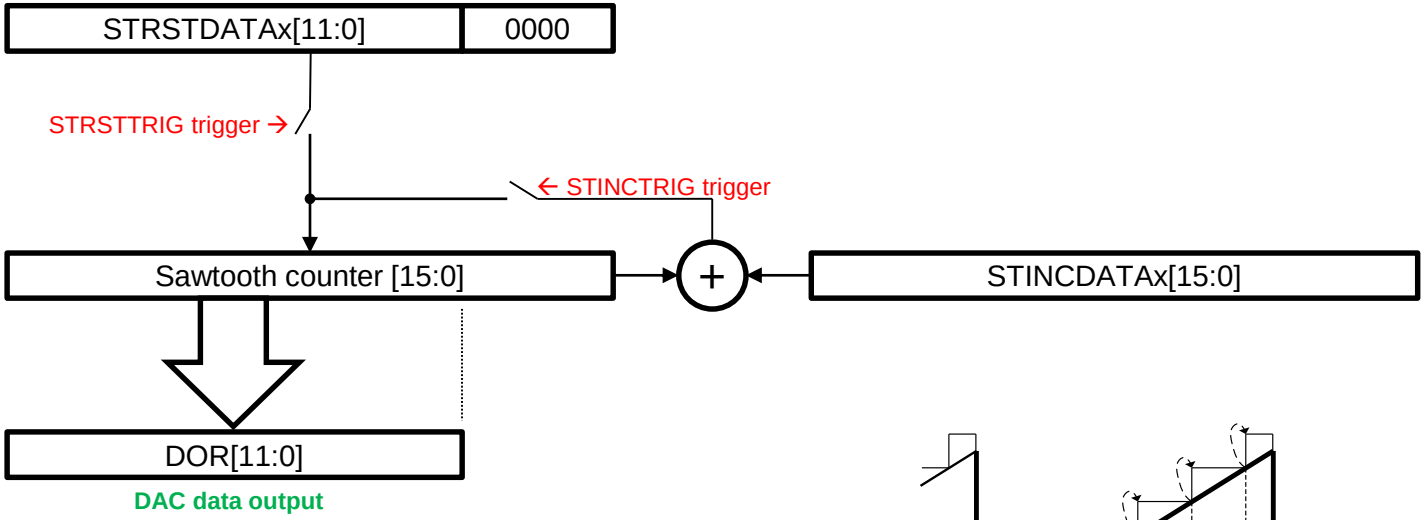




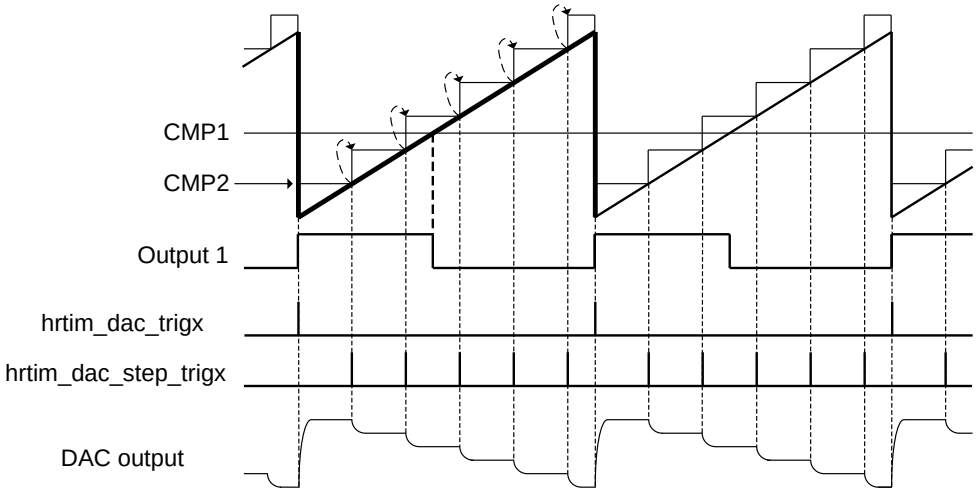
  - Increment/Decrement counter:
    - 16-bit sawtooth counter (starts at base value: STRSTDATAx[11:0]<<4)
    - At each STINCTRIG trigger is incremented/decremented by STINCDATAx[15:0]
    - Only higher 12 bits are used as DAC output
    - When reached 0x0000 or 0xFFFF, the value is saturated
    - Reset trigger signal initializes the counter to base value STRSTDATAx[11:0]<<4
  - Trigger signals for increment/decrement (STINCTRIG) and reset (STRSTTRIG)
    - SWTRIG bit, EXTI, TIMx_TRGO, HRTIM
    - Practical application usage: D-SMPS (Digital Switched Mode Power Supplies)

DAC sawtooth generation (2)

- Fractional counter:
  - Allows to have also very slow slopes (DOR[11:0] step < 1LSB)



Example of sawtooth waveform generation →



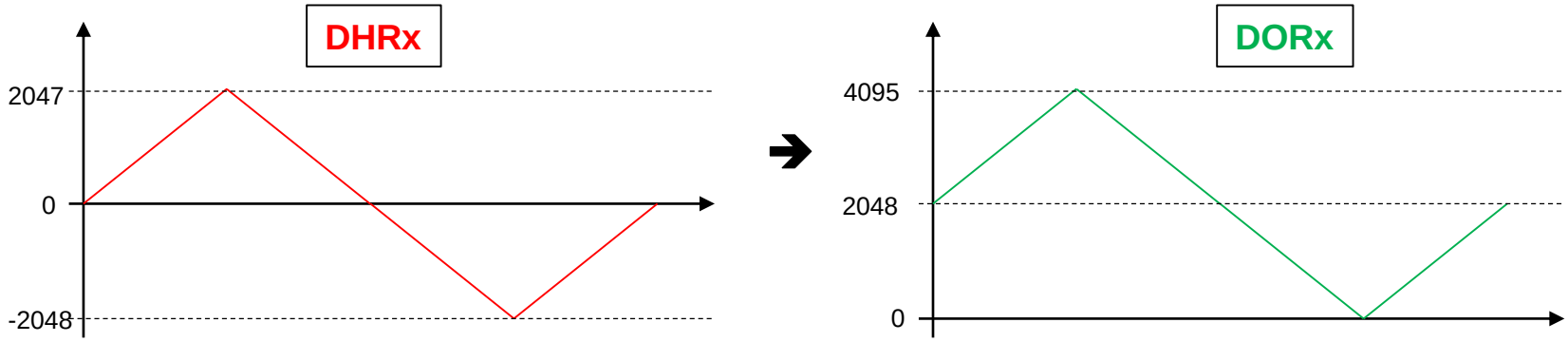
DCDU = 0 (update on roll-over), DCDT = 0 (step trigger on Compare 2)

DMA double data capability

- DMA Double data mode (DMADOUBLEx bit = 1):
  - Allows transfer of 2 consecutive DAC samples in one DMA transfer
    - Consecutive samples for one DAC channel
  - DMA request is generated on each second DAC trigger
    - 2 samples are transferred in one 32-bit transaction
  - Implementation:
    - Two data hold registers (DAC_DHRx, DAC_DHRBx)
      Two output data registers (DAC_DORx, DAC_DORBx)
    - DMA transfer fills DAC_DHRx, DAC_DHRBx
    - Trigger switches between DAC_DORx, DAC_DORBx
      - DORSTATx bit indicates active registers pair

DAC signed/unsigned format

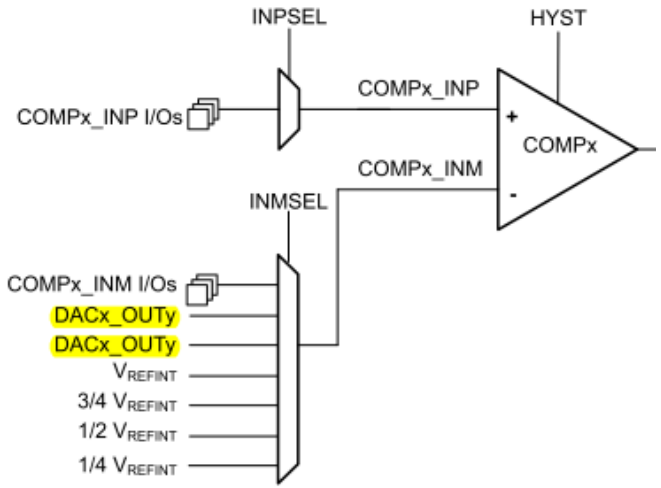
- Signed data format (SINFORMATx = 0):
  - Standard format
    - Consecutive samples for one DAC channel
- Unsigned data format (SINFORMATx = 1):
  - New feature: DAC accepts on input (DHRx register) signed format
  - The MSB is inverted while transferring from DHRx to DORx:
    - Example: 0x000 → 0x800, 0x7FF → 0xFFF, 0x800 → 0x000, 0xFFF → 0x7FF
  - All DAC resolutions are supported in signed format (8, 12, 16 bit)



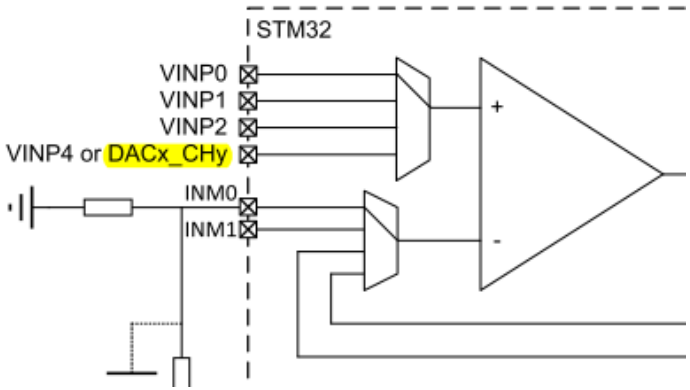
DAC internal outputs

- DAC output as internal signal only:
  - The DAC output channel can be disconnected from the DAC_OUTx output pin and can be connected to on-chip peripherals only.
  - Corresponding DAC_OUTx pin can be then used for another purpose.

- All COMPs INM signal (COMP1-COMP7):
  - Reference voltage for comparator (DC, waveform generation)



- All OPAMPs VINP signal (OPAMP1-OPAMP6) except OPAMP2:
  - Way to get internal DAC channels to pin (OPAMPx_VOUT)



DAC next features

- VREF+ pin used as reference voltage
  - Can be driven by internal VREFBUF output: 2.048V, 2.5V, 2.95V
  - Or external reference connected to VREF+ pin
- Buffer calibration:
  - Offset calibration only
  - Factory calibration loaded at DAC reset
  - Sequence of user calibration (started by bit CENx = 1):
    - Buffer output will be disconnected from the pin
    - Buffer works as comparator:
      - Code 0x800 is put to buffer and compared to VREF+/2 signal
    - By incrementing calibration register (OTRIMx[4:0] bits) is sensed buffer output (bit CAL_FLAGx) for transition
    - If transition occurred then OTRIMx[4:0] contains offset calibration

OPAMP

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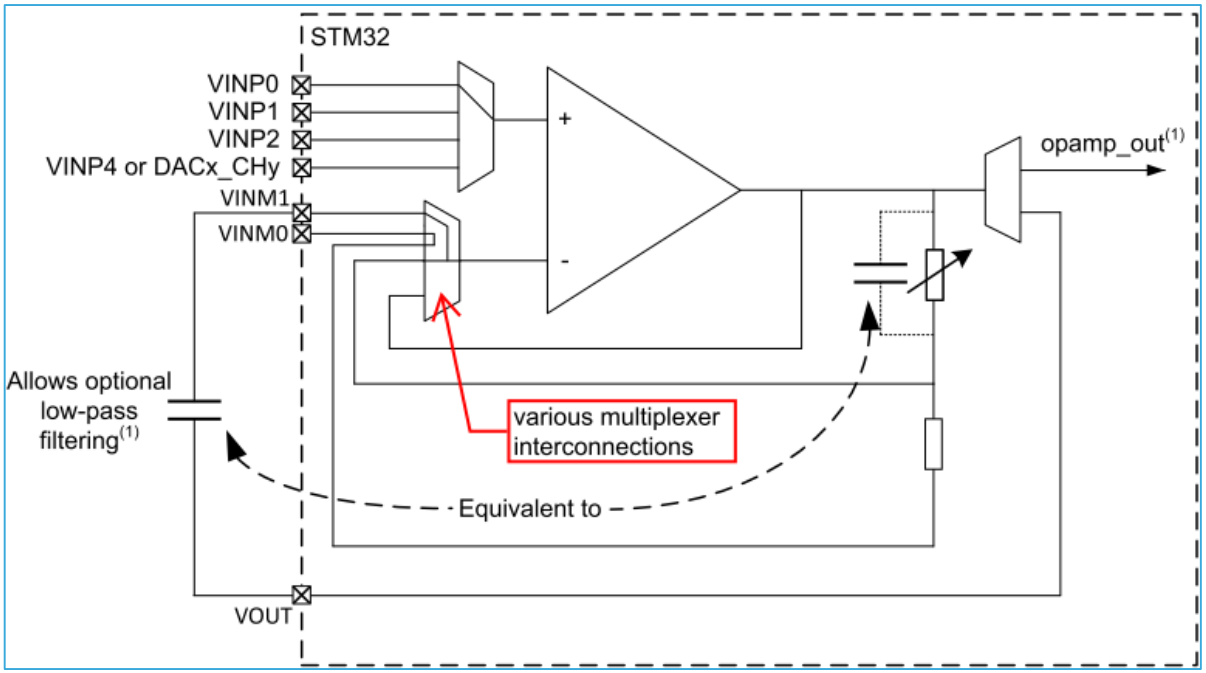
OPAMP in STM32G4 – evolution

- OPAMP functionalities and target improvements/goals:
  - Evolution of STM32F3/ STM32L4 OPAMPs
  - Speed: increase speed to 13MHz bandwidth (vs. 8.2 MHz in F3)
  - Rail-to-rail input and output voltages
  - More PGA gains: up to 64 (or -63)
  - Offset calibration

OPAMP block diagram

- **STM32G43x/ STM32G44x:** OPAMP1, OPAMP2, OPAMP3
- **STM32G47x/ STM32G48x:** OPAMP1, OPAMP2, OPAMP3, OPAMP4, OPAMP5, OPAMP6
- Inputs from internal or external signals
- Flexible modes (by multiplexing inputs)
- Internal gain settings (PGA)
- Internal output to ADC



OPAMPs general overview

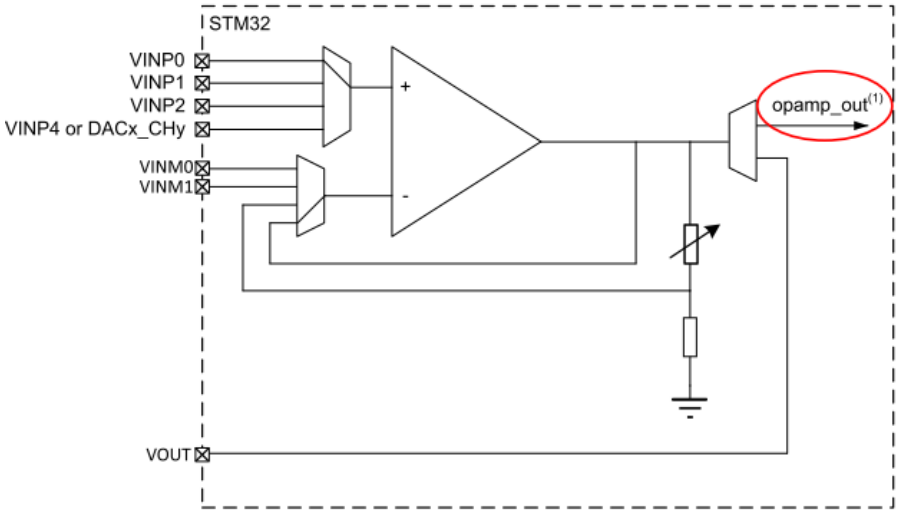
- OPAMP
  - Up to 6 x OPAMP
  - 13 MHz bandwidth
  - Rail-to-rail input and output voltage range
  - Low input bias current
  - Flexible analog multiplexers - various operation modes (inverting/non-inverting, external/internal gains, bias setting)
  - PGA gains:
    - Positive: 2, 4, 8, 16, 32, 64 (F3: no 32, 64 gains)
    - Negative: -1, -3, -7, -15, -31, -63 (F3: no negative gains)
    - Gain set externally
  - Offset calibration
  - Internal output to ADC (no external pin occupation)

OPAMP inputs/outputs configuration

OPAMP	VINPx		VINMx	VOUTx	
	External	Internal	External	External	Internal
OPAMP1	PA1, PA3, PA7	DAC3_CH1	PA3, PC5	PA2/ADC1_IN3	ADC1_IN13
OPAMP2	PA7, PB14, PB0, PD14		PA5, PC5	PA6/ADC2_IN3	ADC2_IN16
OPAMP3	PB0, PB13, PA1	DAC3_CH2	PB2, PB10	PB1/ADC3_IN1/ ADC1_IN12	ADC2_IN18/ ADC3_IN13
OPAMP4	PB13, PD11, PB11	DAC4_CH1	PB10, PD8	PB12/ADC4_IN3/ ADC1_IN11	ADC5_IN5
OPAMP5	PB14, PD12, PC3	DAC4_CH2	PB15, PA3	PA8/ADC5_IN1	ADC5_IN3
OPAMP6	PB12, PD9, PB13	DAC3_CH1	PA1, PB1	PB11/ADC12_IN14	ADC4_IN17

OPAMPs to ADC internal connection

- OPAMPs internal outputs :
  - OPAMP output can be redirected to internal connection to ADC input
  - No pin occupied - OPAMPx_VOUT is then available for another purpose

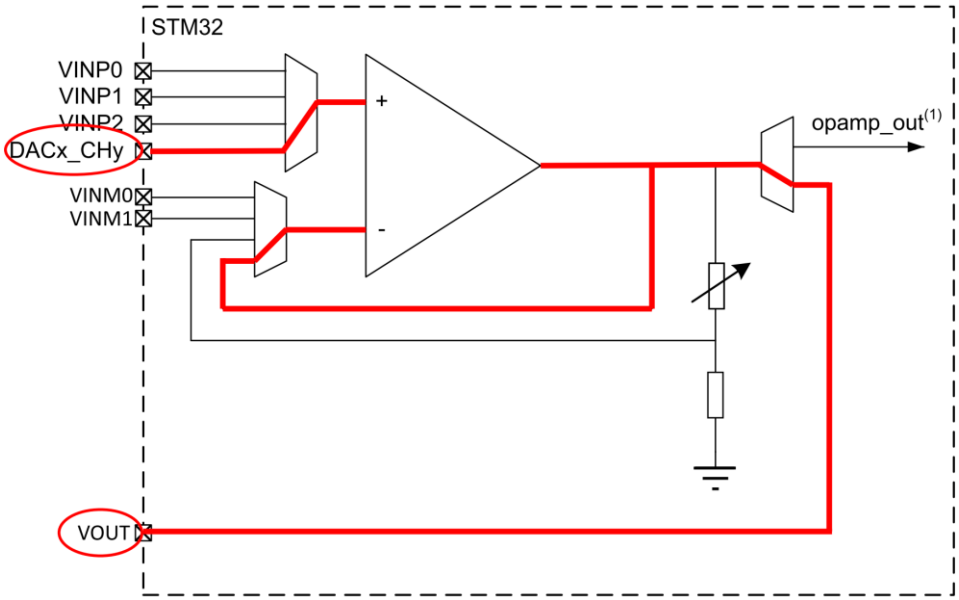


	ADC1	ADC2	ADC3	ADC4	ADC5
IN1	PA0	PA0	PB1	PE14	PA8
IN2	PA1	PA1	PE9	PE15	PA9
IN3	PA2	PA6	PE13	PB12	OPAMP5 (int.)
IN4	PA3	PA7	PE7	PB14	TempSensor
IN5	PB14	PC4	PB13	PB15	OPAMP4 (int.)
IN6	PC0	PC0	PE8	PE8	PE8
IN7	PC1	PC1	PD10	PD10	PD10
IN8	PC2	PC2	PD11	PD11	PD11
IN9	PC3	PC3	PD12	PD12	PD12
IN10	PF0	PF1	PD13	PD13	PD13
IN11	PB12	PC5	PD14	PD14	PD14
IN12	PB1	PB2	PB0	PD8	PD8
IN13	OPAMP1 (int.)	PA5	OPAMP3 (int.)	PD9	PD9
IN14	PB11	PB11	PE10	PE10	PE10
IN15	PB0	PB15	PE11	PE11	PE11
IN16	TempSensor	OPAMP2 (int.)	PE12	PE12	PE12
IN17	VBAT/3	PA4	VBAT/3	OPAMP6 (int.)	VBAT/3
IN18	VREFINT	OPAMP3 (int.)	VREFINT	VREFINT	VREFINT

Internal DAC to OPAMP output

- Internal DACs (DAC3, DAC4):
  - Unbuffered output channels (up to 4 channels) - high speed output 15MHz
  - Internal outputs only to:
    - COMPs – set reference voltage or …
    - OPAMPs – set bias voltage or …
  - No direct connection to pin

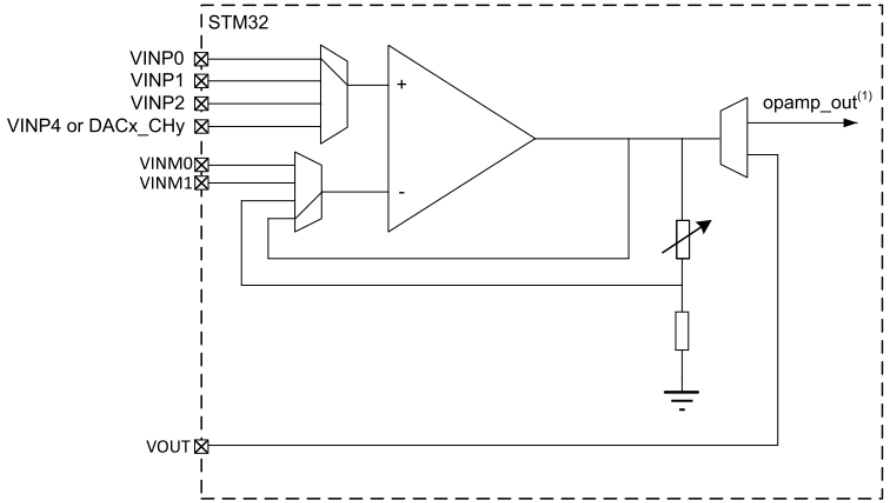
- Redirection of internal DAC signal to pin:
  - Select internal DAC channel as OPAMP input
  - Use OPAMP output in follower mode (or PGA):



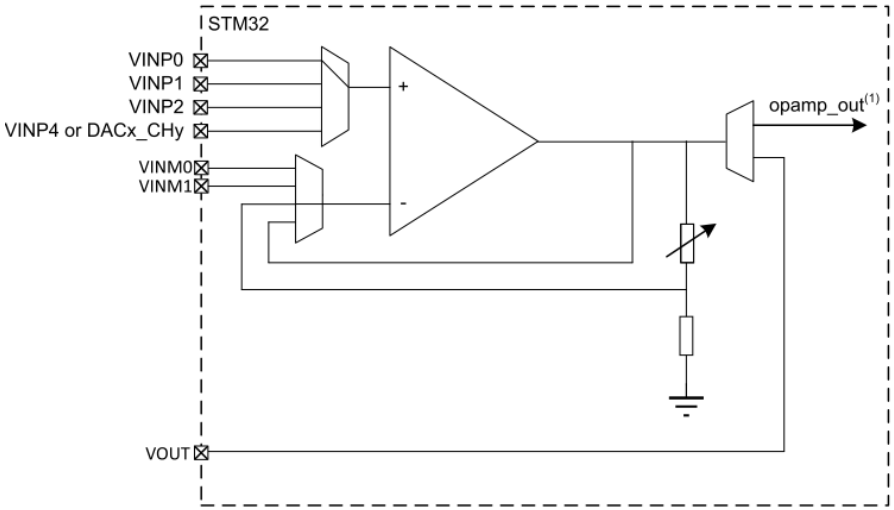
OPAMP operation modes

- Configuration of operation modes:
  - Done by proper analog multiplexers setting
  - PGA gain setting
  - Modes:
    - Standalone mode (external gain setting mode)
    - Follower
    - Programmable gain amplifier (non inverting)
    - Programmable gain amplifier (non inverting) with external filtering
    - Programmable gain amplifier (non inverting / inverting) with external bias
    - Programmable gain amplifier (non inverting / inverting) with external bias and external filtering

OPAMP modes (1)

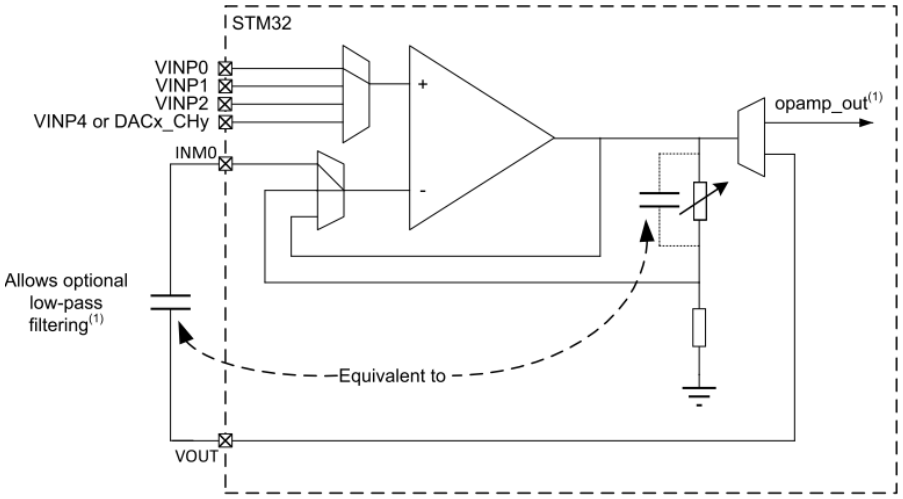


- Follower
  - VINM input not used

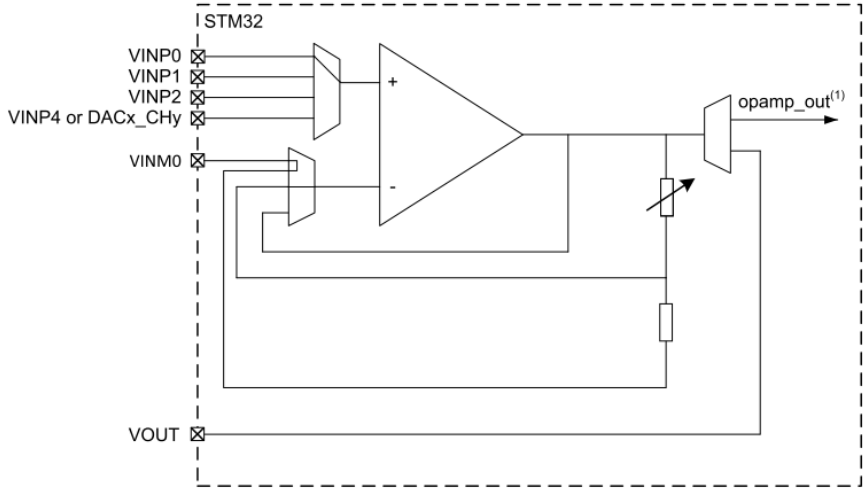


- PGA:
  - Non inverting
  - VINM input not used

OPAMP modes (2)

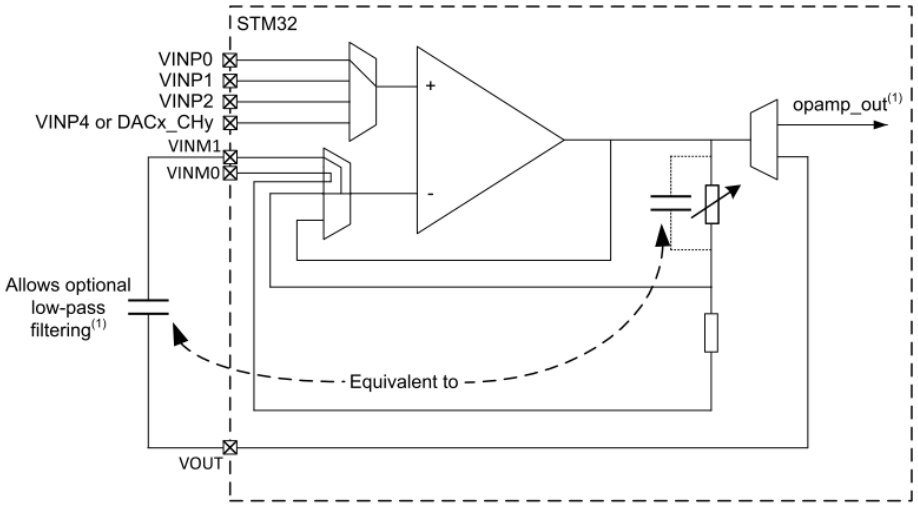


- PGA:
  - Non inverting
  - VINM input used for ext. filtering

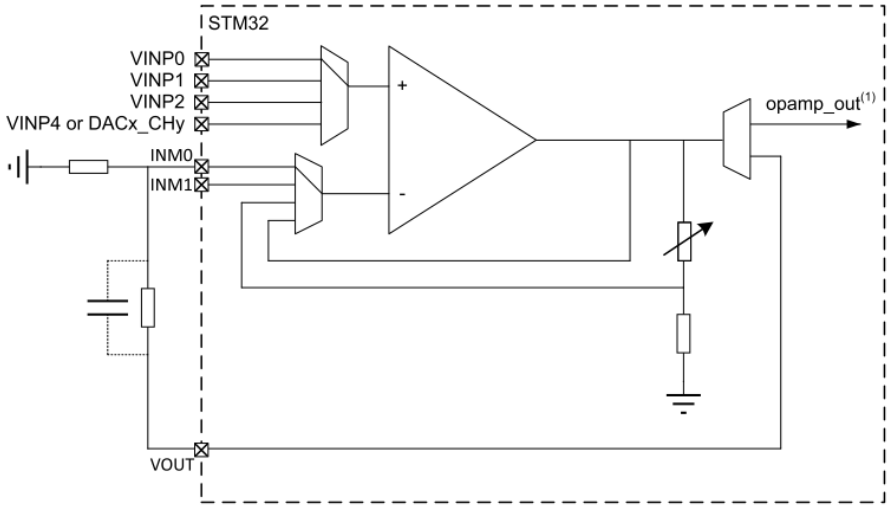


- PGA:
  - Non inverting with ext. bias
  - Or inverting with ext. bias
  - VINP / VINM inputs used

OPAMP modes (3)



- PGA:
  - Non inverting with ext. filtering (and bias)
  - Or inverting with ext. bias (and filtering)
  - VINP / VINM inputs used



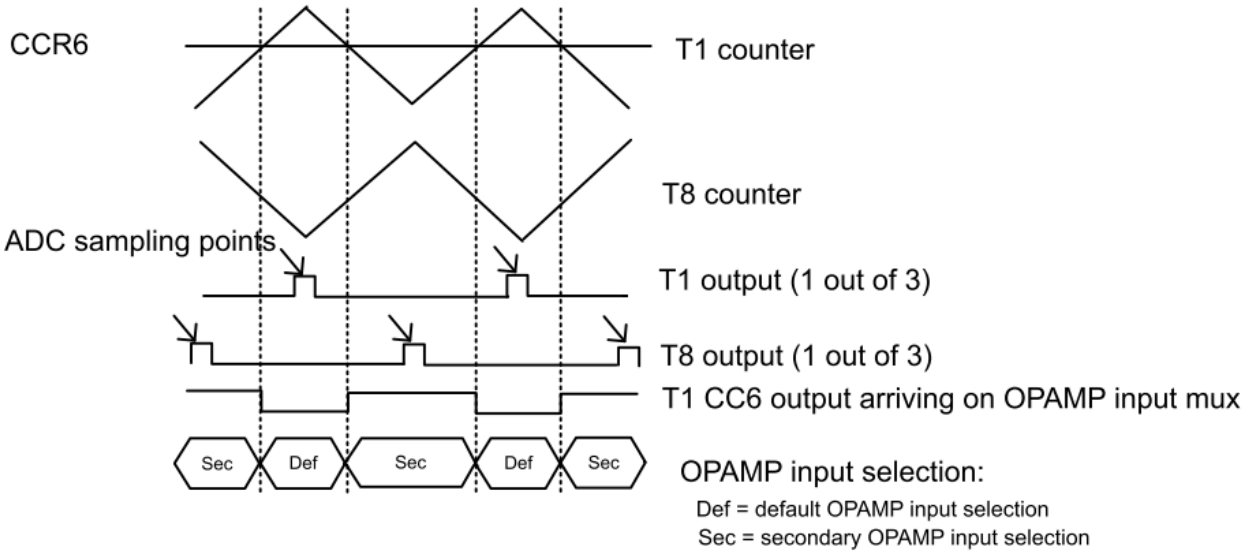
- Standalone mode:
  - External gain setting
  - Inverting or non inverting
  - VINP / VINM inputs used

OPAMP calibration

- Offset calibration:
  - At startup:
    - Loaded factory trimming value
  - User calibration:
    - Can replace factory trimming values
      - For different application conditions: VDD, temperature
    - Two calibration values per amplifier
      - TRIMOFFSETP : for P differential pair
      - TRIMOFFSETN : for N differential pair
    - Calibration sequence:
      - Enable calibration mode
      - Select N/P calibration option
      - Iterate TRIMOFFSETx and watch for CALOUT bit change
      - Then store TRIMOFFSETx value

OPAMP next features

- OPAMP speed modes:
  - Normal mode: 6.5V/us (in F3: 4.7V/µs)
  - High-speed mode (higher slew rate): 45V/us
- Timer controlled Multiplexer mode
  - VINP/VINM signals selection (analog multiplexer setting) can be done also by hardware to alternate between two input pins
    - Switch triggered by timers output signals (TIM1_CC6, TIM8_CC6, TIM20_CC6)
    - Two VINP/VINM signals selection option: Default vs. Secondary configurations
    - It works in all OPAMP modes (in F3 doesn't work in PGA modes)
  - Example: Useful for dual motor control
    - Measure the currents simultaneously on the first phase and then on the second phase



VREFBUF in STM32G4

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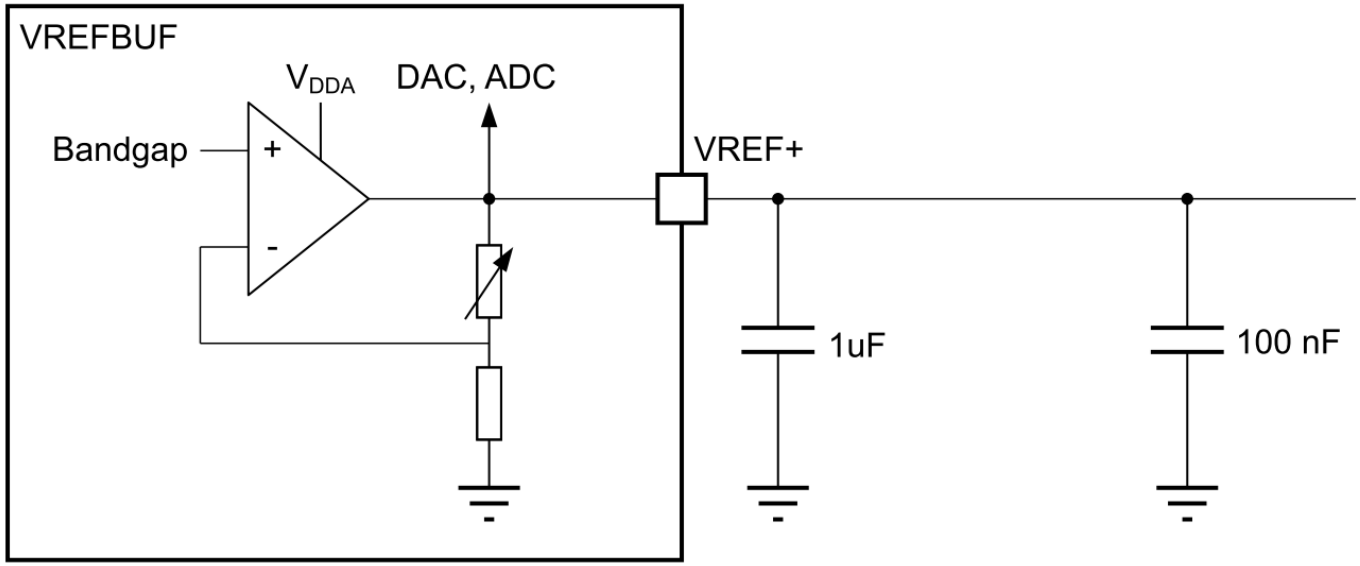
VREFBUF in STM32G4 – evolution

- VREFBUF functionalities and target improvements/goals:
  - Evolution of STM32L4 VREFBUF
    - Voltage reference buffer which can be used as voltage reference for ADCs, DACs
    - Voltage reference buffer output is available on the VREF+ pin (can be used for external purpose).
  - More voltage levels
  - Increase current capability (more ADCs, DACs)



VREFBUF overview

- VREFBUF
  - Internal voltage reference amplifier/buffer to VREF+ pin
    - Voltage reference for ADCs, DACs
    - External usage
  - 3 voltage levels:
    - ~2.048 V … (VDDA>2.40V)
    - ~2.500 V … (VDDA>2.80V)
    - ~2.900 V … (VDDA>3.15V)
  - Higher output current capability:
    - Depends from internal targets usage (DAC, ADC): 6.5mA
  - Operation modes:
    - VREF+ pin as voltage output (VREFBUF enabled)
    - VREF+ pin as voltage input (VREFBUF disabled, VREF provided by external reference)

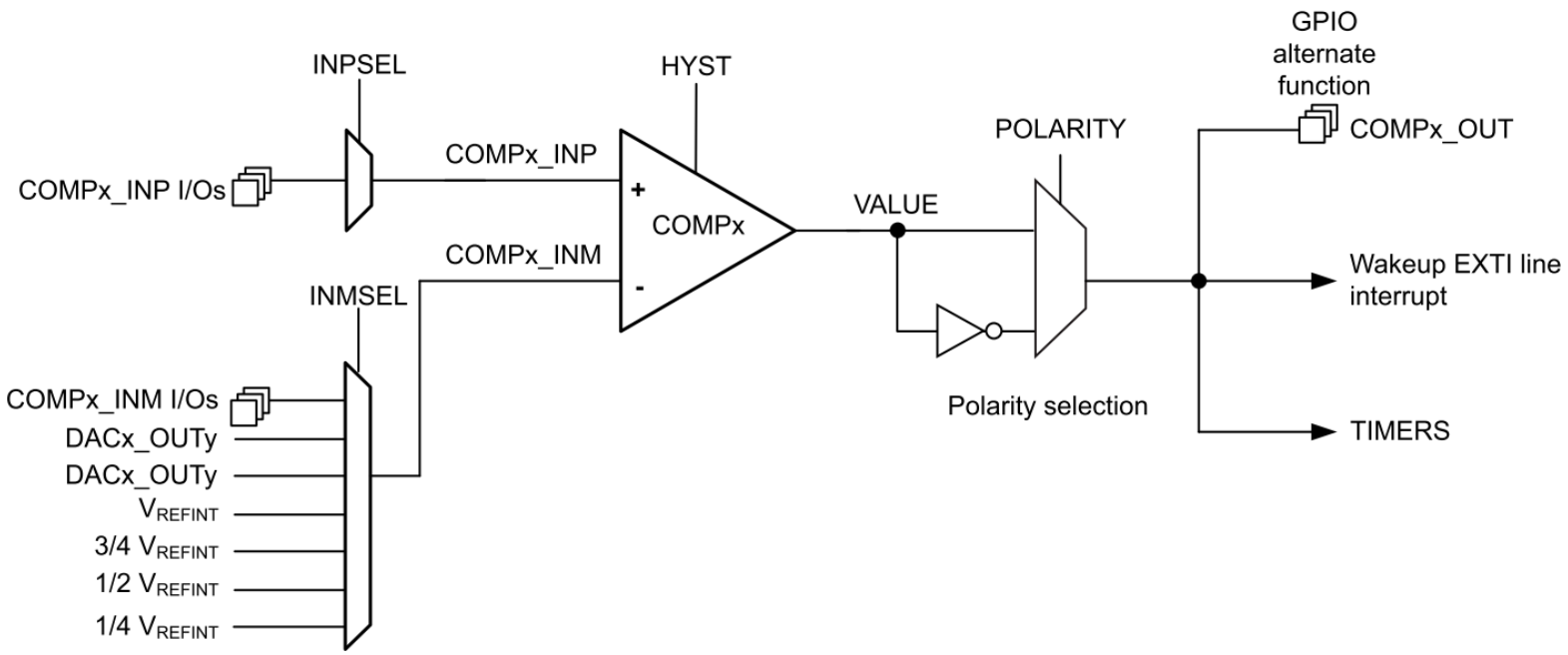
COMP

COMPs in STM32G4 – evolution

- COMP functionalities and target improvements/goals:
  - Evolution of STM32F3/ STM32L4 comparators
  - Speed: increase speed down to 16.7ns propagation delay
  - Programmable hysteresis
  - Extend number of inputs (internal, external signals)
  - Wakeup from low power mode
  - Motor control focus: cooperation with timers (TIMs, HRTIM), DACs, Vrefint

COMP block diagram

- **STM32G43x/ STM32G44x:** COMP1, COMP2, COMP3, COMP4
- **STM32G47x/ STM32G48x:** COMP1, COMP2, COMP3, COMP4, COMP5, COMP6, COMP7
- Inputs from internal or external signals
- Polarity setting
- Output to pins, timers (TIM, HRTIM), EXTI



COMPs general overview

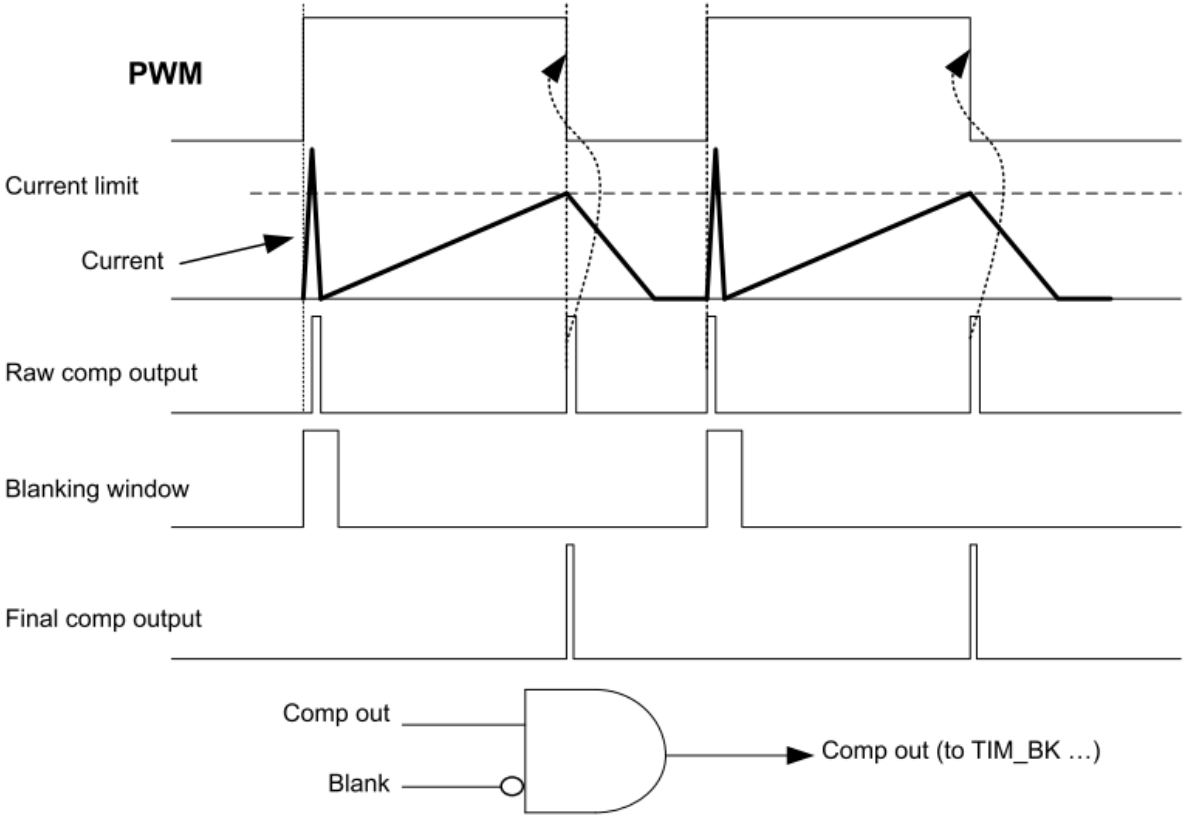
- COMP
  - Up to 7 x COMP
  - ~15 ns propagation delay (in F3: ~25ns)
  - Inputs:
    - External pins
    - Internal signals:
      - DACs channels (internal/external)
      - Vrefint submultiple: ¼, ½, ¾, 1
  - Outputs:
    - GPIOs (alternate function)
    - Timers (TIMs, HRTIM) inputs (trigger, break signals, OCREF_CLR inputs)
  - Output blanking feature – to prevent false spikes removal (current commutation in motor control)
  - Programmable hysteresis
  - Wakeup from low power mode (LP Run, Sleep, LP Sleep, Stop)

COMP inputs/outputs configuration

COMP	INM			INP	OUT	
	External	Internal		External	External	Internal
COMP1	PA4, PA0	DAC3_CH1 DAC1_CH1	¼, ½, ¾, 1 Vrefint	PA1, PB1	PA0, PA6, PA11, PB8, PF4	TIMs, HRTIM, EXTI signals
COMP2	PA4, PA2	DAC3_CH2 DAC1_CH2		PA7, PA3	PA2, PA7, PA12, PB9	
COMP3	PF1, PC0	DAC3_CH1 DAC1_CH1		PA0, PC1	PB7, PB15, PC2,	
COMP4	PE8, PB2	DAC3_CH2 DAC1_CH1		PB0, PE7	PB1, PB6, PB14	
COMP5	PB10, PD13	DAC4_CH1 DAC1_CH2		PB13, PD12	PA9, PC7	
COMP6	PD10, PB15	DAC4_CH2 DAC2_CH1		PB11, PD11	PA10, PC6,	
COMP7	PD15, PB12	DAC4_CH1 DAC1_CH2		PB14, PD14	PA8, PC8	

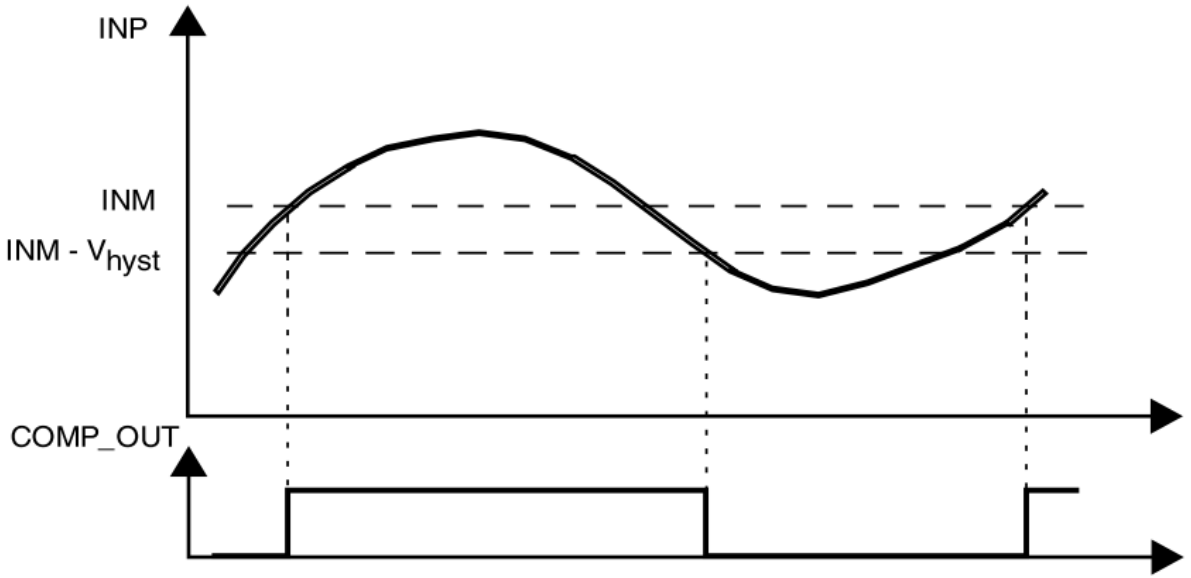
COMP blanking

- COMP blanking feature:
  - Blanking signal can mask comparator output
    - Blanking window is defined by timer output compare signal (TIMx_OCy)
  - Usage: for short current peaks suppression (from current commutation)



COMP hysteresis

- COMP programmable hysteresis:
  - 8 levels of hysteresis:
    - 0 – 63mV with 9mV step
    - Set by HYST[2:0] bits
  - Hysteresis influences output falling edge only:



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