Computer Science Tripos – Part II – Progress Report

An accelerated, network-assisted TCP recovery

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Work Completed

- Are you on track?
- But what is your project? Its aims?

Over the Michaelmas term, I have studied thoroughly the TCP congestion control and recovery mechanisms. With that understanding, I have completed the design for the architecture of my application. It was primarily based around the SimpleSumeSwitch Architecture [1].

With regard to the programming tools and equipment, I have familiarised myself with both the P4 programming language and the P4→NetFPGA workflow by working through the available tutorials. After that, I implemented the architecture and the buffering logic in P4. This was a non-trivial task, as the P4 language and the P4→NetFPGA platform are rather new with a growing community and only have a few publicly available
? documentation. With popular programming languages like Java or C++, one can easily ask questions and find help on `Stack Overflow`. With P4, the main platform for asking questions and getting help is through the `NetFPGA SUME Beta list` [2] mailing list. I have also completed setting up the machine with a NetFPGA SUME board installed for development.

There was an unexpected difficulty that came up during the Michaelmas vacation that
hidden made the project currently slower than expected by 2 weeks. Originally, the plan was to have the project written entirely in P4 language. Unfortunately, what I am trying to do what is it?
cannot really be properly expressed in P4. P4 programs are meant to operate on packet headers only while what I am currently looking for is a way to express programmable buffering logic as opposed to programmable packet processing. To overcome this issue, I plan to add a custom HDL module that follows the SimpleSumeSwitch pipeline which will buffer packets to be retransmitted.

While I was held off by the abovementioned difficulty, I started to write a skeleton for the dissertation. what's the recovery?

Work to be Done

you haven’t told me what this is

Currently, with the change in plan, I am finishing up the P4 code for the application. I will need to test and provide a performance evaluation of the design. Once that is done, I need to demonstrate its interoperability with a software-based client/application to meet my success criteria.

After that, I will need to continue implementing the extensions to the project. I am positive that I will be able to implement some of the extensions proposed.

References

[1] SimpleSumeSwitch Architecture (v1.2.1 and Earlier), `https://github.com/NetFPGA/P4-NetFPGA-public/wiki/SimpleSumeSwitch-Architecture-(v1.2.1-and-Earlier).`

[2] Cl-netfpga-sume-beta – NetFPGA SUME Beta list, `https://lists.cam.ac.uk/mailman/listinfo/cl-netfpga-sume-beta`