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Computer Science Tripos - Part II Project

An accelerated, network-assisted TCP fast retransmit

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Proforma

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Original Aims of the Project

The aim of this project is to investigate the feasibility and effectiveness of a programmable data plane in application to Transmission Control Protocol (TCP) congestion control. More specifically, I aim to design, implement and evaluate a programmable switch to assist the TCP fast retransmit mechanism. The implementation will be evaluated based on a series of tests, including both software and hardware simulations. A performance evaluation will also be provided.

Work Completed

Almost all my success criteria were met, with the exception of demonstrating the interoperability of my implementation with a software-based client/application. The architecture was designed, then implemented in P4. The implementation was tested via three different simulations: SDNet simulation, SUME simulation and hardware simulation. A performance evaluation of the design was provided. Two of the extensions were also completed.

[1] This word count was computed using `texcount -sum -inc -utf8 -sub=chapter diss.tex` for chapters 1–5.

Special Difficulties

The design stage of the architecture took longer than anticipated due to the limitations of SDNet and the SimpleSumeSwitch architecture of the P4-NetFPGA platform. The current P4-NetFPGA only supports programmable packet processing, i.e. operations on packet headers only, while this project used programmable buffering logic, which would require the ability to buffer packets. Hence, my design cannot be fully expressed in P4 alone. To circumvent this, I had to learn to use Verilog in order to design a different architecture by adding additional HDL modules into the framework that allow packet buffering. This rendered me unable to demonstrate the interoperability of my design with a software-based client/application and meet all my success criteria.

Declaration

I, Thanh Bui of Downing College, being a candidate for Part II of the Computer Science Tripos, hereby declare that this dissertation and the work described in it are my own work, unaided except as may be specified below, and that the dissertation does not contain material that has already been used to any substantial extent for a comparable purpose.

SIGNED DATE

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Chapter 1

Introduction

In this chapter, I provide the motivation for this project and setup the problem I am solving. I also explain some key algorithms involved. Finally, I cover some related work.

1.1 Motivation

Transmission Control Protocol (TCP) is the protocol of choice in many data centres. However, it is very sensitive to losses (by design, as a mean for congestion control), which can degrade the performance within the data centres significantly [1]. Various congestion control, avoidance and recovery mechanisms are thus of high importance in this field to minimise such loss rate. Still, not all TCP losses are born equal. For example, losses happening at the destination host's network interface card (NIC) are not an indication of congestion within the network. It is assumed that fast retransmission of such lost packets, from within the network, can increase the utilisation of the network.

In-network computing is an emerging research area in systems and networking, where applications traditionally running on the host are offloaded to the network hardware (e.g. switch, NIC). Examples of applications offloaded in the past include network functions (DNS server [2]), distributed systems functions such as consensus (P4xos [3]), various caching (netCache [4], netChain [5]) and even a game (Tic-Tac-Toe). Key-Value Store (KVS) is also among the popular type of in-network applications.

Therefore, it is particularly interesting, and indeed challenging, to see how network-accelerated KVS concepts can be applied to TCP fast retransmit mechanism in order to improve cross-datacentre performance.

1.2 Project Aims

Fast retransmit is an enhancement to TCP that reduces the time a sender waits before retransmitting a lost segment. A TCP sender normally uses a simple timer to recognize lost segments. If an acknowledgement is not received for a particular segment within a specified time (a function of the estimated round-trip delay time), the sender will assume the segment was lost in the network, and will retransmit the segment.

Duplicate acknowledgement (DUP ACK) is the basis for the fast retransmit mechanism. After receiving a packet (e.g. with sequence number 1), the receiver sends an acknowledgement by adding 1 to the sequence number (i.e. acknowledgement number 2). This indicates to the sender that the receiver received the packet number 1 and it expects packet number 2. Suppose that three subsequent packets are lost. The next packets the receiver sees are packet numbers 5 and 6. After receiving packet number 5, the receiver sends an acknowledgement, but still only for sequence number 2. When the receiver receives packet number 6, it sends yet another acknowledgement value of 2. DUP ACK occurs when the sender receives more than one acknowledgement with the same sequence number (2 in our example).

When a sender receives several DUP ACKs, it can be reasonably confident that the segment with the sequence number specified in the DUP ACK was dropped. A sender with fast retransmit will then retransmit this packet immediately without waiting for its timeout.

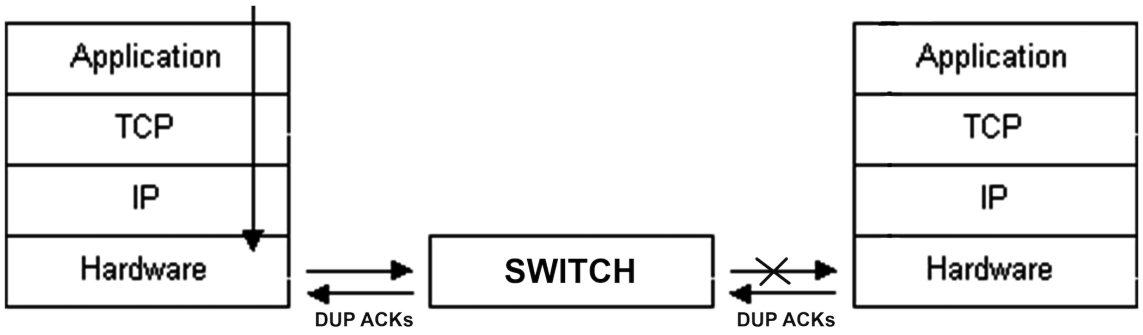

Figure 1.1: The standard convention of TCP handling.

Currently, the DUP ACKs will traverse all the way back to the sender (**Figure 1.1**). The sender receives the DUP ACKs, then retransmits the packet with the next higher sequence number.

This project aims to design and implement a programmable switch that assists the TCP fast retransmit algorithm. The programmable switch will be able to retransmit the packets from within the network, instead of waiting for the DUP ACKs to get back

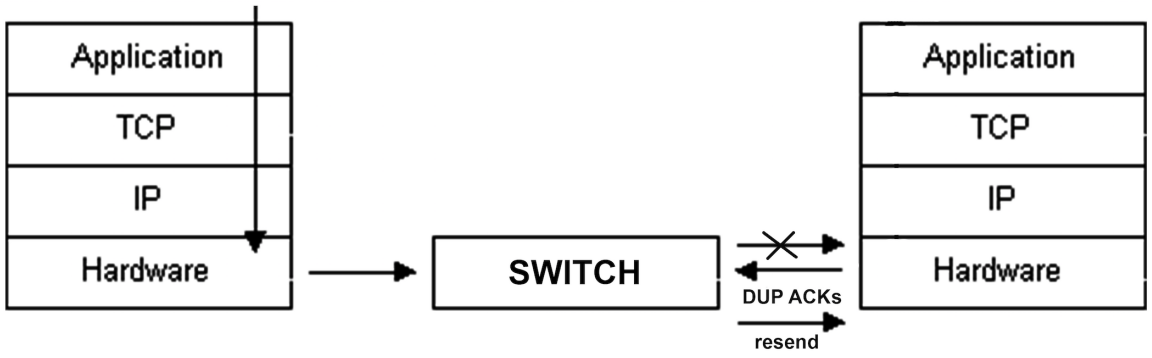

Figure 1.2: The proposed TCP handling.

to the host (**Figure 1.2**), thereby aims to reduce the response time to DUP ACKs and reduce unnecessary changes to the congestion window. The implementation will be based on the KVS concept, where the keys are the flow ID and the packet sequence number, and the value is the payload.

1.3 Related Work

1.3.1 TCP Congestion Control

One of the main aspects of TCP is congestion control, where a number of mechanisms are used to achieve high performance and avoid sending more data than the network is capable of forwarding, that is, to avoid causing network congestion. In particular, TCP uses a *congestion avoidance* algorithm that includes various aspects of an additive increase/multiplicative decrease (AIMD) scheme, with other schemes such as *slow start*, *fast retransmit* and *fast recovery* to achieve congestion avoidance.

The four intertwined algorithms are defined in more detail in RFC 5681[6]. In this project, we are mostly interested in the *fast retransmit* algorithm, which has been explained in the previous section.

1.3.2 Programmable Data Planes

In the last eight years, Software-defined Networking (SDN) and the OpenFlow protocol have reshaped the way people configure forwarding devices and determine network behaviour, by offering an open interface upon which apps like routing, monitoring, etc. can be built. OpenFlow has been the *de facto* implementation of SDN. The key idea behind it was to decouple the control plane from the data plane, which allows

centrally managing the control plane in software, while opening the control logic to the users. However, it is still very limited to a fixed set of features, which does not include new or custom protocols, statistics other than Packet, Byte count and Flow duration, and actions such as stateful matching or forwarding logic [7]. This can change drastically with the re-emergence of programmable data planes and languages like P4 [8–10] and Protocol Oblivious Forwarding (POF) [11, 12]. They enable faster development/provisioning of new and/or custom protocols, as opposed to the long wait for the release of fixed-function Application-Specific Integrated Circuit (ASIC) switches supporting standardised protocols [13]. Data plane programmability has the potential to unleash a new generation of future-proof forwarding devices, which are able to support major control plane and protocol updates, without mandating any hardware upgrades.

Chapter 2

Preparation

In this chapter, I first state the software I used and the starting point for this project. I move on to present the formal requirements. Finally, I discuss the detailed preparation for the project, which includes the project workflow.

2.1 Software Used

2.1.1 Programming Languages

In this project, I used a multitude of languages, including **P4**, **Python**, **Verilog** and **Tcl**.

- **P4** is a language designed to describe packet processing logic in the packet forwarding planes. Besides, unlike general purpose languages such as C or Python, P4 is domain-specific with a number of constructs optimized around network data forwarding, hence is well-suited for implementing the forwarding plane of network elements such as our switch.

- **Python** was used extensively in the evaluation because of the `scapy` module, which enables the user to send, sniff, dissect and forge network packets. This capability allows me to write unit tests for my program by building customised packets, sending and checking them.

- **Verilog** was used to implement certain HDL modules within the P4-NetFPGA platform, in order to add or modify certain functionalities to suit the purpose of my design. It is the language of choice of the P4-NetFPGA platform.

- **Tcl** was used to write project wrappers and debug scripts.

I also made use of the `make` build automation tool to automate project builds, tests and benchmarks.

2.1.2 Development Environment

- **The NetFPGA SUME Board**[2] is an advanced board that features one of the largest and most complex FPGA's ever produced, a Xilinx Virtex-7 690T supporting thirty 13.1 GHz GTH transceivers. This board easily supports simultaneous wire-speed processing on the four 10Gb/s Ethernet ports, and it can manipulate and process data on-board, or stream it over the 8x Gen3 PCIe interface and the expansion interfaces. It is indeed ideal for any high-performance design such as in this project.

- **P4→NetFPGA** (P4 on NetFPGA) is the environment to develop and test P4 programs using the Xilinx P4-SDNet[3] toolchain within the NetFPGA SUME reference switch design.

- **Vivado® Design Suite** is a software suite produced by Xilinx[4] for synthesis and analysis of HDL designs. Vivado was used in the project because it is the design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips. Its flexibility also enables me to simulate my design behaviour with different stimuli, synthesize the design to hardware and perform timing analysis.

- **Git** was used for version control, allowing quick roll-back and efficient management of multiple source trees using branches to implement different functionalities at various stages of the project.

- **Backups** were taken by uploading relevant files to Microsoft OneDrive[5]. The git repository itself was hosted remotely on GitHub[6].

2.2 Starting Point

This project uses the knowledge about TCP introduced in the Part IB *Computer Networking* course and the experience in Electronic Computer-aided Design (ECAD) and working with a design-flow for Field Programmable Gate Arrays (FPGAs) from Part IB *ECAD and Architecture Practical Classes*.

[2]A collaborative effort between Digilent, the University of Cambridge and Stanford University.
[3]https://www.xilinx.com/products/design-tools/software-zone/sdnet.html
[4]https://www.xilinx.com/
[5]https://onedrive.live.com/about/en-gb/
[6]https://github.com/ttbui11/part-ii-proj/

During the development of this project, I acquired further knowledge from the materials covered in the following Part II and Part III courses:

- *High Performance Networking* — Introduction to P4 and P4→NetFPGA;
- *Principle of Communications* — TCP flow control and congestion control. Design choices for scheduling and queue management algorithms for packet forwarding;
- *LaTeX and MATLAB* — Typesetting the project proposal and dissertation.

In terms of familiarity, I had no prior experience with P4 programming language, the P4→NetFPGA workflow and Tcl, and little experience with Verilog, based on the similar language SystemVerilog learnt in Part IB *ECAD and Architecture Practical Classes*. Therefore, I had to spent some time learning the languages and the workflow. I had some prior experience in Python and Git from various projects and internships.

The main code in P4 and the tests in Python were written from scratch, using the template given by the P4→NetFPGA workflow as the starting point. The code for the additional modules and externs in Verilog as well as the project wrappers in Tcl are modified from some of the current modules to suit the required functionalities.

2.3 Requirements Analysis

This project has one software deliverable: an implementation of a programmable switch that will retransmit a packet when it receives the third DUP ACK from the receiver.

Below is a list of requirements and extensions for the deliverable, prioritised using *MoSCoW* criteria [14]:

Must have

- Have an implementation of the switch in P4.
- The implementation works correctly in an SDNet simulation.
- The implementation works correctly in a SUME simulation.
- The implementation works correctly in a hardware simulation.
- A performance evaluation of the design.

Should have

- The switch will send a notification to the source if the retransmit fails.
- A performance evaluation in comparison to existing TCP fast retransmit mechanism.

Could have

- The design will support more than a single flow, and support the configuration of flows to monitor.
- The design will support different packet sizes.
- The design has the ability to adaptively add or remove flows to monitor.

Won't have

- The implementation will not be simulated using network simulators such as ns2 or omnet++.

2.4 Detailed Preparation

2.4.1 The P4 Language

2.4.2 The Xilinx P4-SDNet

The Xilinx P4-SDNet compiler is the centerpiece of the P4→NetFPGA workflow. It is the Xilinx SDNet original design environment for an internally-created packet processing language called PX [15], with a P4 to PX translator. Figure 2.1 depicts the process of compiling P4 programs that target the SimpleSumeSwitch architecture using P4-SDNet. The front end translator maps P4 programs into corresponding PX programs and also produces a JSON file with information about the design that is required by the runtime control software. The PX program is passed, along with configuration parameters, into SDNet which then produces an HDL module that implements the user's P4 program, and has standard AXI-Stream packet interfaces and an AXI-Lite control interface. SDNet generated designs can be configured to process packets at line rates between 1 and 400 Gb/s, hence is able to easily handle the aggregate 40G rate in the SUME reference switch design. SDNet also produces a SystemVerilog simulation testbench, C

drivers to configure the PX tables, and an optional C++ model of the PX program to be used for debugging purposes.

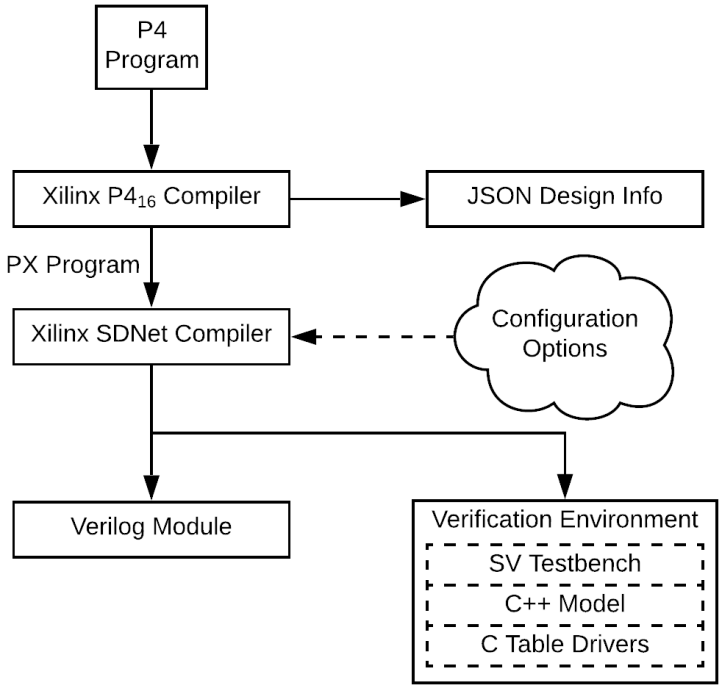

Figure 2.1: The Xilinx P4-SDNet compilation flow. P4 programs are first translated into a PX program, which is then compiled into a Verilog module using the SDNet flow. SDNet also produces a verification environment.

2.4.3 The NetFPGA Platform

The NetFPGA (Networked FPGA) project is a teaching and research tool designed to allow packets to be processed at line-rate in programmable hard-ware. It consists of four components: boards, tools and reference designs, a community of developers and contributed projects. The SUME board that was used in this project is the latest product in the NetFPGA hardware family.

Figure 2.2 depicts a block diagram of the canonical NetFPGA reference design which is used for switches, NICs, and IPv4 routers. It consists of four 10G SFP+ input/output ports along with one DMA interface for the CPU path. The NetFPGA data path consists of three main components: Input Arbiter, Output Port Lookup, and Output Queues. The Input Arbiter admits packets from the ports into the data path, towards the Output Port Lookup Module, where the main packet processing occurs and an output port is selected. The Output Queues buffer packets while they wait to be sent

to the outputs. The core data path uses a 256-bit wide bus and runs sufficiently fast at 200 MHz to support an aggregate of 40 Gb/s from all four SFP+ ports.

The limitation of this platform is that it requires a substantial knowledge in both hardware design and networking, with programs written in Verilog or VHDL. To overcome this, the P4→NetFPGA workflow was created to make it much easier to process packets in hardware and prototype new systems without being bogged down in hardware development.

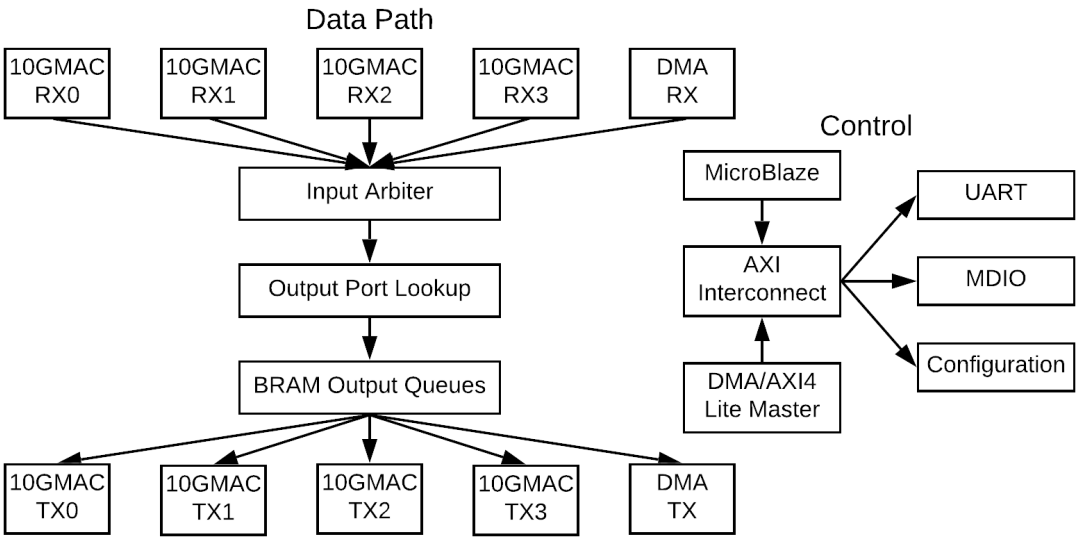

Figure 2.2: A block diagram of the NetFPGA reference design.

2.4.4 The P4→NetFPGA Workflow

The *SimpleSumeSwitch* (SSS) is the P4 architecture that is currently defined for the NetFPGA SUME board. The architecture consists of a single parser, single match-action pipeline, and single deparser, as shown in Figure **??**.

2.4.5 High-Level Architecture

Network Level

System Level

The

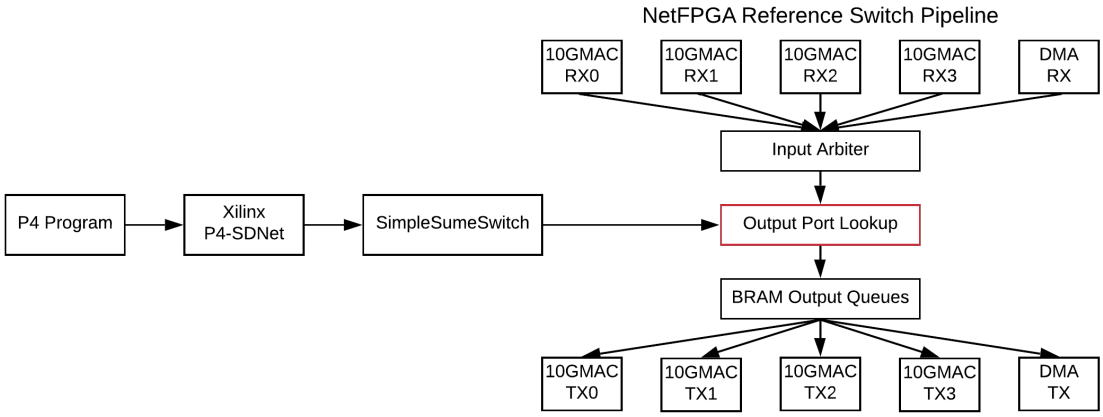

Figure 2.3: The automated P4→NetFPGA compilation flow. P4 programs are compiled into an HDL instance of the SimpleSumeSwitch architecture, which is then used to replace the Output Port Lookup module in the NetFPGA Reference Switch Design.

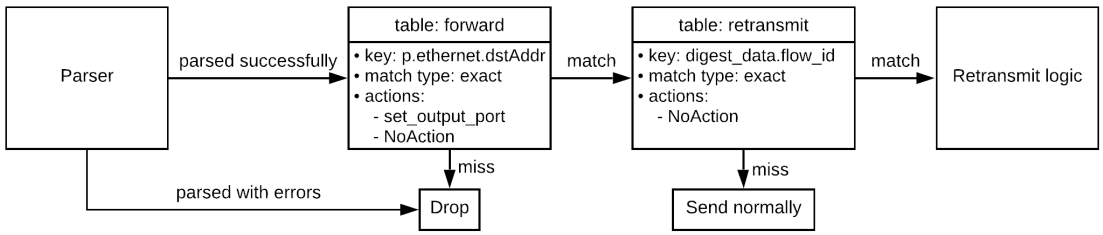

Figure 2.4: Test

2.4.6 Project Workflow

Figure 2.4 shows the workflow for this project, according to the requirement analysis.

I will follow the *spiral development model* [16] with an iteration count equal to the number of major functionalities to add. This allows for continual implementation, testing and integration of the different functionalities.

2.4.7 Risk Analysis

The P4→NetFPGA workflow is a complex platform that required the knowledge of a multitude of languages, with limited documentation [17] and community support [18]. A potential risk for the project was the difficulty of being sufficiently proficient with the platform to modify its core components and hence the inability to implement the design. Complete failure to do so was unlikely, but it could have consumed a significant amount of development time. As suggested by the spiral development model [16], this

high-risk part was scheduled early and some "catch-up" time was allocated in the project timetable in case it caused significant delays.

2.4.8 Backup Plan

Throughout the project development, I made sure to follow good backup procedure by keeping local weekly backups of my project using Time Machine for macOS. This provides recent history through incremental backups. I ensured additional remote storage by backing up with Microsoft OneDrive and Git, which also provided version control.

Chapter 3

Implementation

I give the overview of the project repository. I move on to explain the

3.1 Repository Overview

```
P4-NetFPGA
├── project
│   ├── simple_sume_switch
│   │   ├── hw
│   │   │   └── hdl
│   │   │       └── nf_datapath.v*
│   │   └── test
│   │       └── sim_switch_default
│   │           └── run.py*
│   ├── src
│   │   ├── tcp_retransmit.p4*
│   │   └── commands.txt*
│   ├── testdata
│   │   ├── gen_testdata.py*
│   │   ├── digest_data.py*
│   │   └── sss_sdnet_tuples.py*
│   └── templates
│       └── externs
│           └── <externs-name>
│               └── hdl
│                   └── <externs-name>_template.v*
└── lib
    └── hw
        ├── contrib
        │   └── cores
        │       └── sss_cache_queues_v1_0_0*
        └── std
            └── cores
                └── output_arbiter_v1_0_0*
```

This project will work mainly with a NetFPGA SUME board [19], using P4 programming

language. I will be using the P4-NetFPGA workflow, which provides infrastructure to compile P4 programs to NetFPGA [17]. Apart from that, everything else will be built from scratch.

3.2 Software Implementation

3.2.1 The Parser

Parsers are functions that map packets into headers and metadata, written in a state machine style. A parser is defined by:

```
// Parser Implementation
@Xilinx_MaxPacketRegion(8192)
parser TopParser(packet_in b,
                 out Parsed_packet p,
                 out user_metadata_t user_metadata,
                 out digest_data_t digest_data,
                 inout sume_metadata_t sume_metadata) {

      /*** state machine description ***/

}
```

where `@Xilinx_MaxPacketRegion(8192)` is Xilinx P4-SDNet's additional annotation for parser/deparser that declares the largest packet size (in bits) the parser/deparser needs to support.

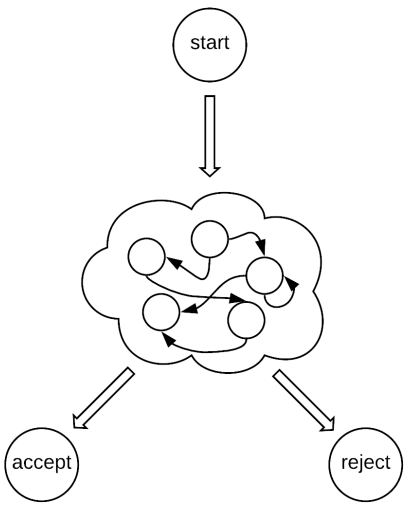

Figure 3.1: Parser general FSM structure.

Figure 3.1 illustrates the general structure of a parser state machine, which includes three predefined states:

- `start` – the start state.
- `accept` – indicating successful parsing.
- `reject` – indicating a parsing failure.

and other internal states that may be defined by the user. The `start` state is part of the parser, while the `accept` and `reject` states are distinct from the user-defined states and are logically outside of the parser.

An architecture must specify the behaviour when the `accept` and `reject` states are reached. For example, an architecture may specify that all packets reaching the `reject` state are dropped without further processing. Alternatively, it may specify that such packets are passed to the next block after the parser, with intrinsic metadata indicating that the parser reached the `reject` state, along with the error recorded. The SimpleSumeSwitch architecture adopts the former.

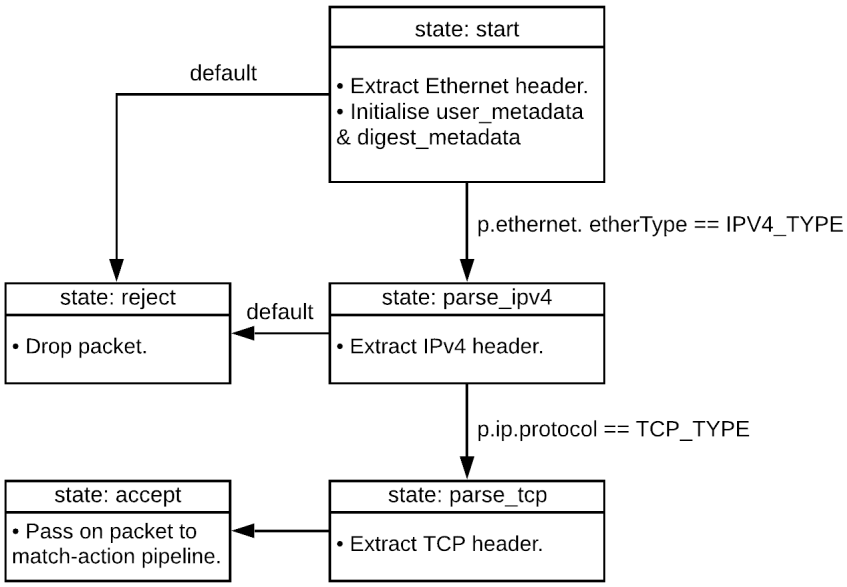

Figure 3.2: The FSM of the design.

Figure 3.2 describes the FSM structure of my parser, in which I defined two additional states `parse_ipv4` and `parse_tcp`:

The P4 `select` statement is used to branch in a parser. It is similar to `case` statement in C or Java, but without "fall-through behaviour"—i.e., `break` statements are not needed. A `parse_ethernet` state could be defined similarly, but I decided to include the parsing of the Ethernet header within the `start` state, together with initialising the metadata, for simplicity. Here, the `parse_ipv4` state extracts the packet's IPv4 header,

```
state parse_ipv4 {
  b.extract(p.ip);
  transition select(p.ip.protocol) {
    TCP_TYPE: parse_tcp;
    default: reject;
  }
}
```

Figure 3.3: The definition of `parse_ipv4` state.

```
state parse_tcp {
  b.extract(p.tcp);
  transition accept;
}
```

Figure 3.4: The definition of `parse_tcp` state.

looks at the `protocol` field and makes a transition to the `parse_tcp` state only if it is `TCP_TYPE` which is defined to be 6. Otherwise, the packet is rejected. The `parse_tcp` state simply extracts the TCP header of the packet and made a transits to the `accept` state, where the packet will be passed to the match-action pipeline.

3.2.2 The Match-Action Pipeline

A match-action pipeline can be defined by the following code sequence:

```
// Match-action pipeline
control TopPipe(inout Parsed_packet p,
                inout sume_metadata_t sume_metadata,
                inout digest_data_t digest_data,
                inout user_metadata_t user_metadata) {
  /** actions **/
  /** tables **/
  /** logic **/
}
```

This is where the header processing logic is implemented, using a data-dependent sequence of match-action unit invocations and other imperative constructs (indicated by the **`control`** keyword). This pipeline receives four inputs: the parsed packet `p`, the SUME metadata, the digest data and the user metadata. The direction `inout` indicates that the parameters are both an input and an output. Thus, their values, including the fields in the headers of packet `p`, can be modified. Nonetheless, the user metadata was not used in this design.

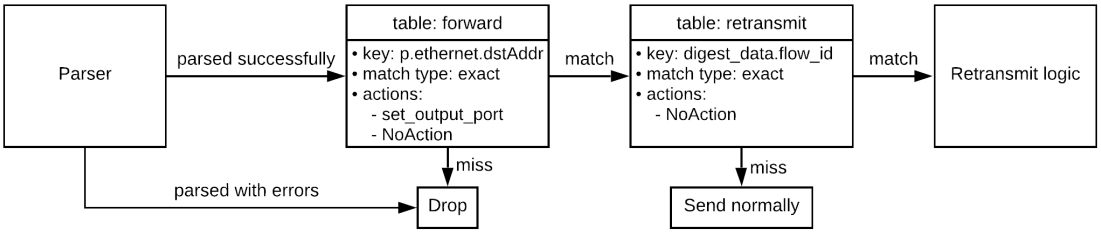

Figure 3.5: A packet processing program describing a simple L2/L3 IPv4 switch.

Figure 3.5 illustrates the control flow program acting on a packet going through our

match-action pipeline, which comprises two match-action units (represented by the P4 `table` keyword): `forward` and `retransmit`. The first table uses the Ethernet destination address to determine the output port for the next hop. If this lookup fails, the packet is dropped (by assigning `sume_metadata.dst_port` to 0). The second table checks the computed `digest_data.flow_id`: if it matches our flow of interest, the packet will be monitored to assist the fast retransmit of TCP congestion control. Otherwise, the packet will just be sent normally. A packet will be modified by a series of `actions`: `set_output_port` sets the output port on the SUME board for packets whose Ethernet destination address matches what was defined in the first table, and `compute_flow_id` computes the flow number of the packet for the second table to look up. `cache_write`, `cache_read` and `cache_drop` modify `digest_data.tuser` to signal the cache queue to cache, retransmit and drop the packet at the head of the queue respectively.

In summary, the switch will perform the following tasks in the SSS module:

- Receive and parse packet from the sender.
- Look up the Ethernet destination address to determine the output port. Drop on a miss.
- Compute the flow number of the packet.
- Look up the flow number of the packet to determine if it should be monitored. Send normally on a miss.
- Set `digest_data.tuser` and/or set the `ACK` flag in the TCP header appropriately.
- Construct the final packet and send it to the receiver.

3.2.3 The Deparser

The inverse of parsing is deparsing, or packet assembly, where the outgoing packet is constructed by reassembling of the headers as computed by the pipeline. P4 does not provide a separate language for packet deparsing; deparsing is done in a `control` block that has at least one parameter of type `packet_out`. The advantage of this approach is that it makes deparsing explicit, but decouples it from parsing.

The following code block, which implements the deparser of the switch, first writes an Ethernet header, followed by an IPv4 header, and then a TCP header into a `packet_out`. Since emitting a header appends the header to the `packet_out` only if the header is

valid, P4 first checks the validity of the headers before serialising them.

```
// Deparser Implementation
@Xilinx_MaxPacketRegion(8192)
control TopDeparser(packet_out b,
                    in Parsed_packet p,
                    in user_metadata_t user_metadata,
                    inout digest_data_t digest_data,
                    inout sume_metadata_t sume_metadata) {
    apply {
      b.emit(p.ethernet);
      b.emit(p.ip);
      b.emit(p.tcp);
    }
}
```

3.2.4 The Externs

P4 externs are platform-specific functions that are not described in the core P4 language—some sort of "black boxes" for P4 programs. They can either be **stateless**—reinitialised for each packet—or **stateful**—keeping states between packets. A set of supported externs is defined by the architecture in the `templates` folder. In this project, the following

An important feature of P4→NetFPGA externs is that each stateful atom (i.e. register) can only be accessed *one* time in the P4 code. Multiple calls to the extern function will generate multiple instances of the atom and thus will likely give unexpected results. This complicates my

3.3 Hardware Implementation

3.3.1 The Cache Queue

3.3.2 The Output Arbiter

The P4→NetFPGA platform comes with an input arbiter, which performs the following functions:

- It receives packets from one of the physical input Ethernet ports, from the control plane, or from the input recirculation port.
- For packets received from Ethernet ports, the block computes the Ethernet trailer

checksum and verifies it. If the checksum does not match, the packet is discarded. If the checksum does match, it is removed from the packet payload.

- Receiving a packet involves running an arbitration algorithm if multiple packets are available.

- If the arbiter block is busy processing a previous packet and no queue space is available, input ports may drop arriving packets, without indicating the fact that the packets were dropped in any way.

- After receiving a packet, the arbiter block sets the inCtrl.inputPort value that is an input to the match-action pipeline with the identity of the input port where the packet originated. Physical Ethernet ports are numbered 0 to 7, while the input recirculation port has a number 13 and the CPU port has the number 14.

For our architecture, since we have two queues—the output queue and the cache queue—we would require an "output" arbiter for each of the five ports.

Chapter 4

Evaluation

In this chapter, I show that my implementation works across three different levels. I then evaluate the performance of the design. Finally, I compare the performance of my design to existing TCP fast retransmit mechanism.

Chapter 5

Conclusion

5.1 Accomplishments

Overall, the project achieved its aim of implementing and evaluating a programmable switch that is capable of assisting the fast retransmit process of TCP. The switch functionalities were evaluated at three different stages: a software simulation, a SUME simulation and a hardware test. A

An evaluation for the switch was also provided as comparing to TCP

With the benefit of hindsight, I would have implemented the architecture prior to starting the project and used it as the starting point. This would have enabled me to focus more on evaluating and give more time to explore useful extensions.

5.2 Future Work

Many promising avenues for further improvement were not explored due to time constraints:

- **Supporting multiple packet sizes**. The current design only supports a single packet size. It would definitely be more useful if the design could support a
- **Supporting multiple flows**. Embedding schemes that withstand transcoding would be useful for things like communication over social media. Services such as YouTube, Facebook and Tumblr transcode user-uploaded videos before presenting them to other users, destroying any payload hidden in motion vectors. Embedding algorithms that make use of error correcting codes or redundant encoding may be better able to resist this.
- **User INteface**. The current CLI could be replaced by a more novice-friendly

GUI, providing helpful guidance for inexperienced users who want to start using covert communication. This could allow

adaptively installing and removing flows to monitor, as well as the ability to configure the flow.It could include a privacy advice and an automatic algorithm recommendation based on a set of predefined use-cases, the payload size and the video embedding capacity. An HCI trial could be conducted to evaluate whether the interface helps the users achieve the required communication secrecy level while being educative and easy to use.

Closing Remarks

This project has been a fascinating opportunity to explore the field of computer networking, especially high-performance networking, comprehend and appreciate the intricacy of TCP congestion control mechanism and the potential of data plane programmability. The project has achieved most of its goals and attempted to investigate and evaluate a modification to assist TCP fast retransmit algorithm, providing a starting point for future improvements. This project has also contributed to my personal development by improving my software engineering and technical writing skills.

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