Computer-Aided Design for VLSI Design

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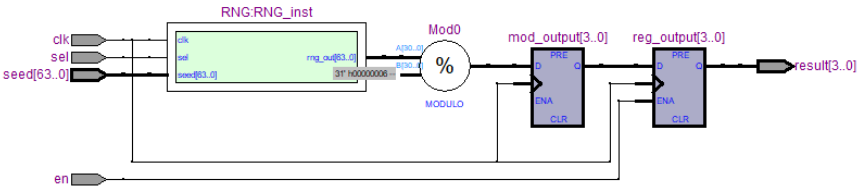
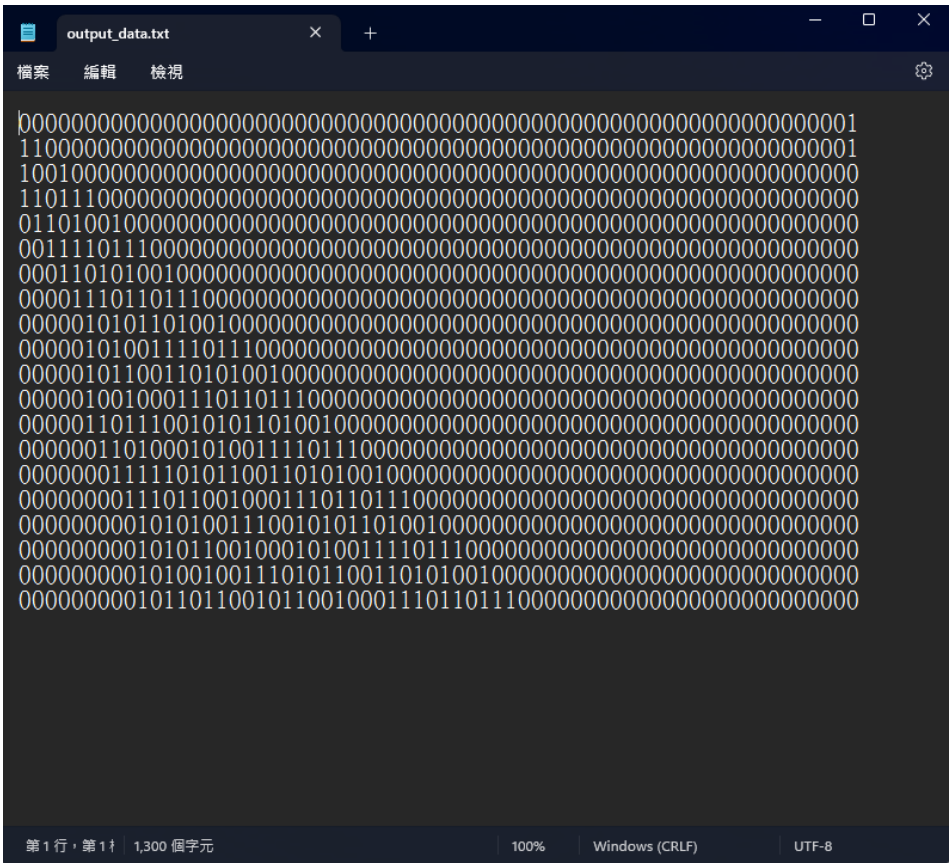
1. Provide a simple explanation of your code.
   在這份作業，我應用三個 VHDL file，分別是 CA/ RNG / My_Optional
   我將 My_Optional 設為 Top-Level-Entity，以下是我的 My_Optional 的 Code、RTL Viewer 以及 RNG ModelSim 後的 outputdata.txt file




```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity My_Optional is
port(
     clk, en: in std_logic;
     sel: in std_logic;
     seed: in std_logic_vector(63 downto 0);
     result: out std_logic_vector(3 downto 0));
end My_Optional;

architecture behavior of My_Optional is
    component RNG is
        port(seed : in std_logic_vector(63 downto 0);
             clk, sel : in std_logic;
            rng_out : out std_logic_vector(63 downto 0)
           );
    end component;

    signal rng_output : std_logic_vector(63 downto 0);
    signal mod_output : std_logic_vector(3 downto 0);

    signal reg_output : std_logic_vector(3 downto 0);

begin
    RNG_inst : RNG port map(seed => seed,
                            clk => clk,
                            sel => sel,
                            rng_out => rng_output);
    process(clk)
```

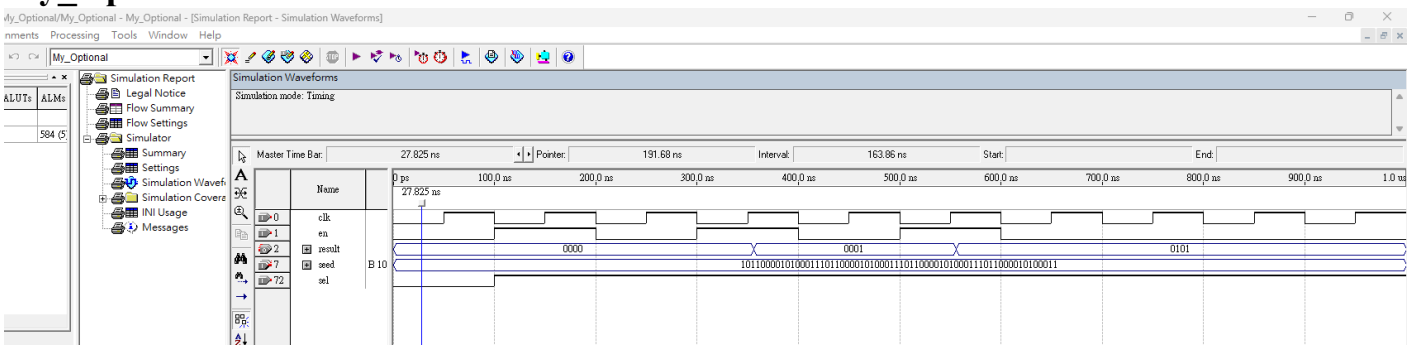
```
      variable dec_value : integer;
    begin
      if rising_edge(clk) then
         dec_value := to_integer(unsigned(rng_output));

         mod_output <= std_logic_vector(to_unsigned(dec_value mod 6,
mod_output'length));
      end if;
    end process;

    process(clk)
    begin
     if rising_edge(clk) then
      if en='1' then
         reg_output <= mod_output;
       end if;
    end if;
    end process;
    result <= reg_output;
end behavior;
```

RNG ModelSim 後的 outputdata.txt file

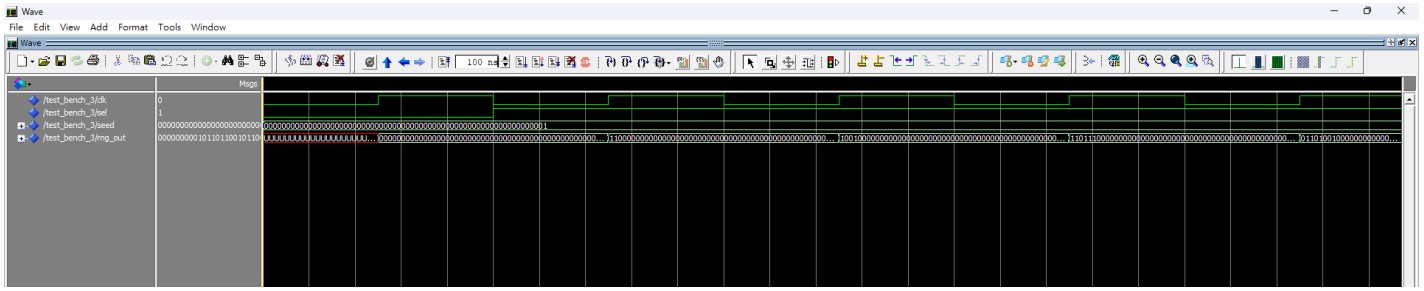


2. Waveform diagram here (Simulation Results)

My_Optional:



RNG:



3. Reflections and discussions

謝謝助教/教授出了加分作業讓我們不只加分還可以學習如何應用 ModelSim 去實作 test bench，在投影片中教授的教學十分清楚，透過步驟自己去實作出來還有收穫，也應用之前作業的 component 以及設定 top-level entity 方法讓專案可以成功執行。在 electronic die system 撰寫過程也讓我更加熟悉語法的應用以及 rising edge 的用途!