Computer-Aided Design for VLSI Design

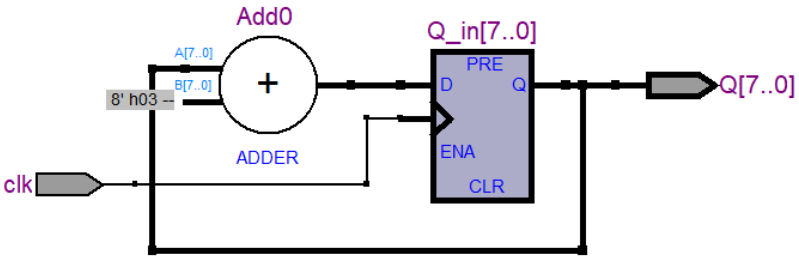
Homework2（Student ID: 61047046S｜Name: 鄭琮達）

1. Provide a simple explanation of your code.

   在作業中我使用到 use ieee.std_logic_unsigned.all;來幫我解決"+"只能用在整數的問題，在 structural model 使用 component 語法合併我的 D-FF 以及 Adder。以下為我的 code 以及 RTL Viewer

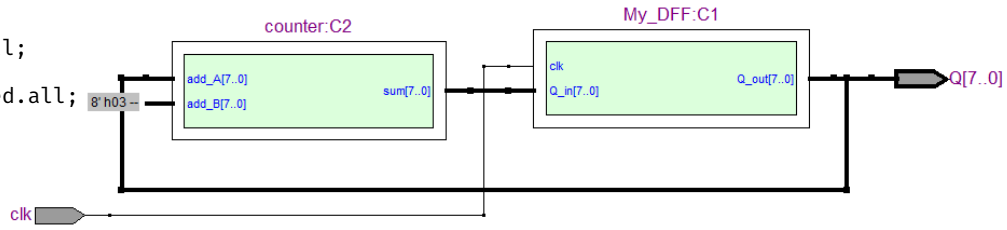
   (a) Behavior Model

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;



entity My_count is
port(
      clk: in std_logic;
      Q: out std_logic_vector(7 downto 0));
end My_count;

architecture behavior of  My_count is
signal Q_in: std_logic_vector(7 downto 0) := "00000000";
begin
     process(clk)
     begin
      if(clk'EVENT and clk='1') then
        Q_in <= Q_in + "011";
      end if;
     end process;
     Q <= Q_in;
end behavior;
```



(b) Structural Model

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;


entity My_struct_count is
port(
        clk: in std_logic;
        Q:out std_logic_vector(7 downto 0));
end My_struct_count;

architecture structural of My_struct_count is
  component My_DFF
    port(
      clk: in std_logic;
      Q_in: in std_logic_vector(7 downto 0);
      Q_out: out std_logic_vector(7 downto 0)
    );
  end component;

  component counter
    port(
      add_A: in std_logic_vector(7 downto 0);
      add_B: in std_logic_vector(7 downto 0);
      sum : out std_logic_vector(7 downto 0)
    );
  end component;

  signal Q_in, Q_out : std_logic_vector(7 downto 0);
  constant B : std_logic_vector(7 downto 0) := "00000011";
begin
  C1: My_DFF port map(clk, Q_in, Q_out);
  C2: counter port map(Q_out, B, Q_in);
  Q <= Q_out;
end structural;
```

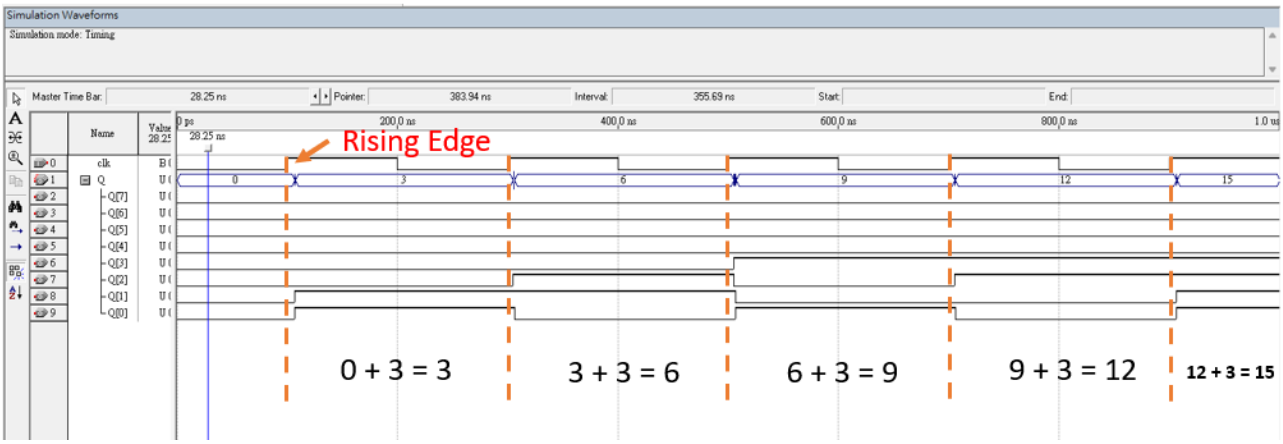


```
library ieee;
use ieee.std_logic_1164.all;

entity My_DFF is
port(
      clk: in std_logic;
      Q_in: in std_logic_vector(7 downto 0);
      Q_out: out std_logic_vector(7 downto 0));
end My_DFF;

architecture behavior of My_DFF is
begin
     process(clk)
          begin
               if(clk'EVENT and clk='1') then
                    Q_out <= Q_in;
          end if;
     end process;
end behavior;
```

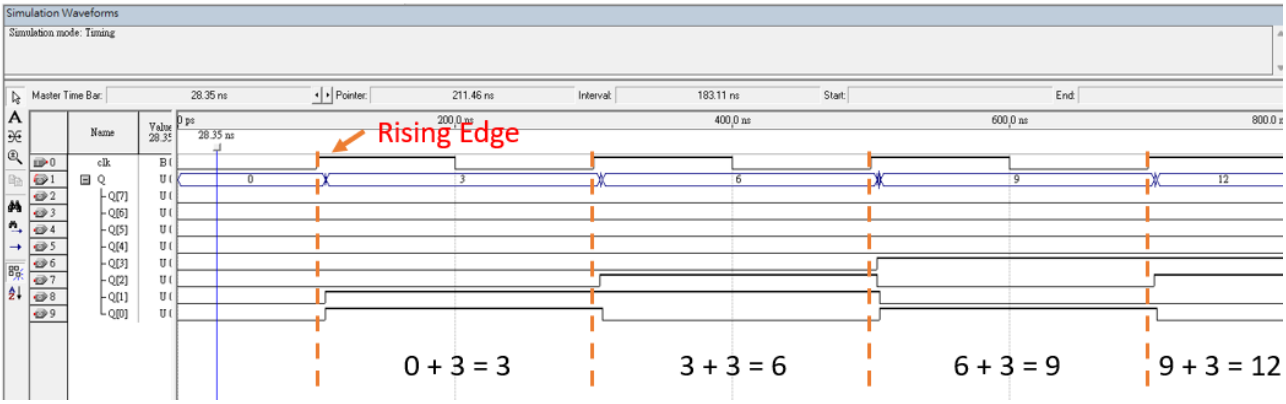
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity counter is
port(
       add_A: in std_logic_vector(7 downto 0);
       add_B: in std_logic_vector(7 downto 0);
       sum : out std_logic_vector(7 downto 0));
end counter;

architecture behavior of counter is
begin
     process(add_A)
          begin
               sum <= add_A + add_B;
     end process;
end behavior;
```

2. Waveform diagram here (Simulation Results)

(a)Behavior Model



(b)Structural Model



3. Reflections and discussions

謝謝教授以及助教提供作業讓我學習 behavior model 以及 structural model 的使用方式，透過 Rising Edge 的方法來設計加法器，在這份作業上，我學會不僅可以+3，也可以使程式加特定的數字。以及利用教授課堂提醒到的 std_logic_unsigned 可以用來解決非整數加法運算的問題。