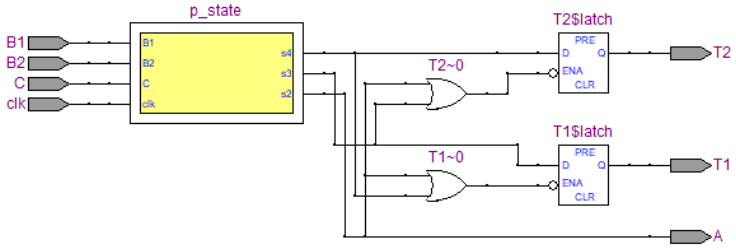
Computer-Aided Design for VLSI Design

Homework3（Student ID: 61247046S｜Name: 鄭琮達）

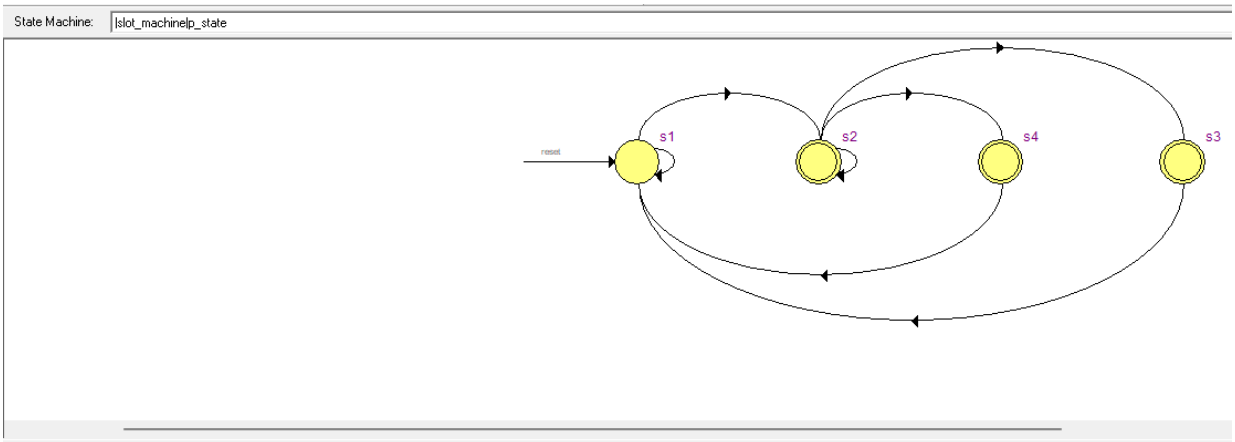
1. Provide a simple explanation of your code.

   在作業中我使用到 type four_state is (s1, s2, s3, s4);來定義一個新的數據類型”four_state”且包含四個可能狀態”s1”, “s2”, “s3”, “s4”。以下為我的 code 以及 RTL Viewer 以及 State Machine Viewer。

```
entity slot_machine is
port(
        C, B1, B2, clk: in bit;
        A, T1, T2:out bit);
end slot_machine;

architecture behavior of slot_machine is
 type four_state is (s1, s2, s3, s4);
 signal p_state, n_state: four_state;

begin
    process(clk)
    begin
        if clk'EVENT and clk='1' then
            p_state <= n_state;
        end if;
    end process;

    process(p_state, C)
    begin
        case p_state is
            when s1=>
                A <= '0';
                T1 <= '0';
                T2 <= '0';
                if C='1' then
                    n_state <= s2;
                else
```

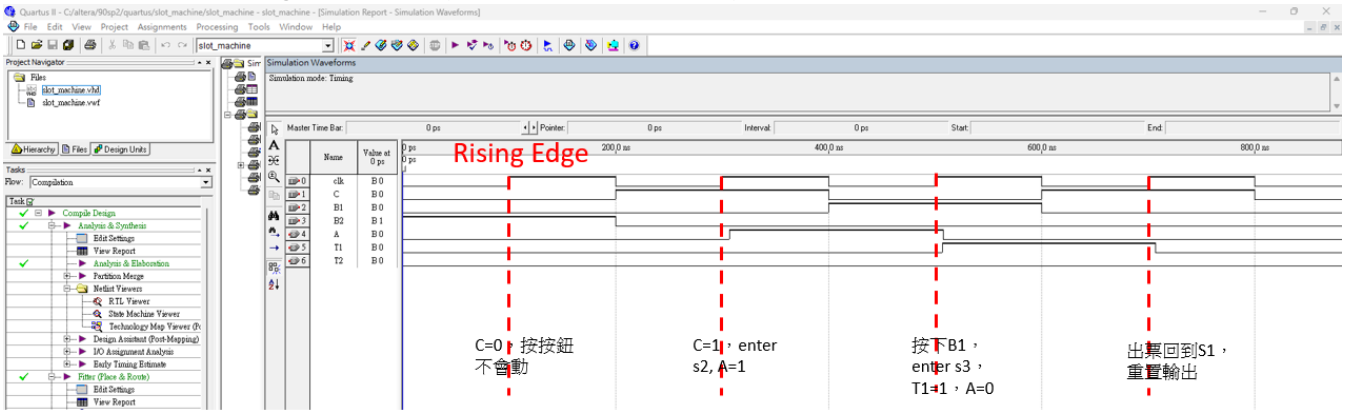


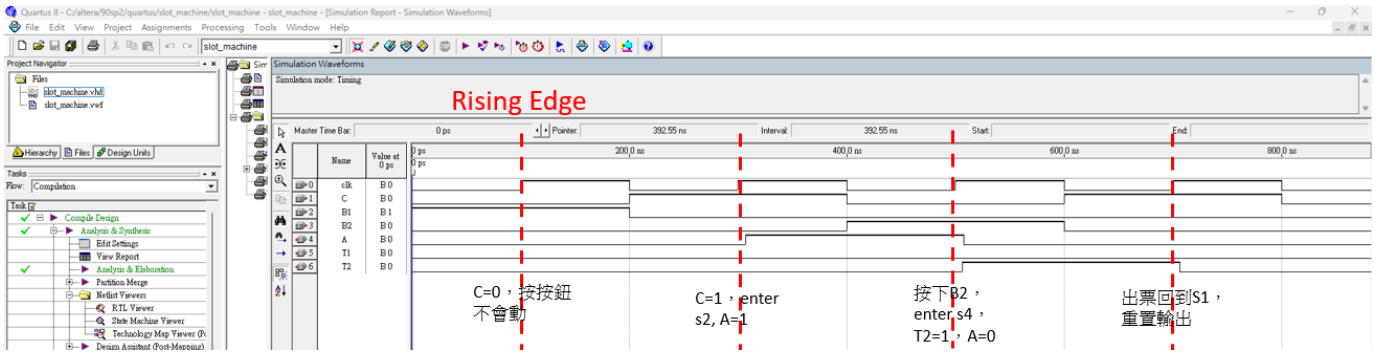
```
                n_state <= s1;
            end if;

        when s2=>
            A <= '1';
            if (B1='1' or (B1='1' and B2='1')) then
                n_state <= s3;
            elsif B2='1' then
                n_state <= s4;
            else
                n_state <= s2;
            end if;

        when s3=>
            A <= '0';
            T1 <= '1';
            n_state <= s1;

        when s4=>
            A <= '0';
            T2 <= '1';
            n_state <= s1;

    end case;
  end process;
end behavior;
```



	Source State	Destination State	Condition
1	s4	s1	
2	s3	s1	
3	s2	s4	(B2).(!B1)
4	s2	s3	(B1)
5	s2	s2	(!B2).(!B1)
6	s1	s2	(C)
7	s1	s1	(!C)

2. Waveform diagram here (Simulation Results)





3. Reflections and discussions

謝謝教授以及助教提供作業讓我學習 Type 自定義型態以及 case when 的使用方式，透過 Rising Edge 的方法來改變狀態，並且利用 case when 的語法，讓狀態依照條件判斷前進下去，最後透過重置回到原點，形成一個 FSM。