ECE 372A Fall 2015 - Lecture 13

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October 8, 2015

Outline

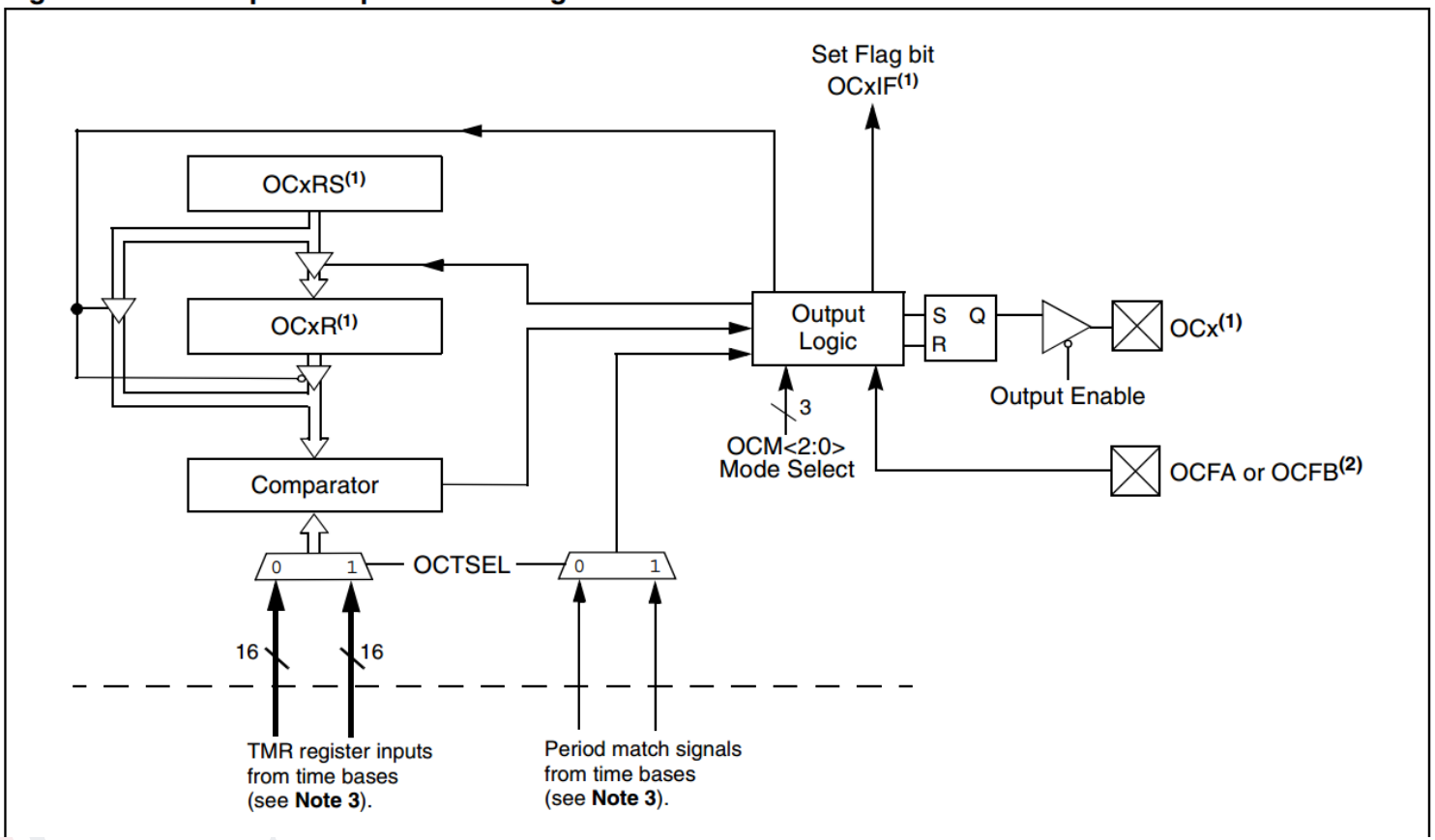
Output Compare Module

Reference Material

Section 16 in the PIC24F Family Reference Manual
Section 16 in the PIC32MX Data Sheet

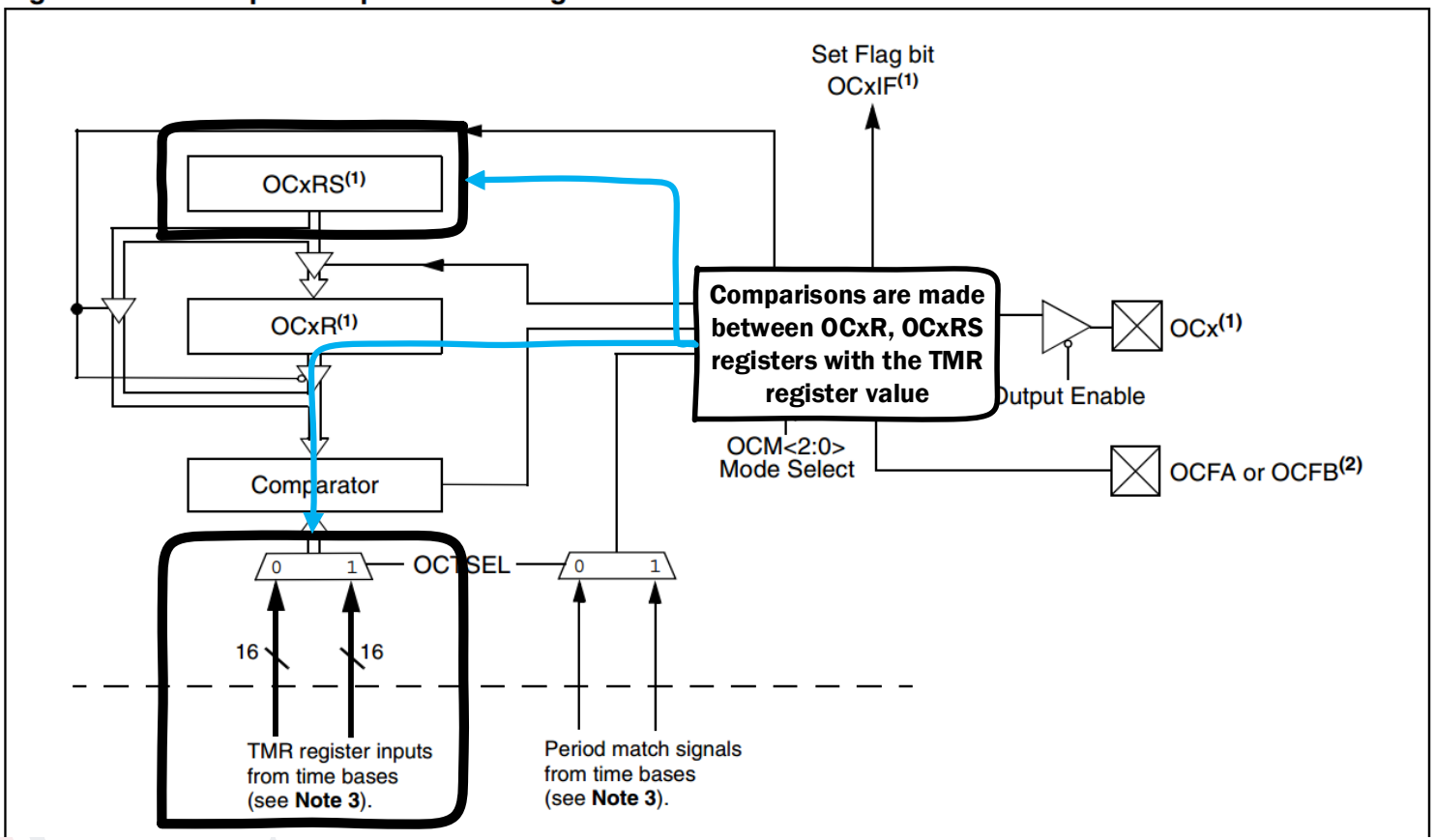
Output Compare Circuit

Figure 16-1: Output Compare Block Diagram



Output Compare Circuit

Figure 16-1: Output Compare Block Diagram



Output Compare Circuit

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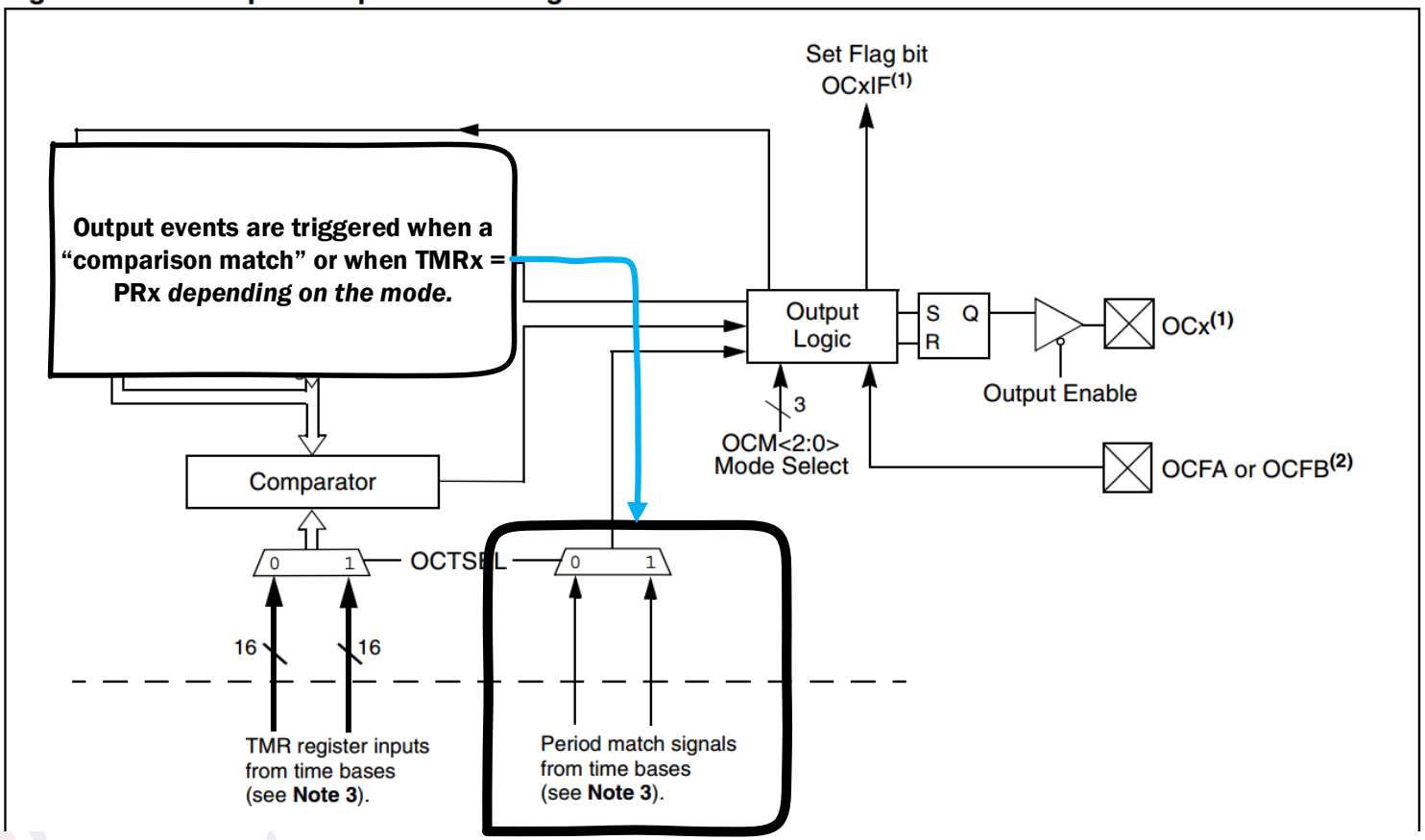
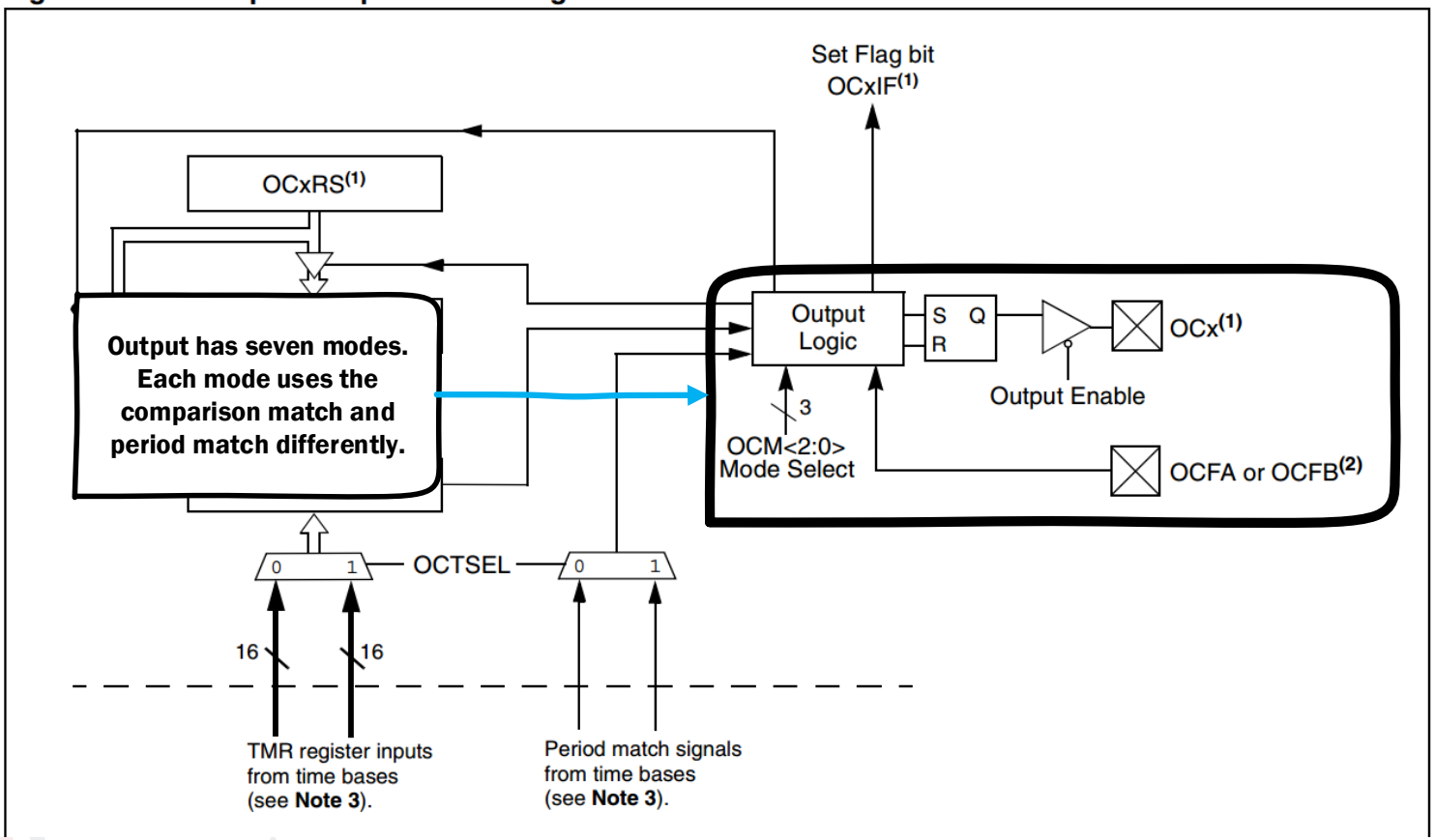


Output Compare Circuit

Figure 16-1: Output Compare Block Diagram



Output Compare Register

bit 2-0 **OCM<2:0>:** Output Compare x Mode Select bits

111 = PWM mode on OCx, Fault pin enabled
110 = PWM mode on OCx, Fault pin disabled
101 = Initialize OCx pin low, generate continuous output pulses on OCx pin
100 = Initialize OCx pin low, generate single output pulse on OCx pin
011 = Compare event toggles OCx pin
010 = Initialize OCx pin high, compare event forces OCx pin low
001 = Initialize OCx pin low, compare event forces OCx pin high
000 = Output compare channel is disabled

For PWM, do not use the fault pin

Output Compare Register

Other uses we will go over.

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OC Modes

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1. Single Compare Match mode (Only OCxR is involved)

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2. Dual Compare Match mode (OCxR and OCxRS is involved)

OC Modes

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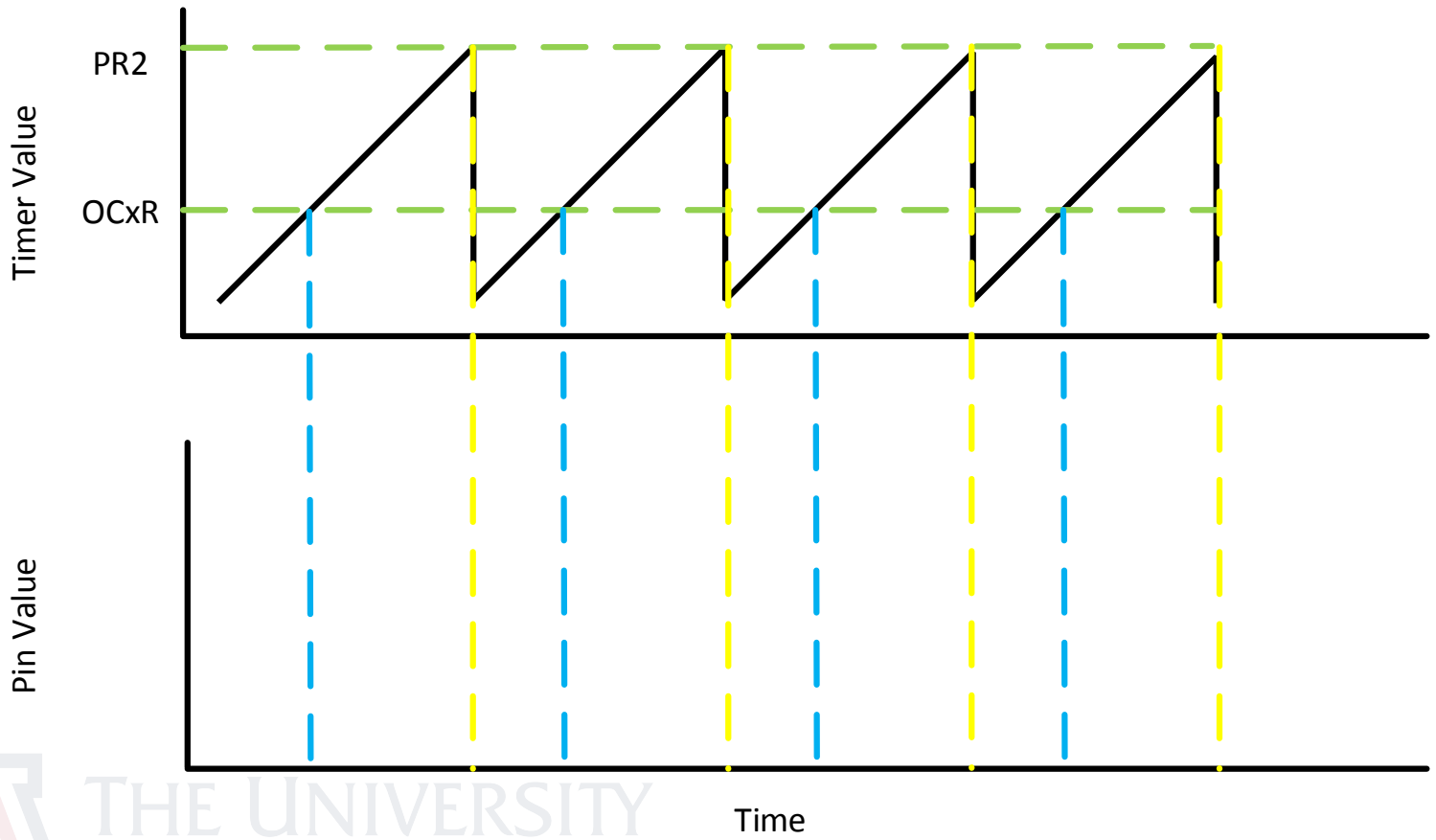
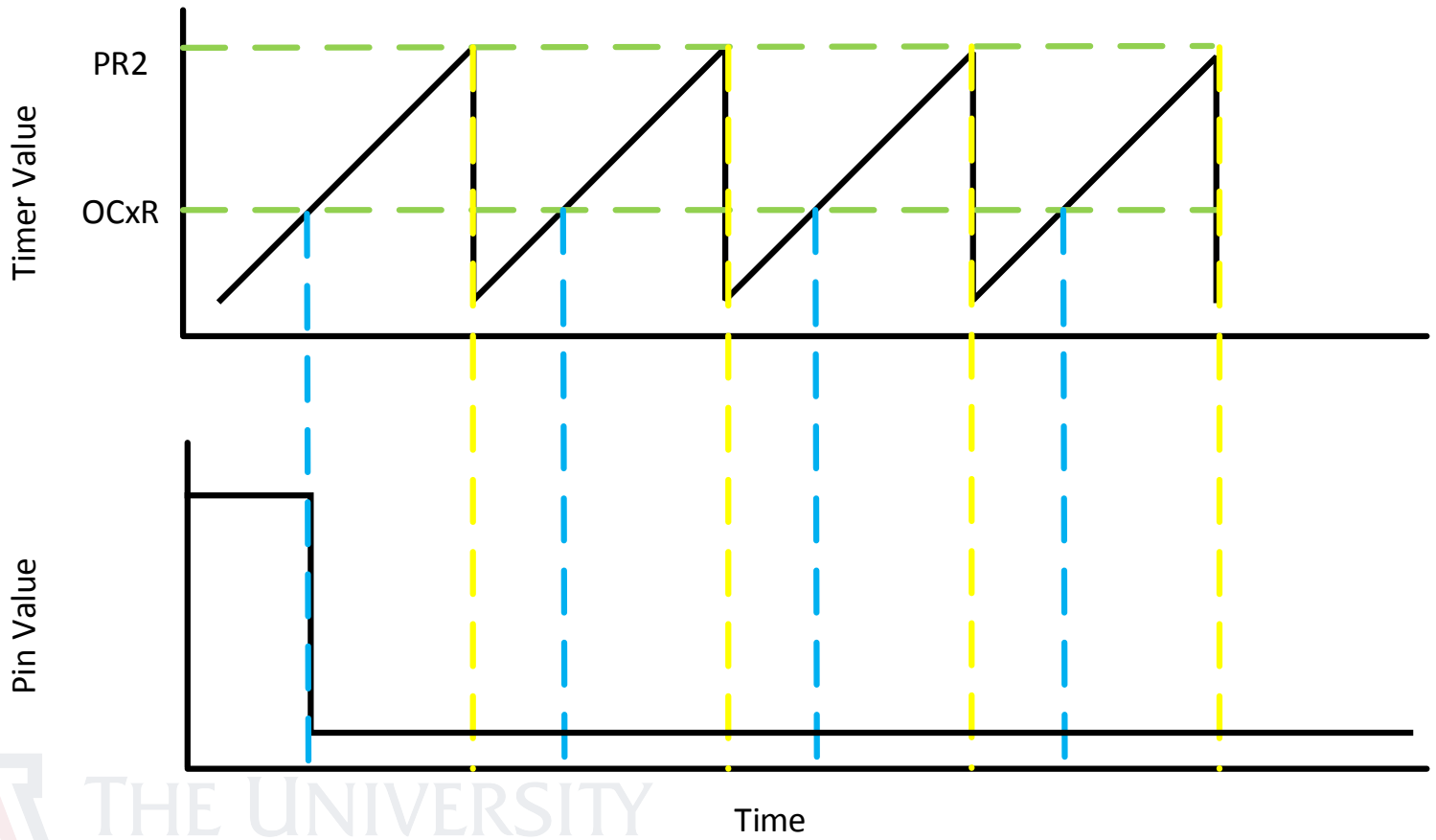
1. Single Compare Match mode (Only OCxR is involved)
2. Dual Compare Match mode (OCxR and OCxRS is involved)
3. PWM mode (previously covered)

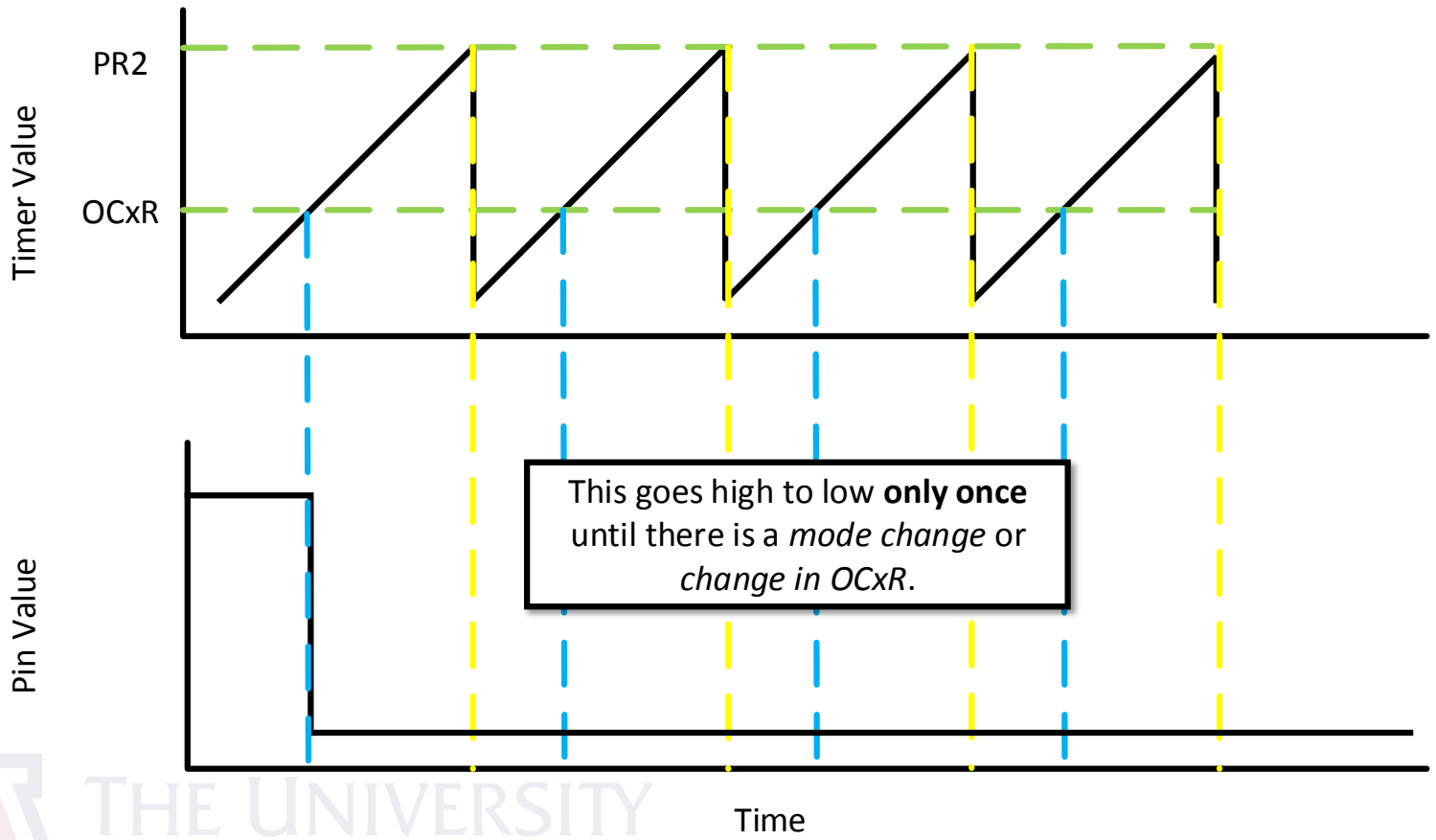
Single Compare



Single Compare



Single Compare



Single Compare Modes

Single Compare Modes

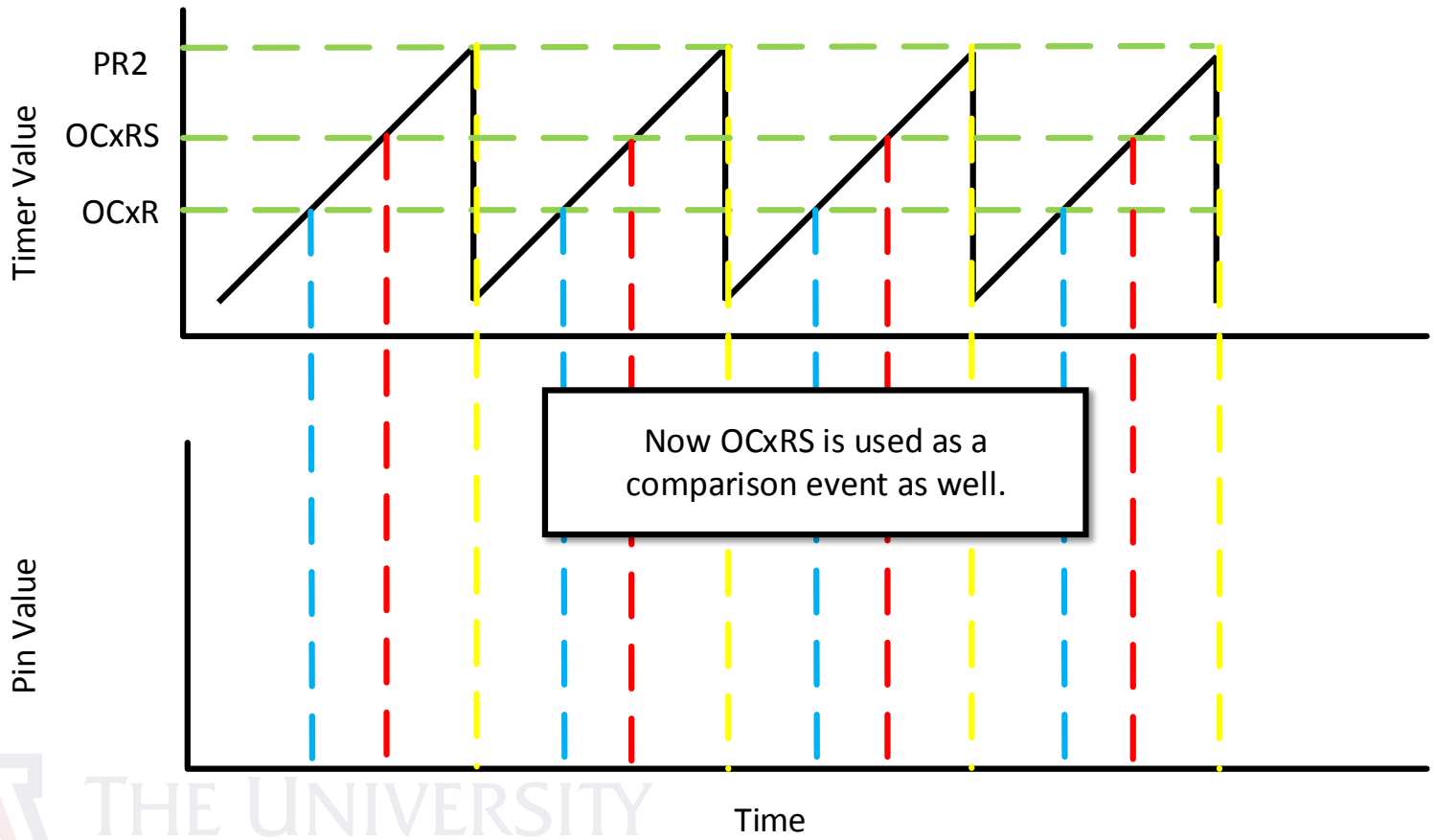
1. From high to low
2. From low to high

Single Compare Modes

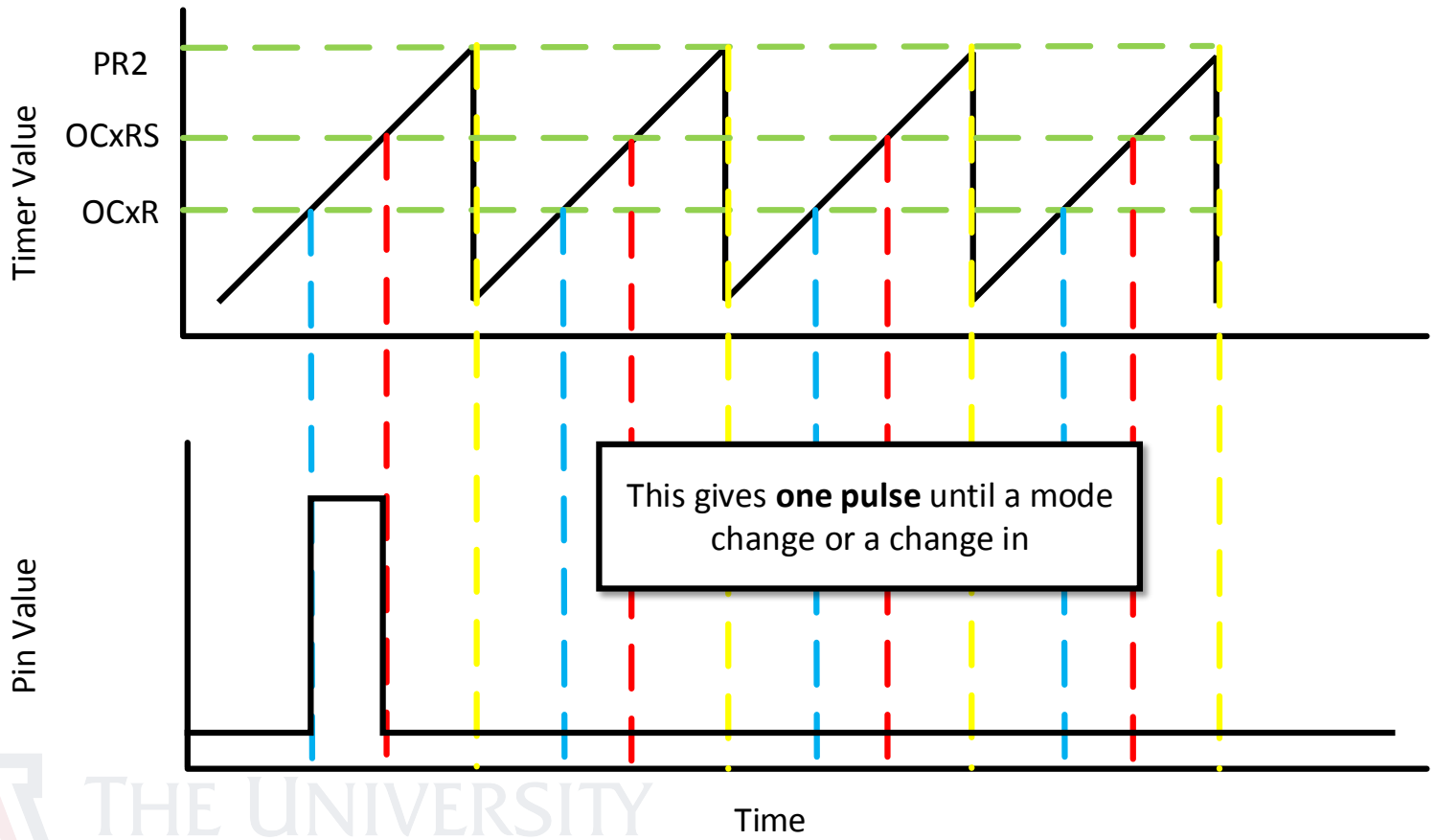
Single Compare Modes

1. From high to low
2. From low to high
3. Toggle

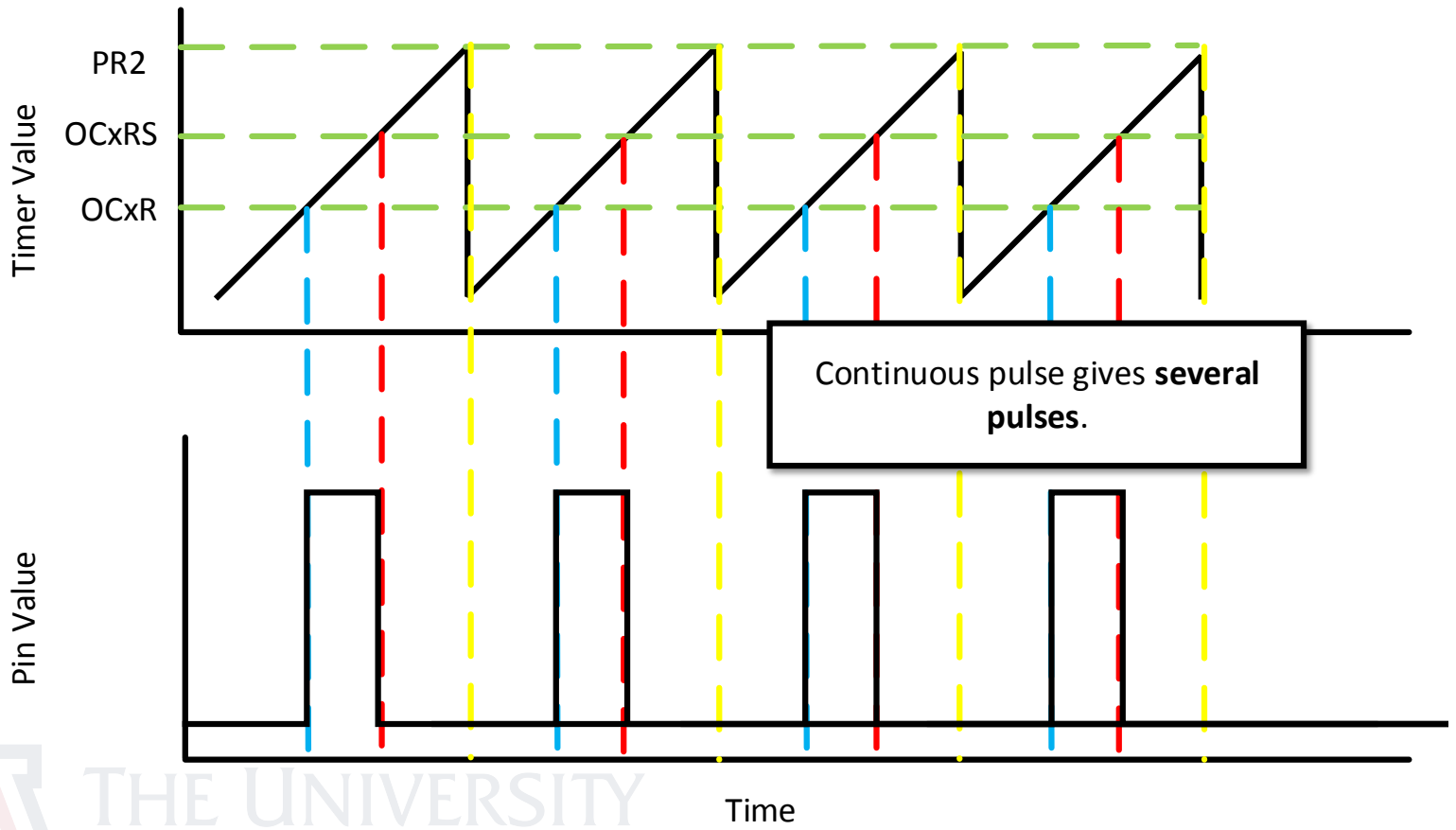
Dual Compare Single Pulse



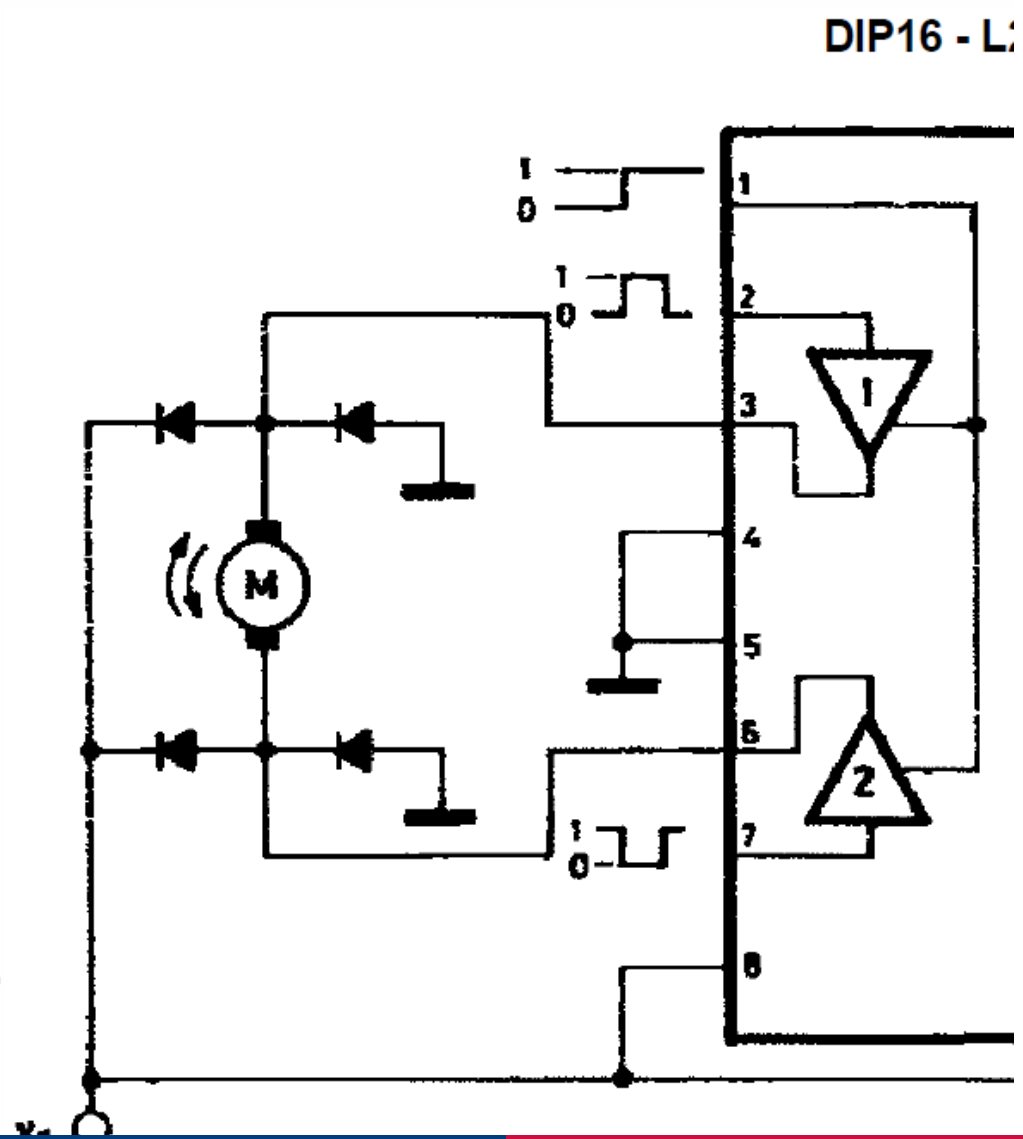
Dual Compare Single Pulse



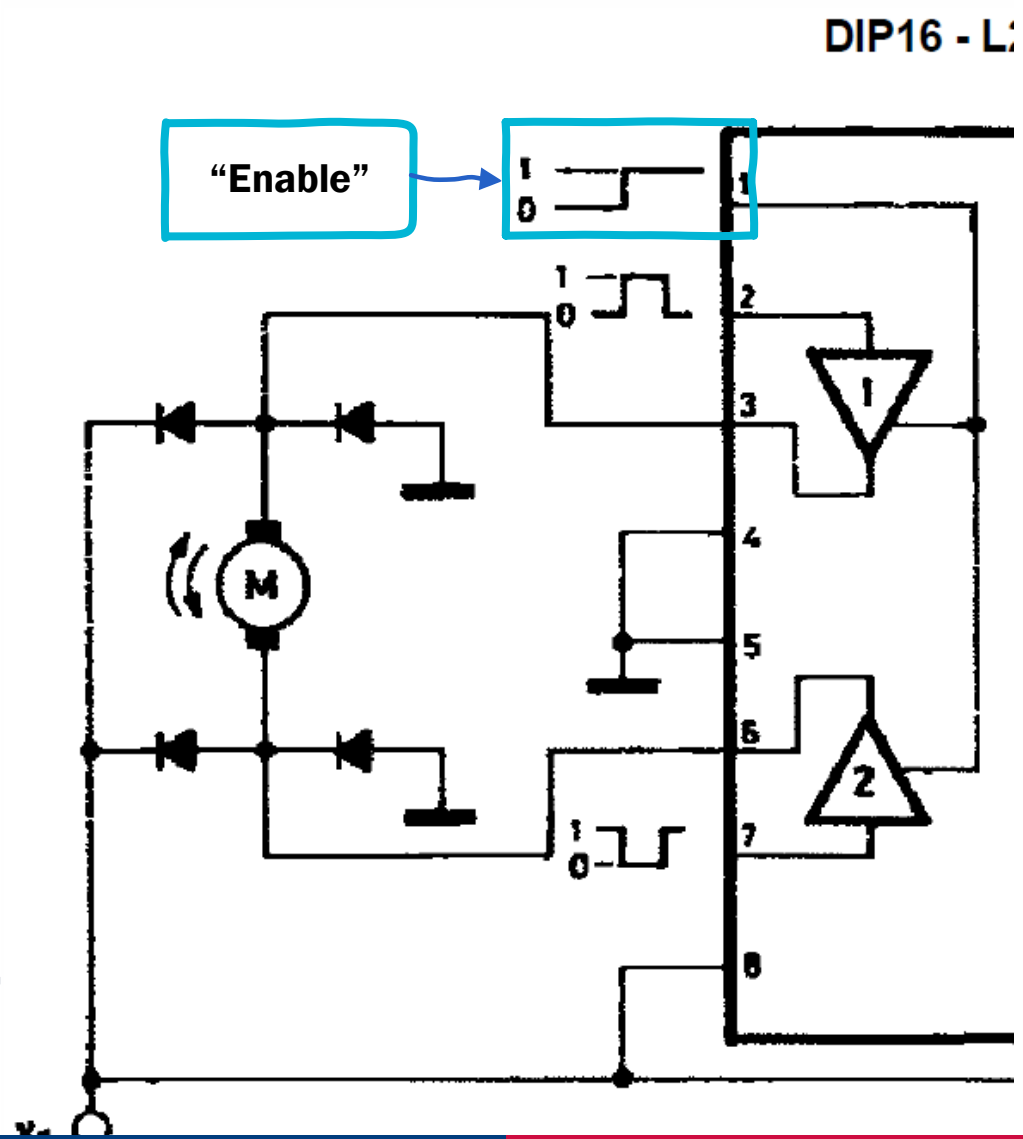
Dual Compare Single Pulse



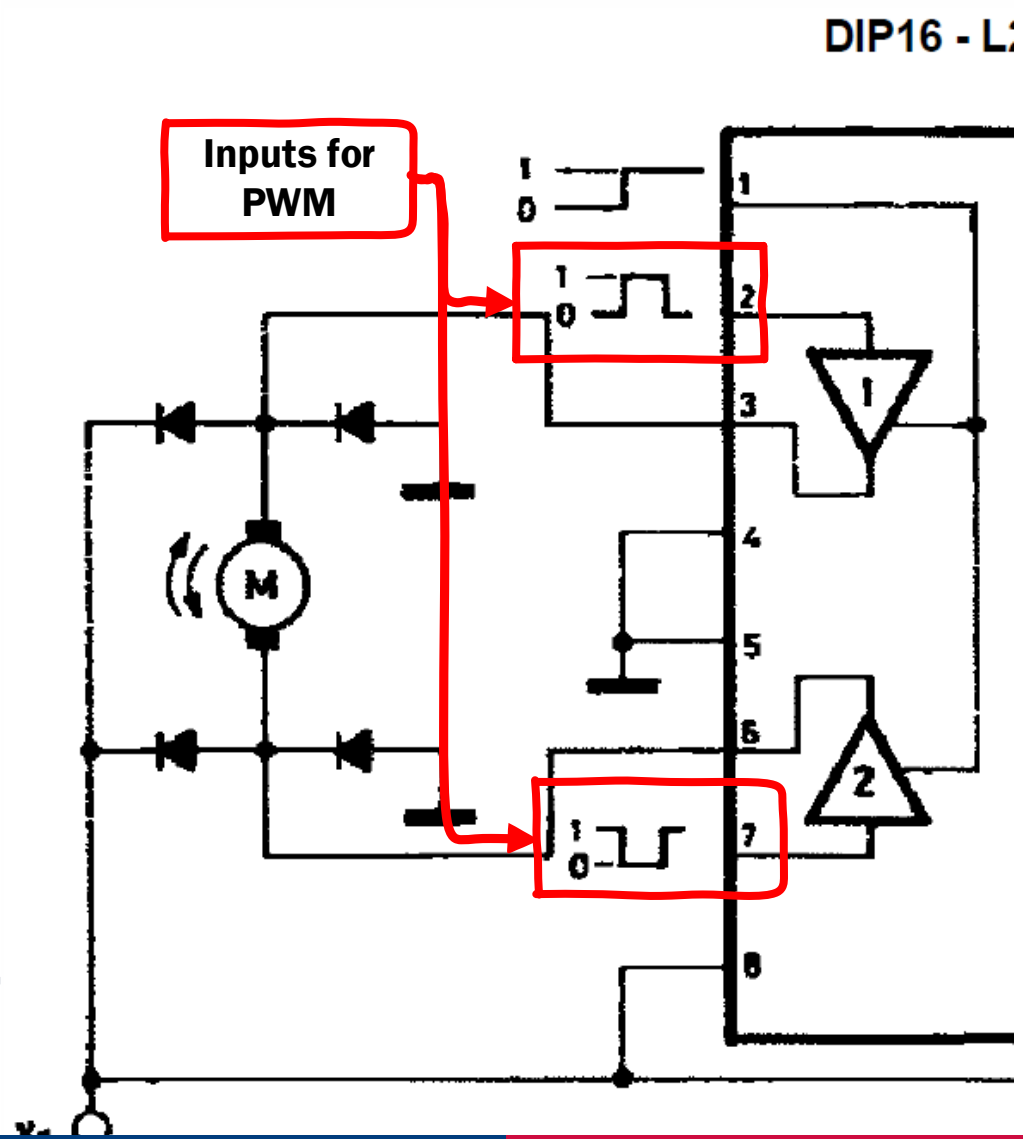
H-Bridge Circuit



H-Bridge Circuit



H-Bridge Circuit



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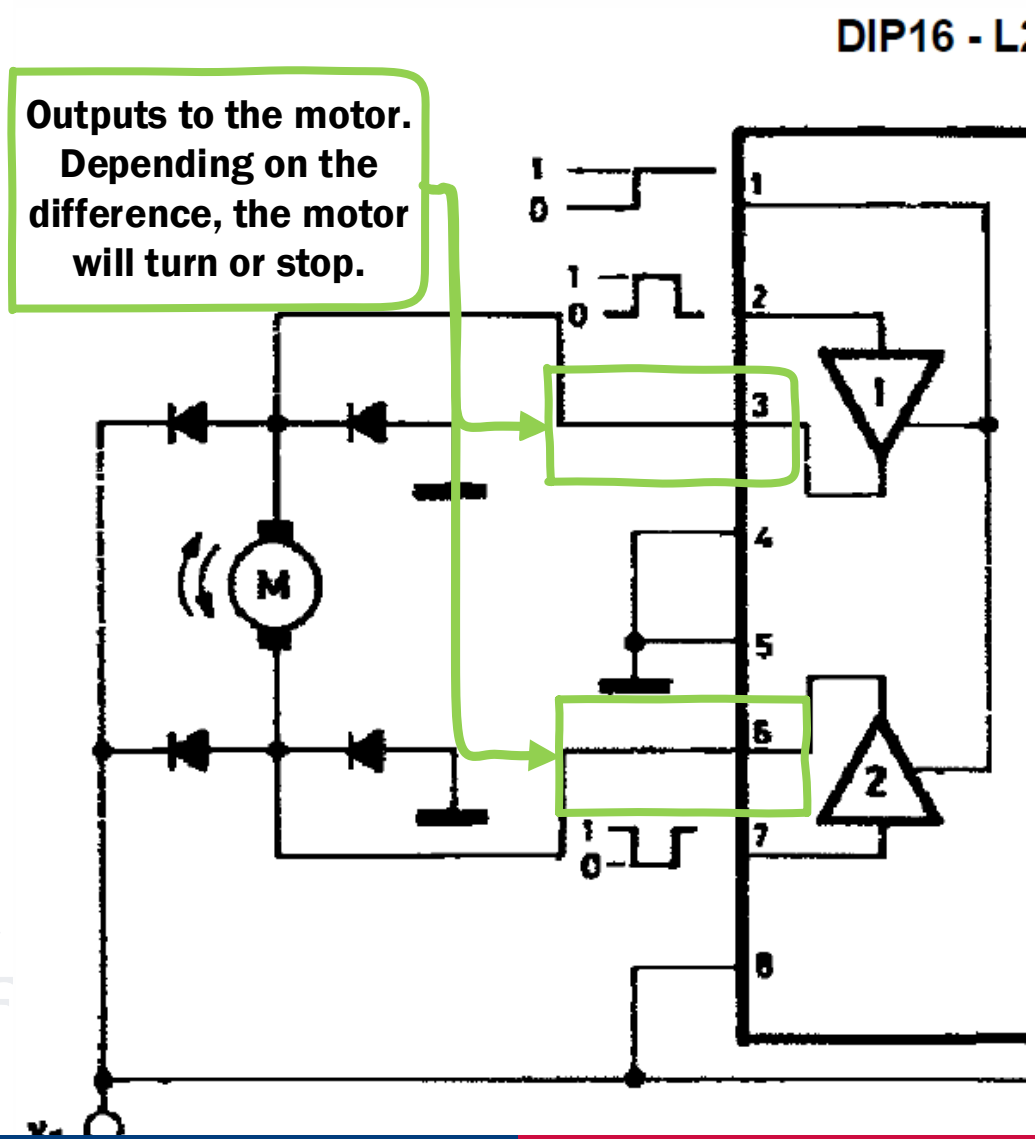
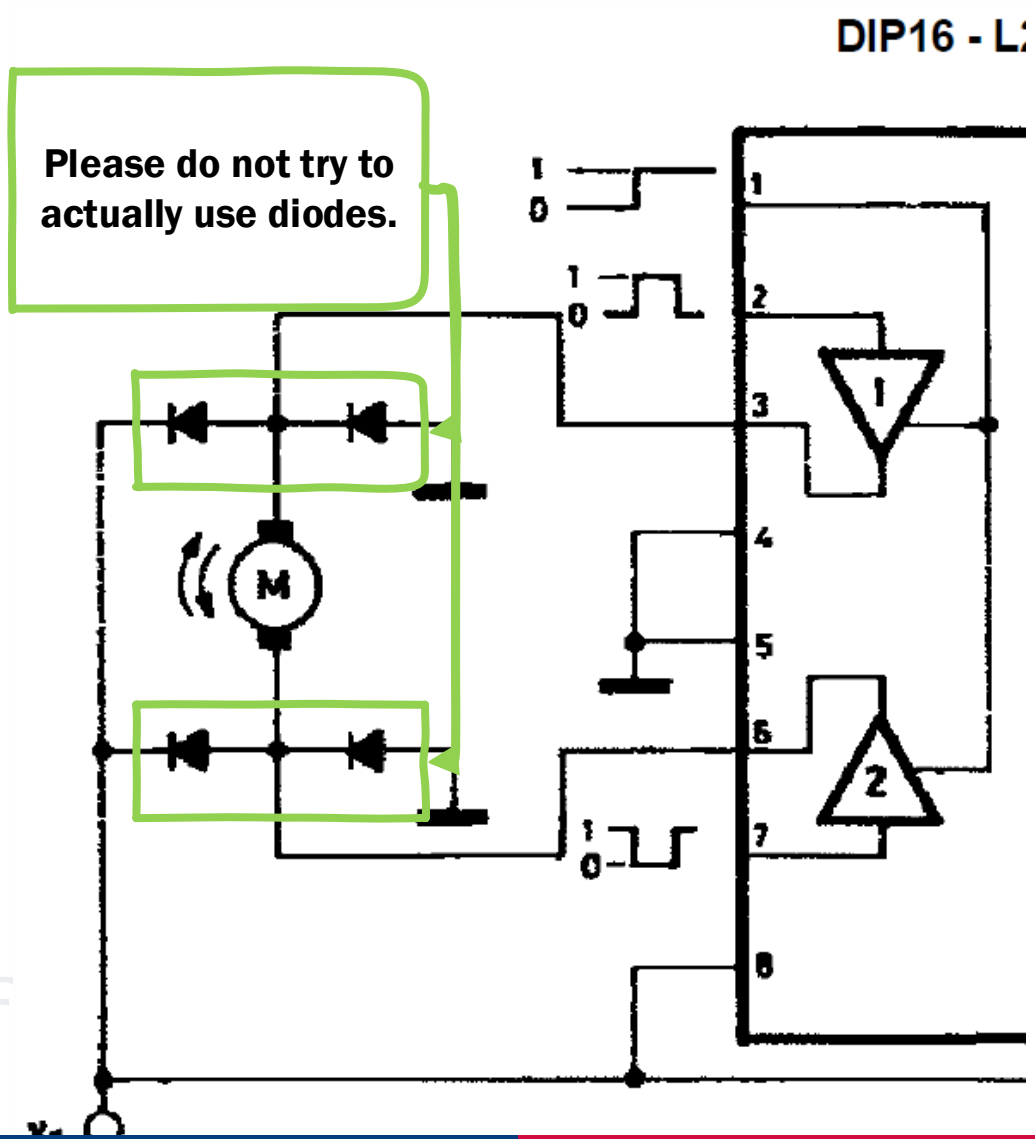


H-Bridge Circuit



Outline

SPI

Reference Material

Section 23 in the PIC32MX Family Reference Manual
Section 17 in the PIC32MX Data Sheet

SPI

Introduction to SPI

1. Stands for Serial Peripheral Interface

SPI

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2. It is a *serial*, *synchronous* protocol.

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3. It is full-duplex.

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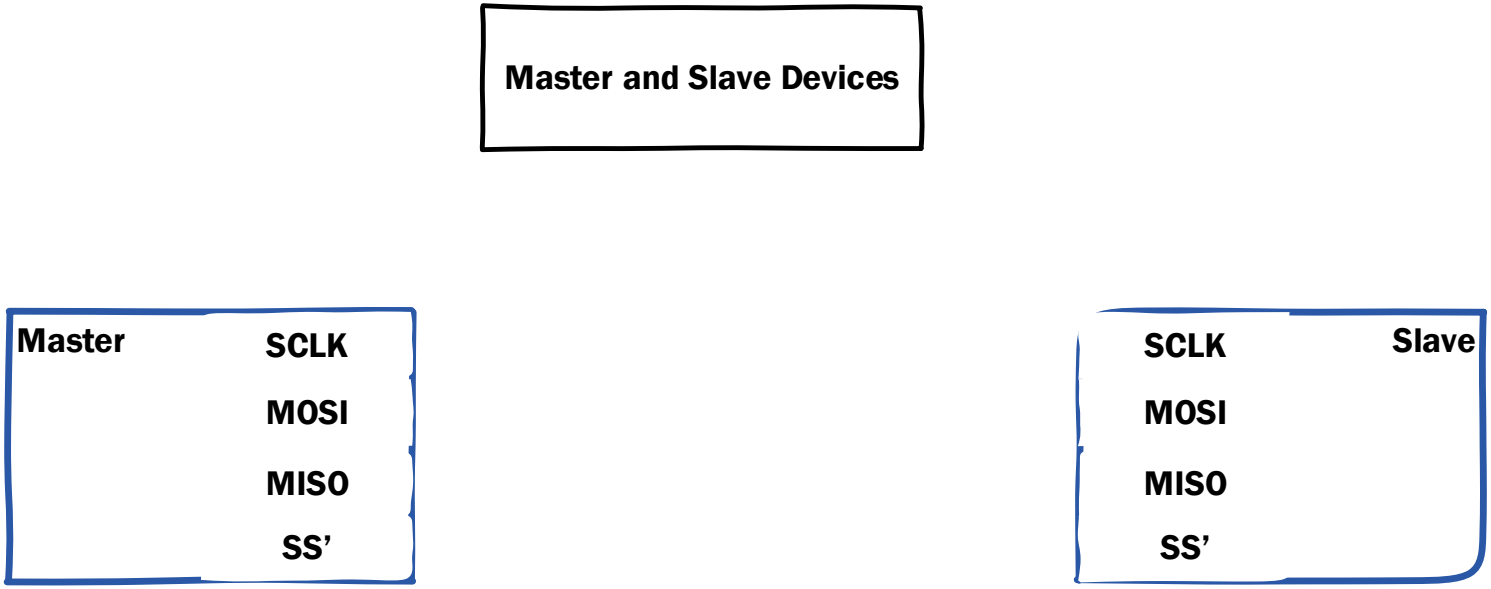
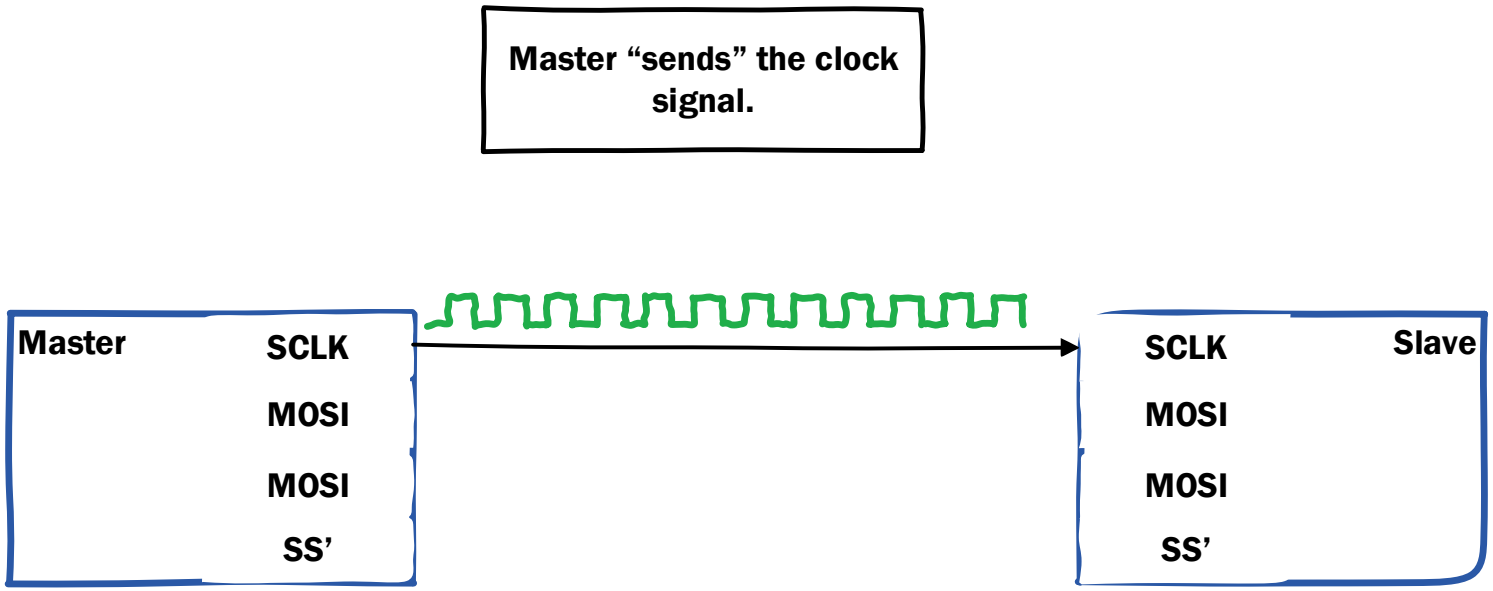
Introduction to SPI

1. Stands for Serial Peripheral Interface
2. It is a *serial*, *synchronous* protocol.
3. It is full-duplex.
4. Uses a master-slave configuration

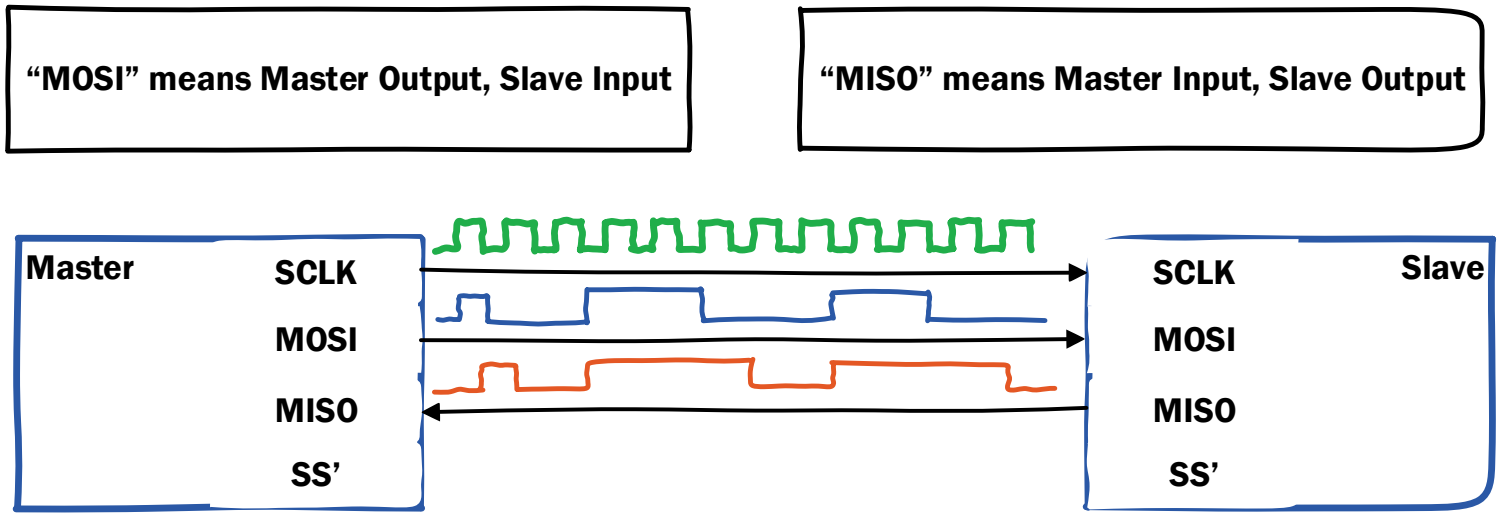
SPI Configuration



SPI Configuration

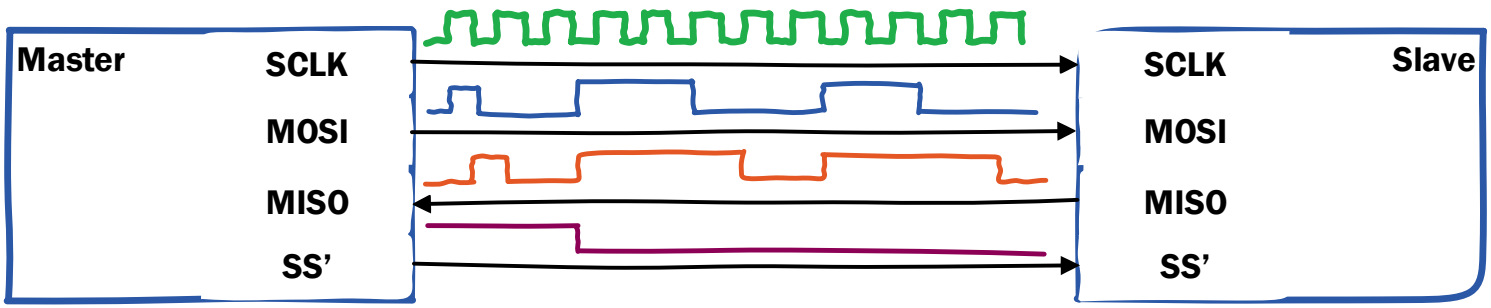


SPI Configuration

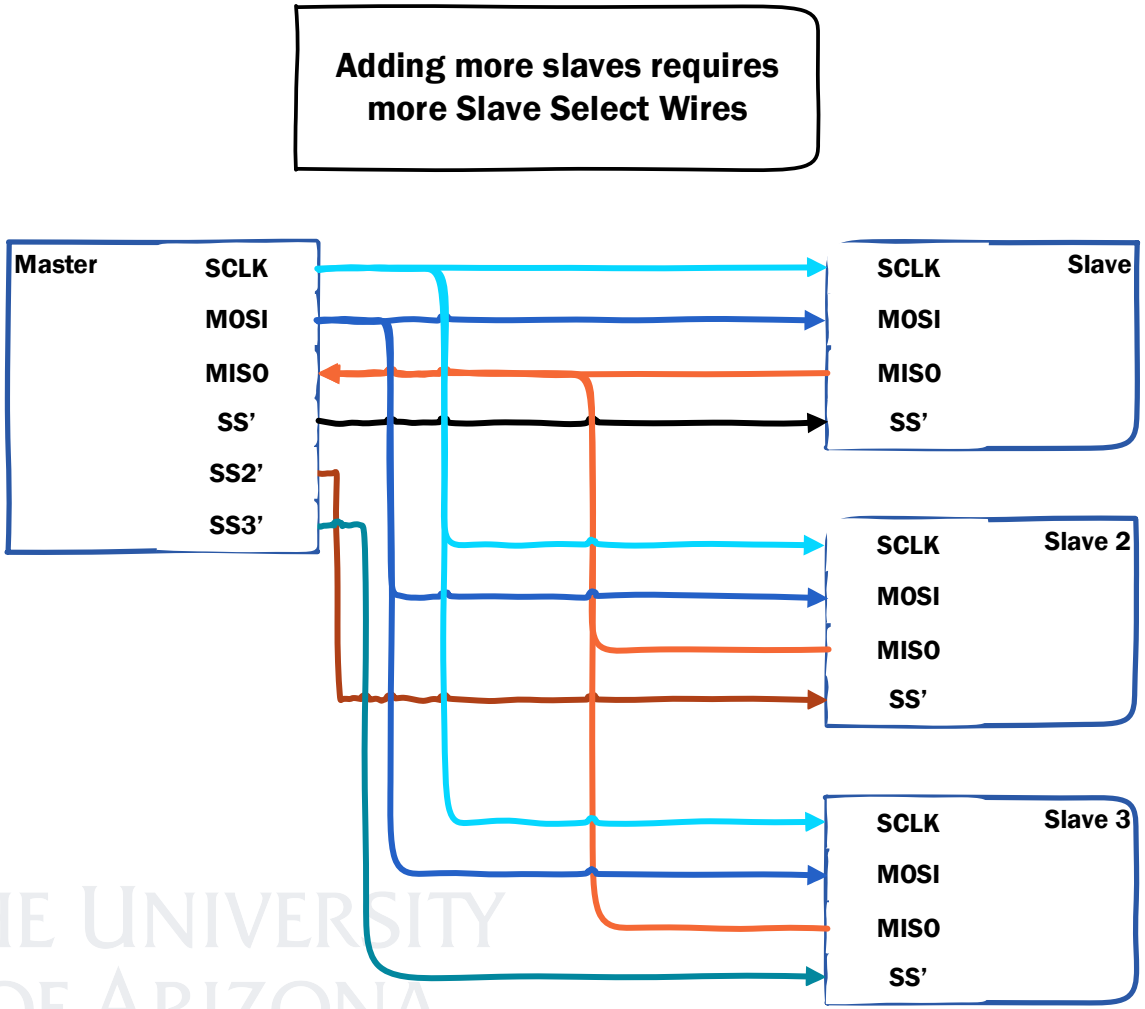


SPI Configuration

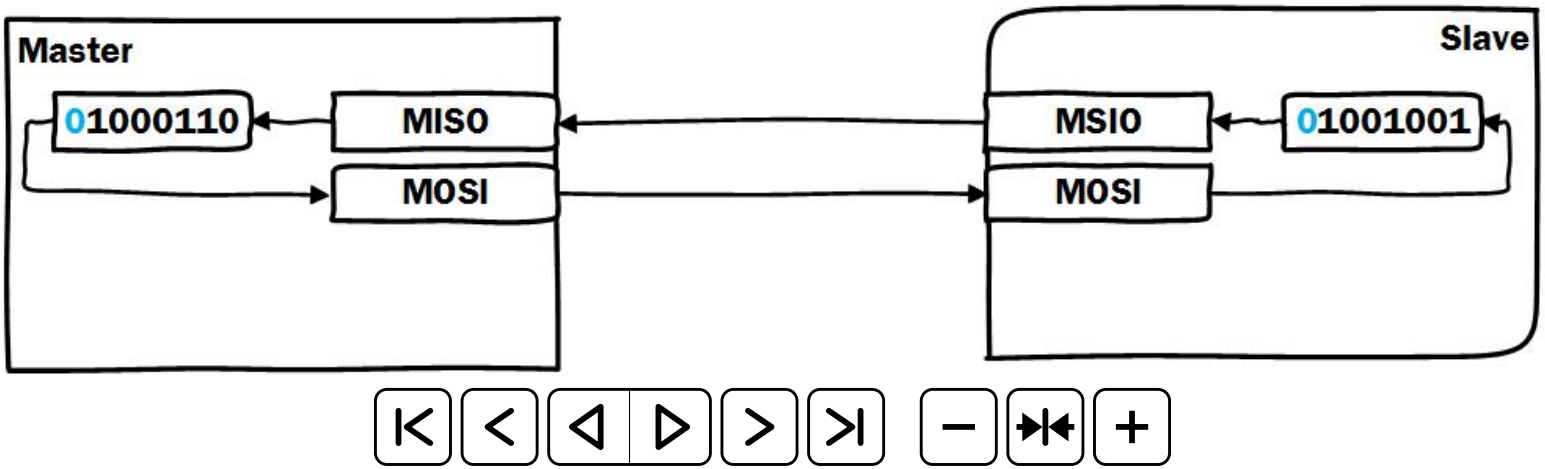
"SS'" is Slave Select
When the SS is *high*, data is not valid.
In fact, unless it is low, the slave will not send data in general.



SPI Multi-Slave Configuration

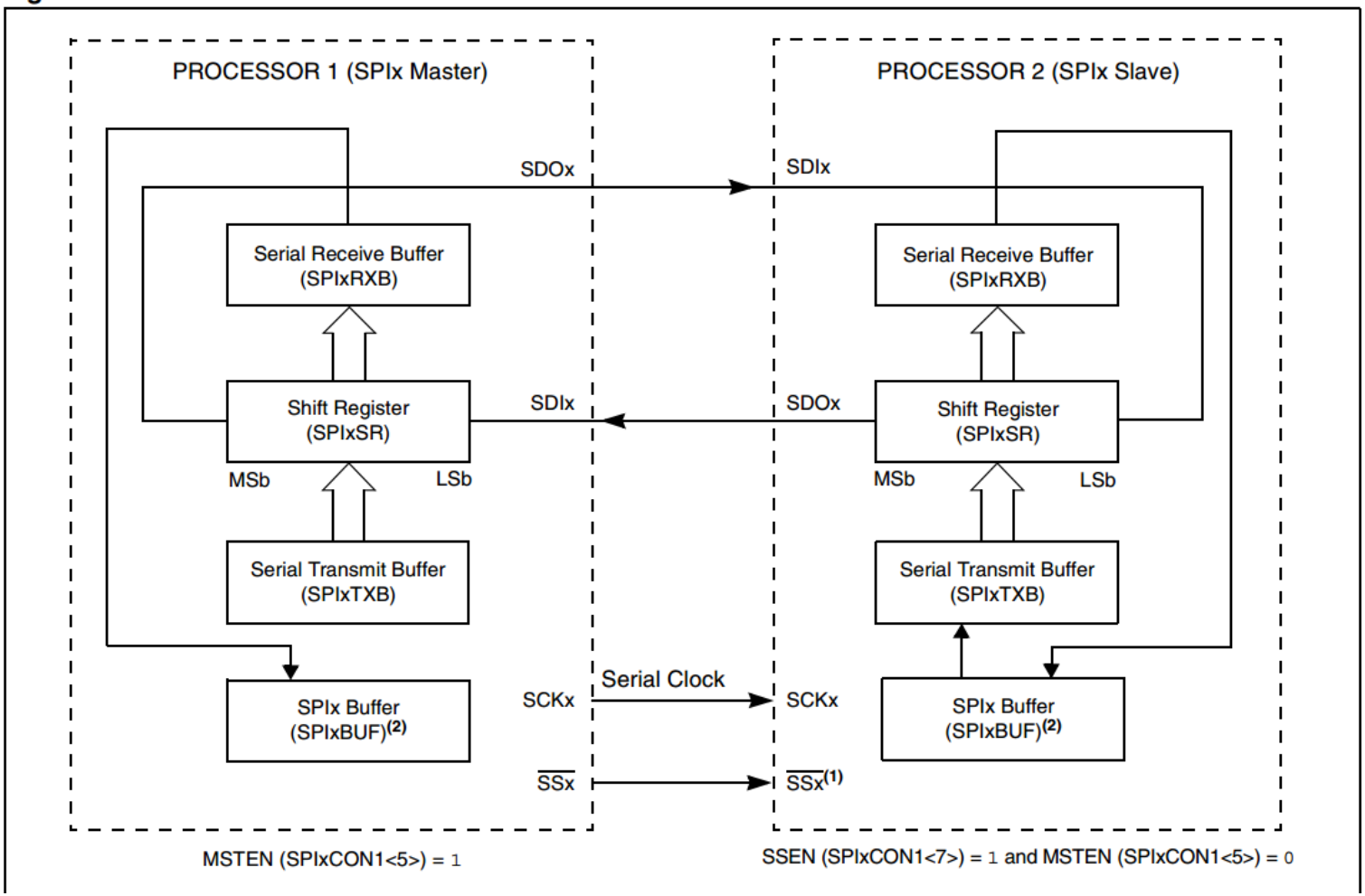


SPI Configuration



SPI Circuit

Figure 23-3: SPIx Master/Slave Connection



Demonstration

SPI Demonstration

Sending data to an accelerometer.