Aristotle Reference Data

Instructions

Mnemonic	Tvpe	Name	Description	Opcode
add	S	ADD	R[cr] = R[cr] +	
aaa	D	1100	M[sp+{s1, 1b'0}]	00010
addc	С	ADD Const	R[cr] = R[cr] +	00001
adde	C	ADD CONSC	const	00001
addcsp	С	ADD Const	$SP = SP + \{const,$	00101
addesp	C	Stack		00101
			1b'0}	
	S	Pointer	R[cr] = R[cr] &	10110
and	5	AND		10110
1 -	-	7.N.D. C	M[sp+{s1, 1b'0}]	10101
andc	С	AND Const	R[cr] = R[cr] &	10101
		0.0	const	01110
or	S	OR	$R[cr] = R[cr] \mid$	01110
	_		M[sp+{s1, 1b'0}]	10001
orc	С	OR Constant	$R[cr] = R[cr] \mid$	10001
			const	
sub	S	SUBtraction	R[cr] = R[cr] -	00110
			M[sp+{s1, 1b'0}]	
sl	С	Shift Left	R[cr] << const	01001
sr	С		R[cr] >> const	
lds	S	LoaD from	$R[cr] = M[sp+{s1,}$	11010
		Stack	1b'0}]	
wrs	S	WRite to	M[sp+{s1, 1b'0}]	10010
		Stack	= R[cr]	
ssp	С	Set Stack	SP = R[cr]	00011
		Pointer		
lpc	S	LoaD PC	R[cr] = PC	00111
lsp	S	LoaD SP	R[cr] = SP	01011
lu	С	Load Upper	R[cr] = {const,	10100
		bits	6b'0}	
b	С	Branch	PC = R[cr]	11100
beq	S	Branch	if (M[sp+{s1,	00000
	-	EQual	1b'0}] ==	
		~	M[sp+{s2, 1b'0}])	
			PC = R[cr]	
bge	S	Branch	if (M[sp+{s1,	00100
290	~	Greater	1b'0}] >=	00100
		than or	M[sp+{s2, 1b'0}])	
		Equal	PC = R[cr]	
bat	S	Branch	if (M[sp+{s1,	01000
290	~	Greater	1b'0}] >	01000
		Than	M[sp+{s2, 1b'0}])	
		111411	PC = R[cr]	
bneq	S	Branch Not	if (M[sp+{s1,	01100
Direq	U	EQual	1b'0}] !=	01100
		Dogadi	M[sp+{s2, 1b'0}])	
			PC = R[cr]	
bpc	С	Branch	PC = PC + const	11111
PPC	C		IC - IC + CONSC	T T T T T
		relative to		
and	C	PC FND of the	Marka the and of	11011
end	С	END of the	Marks the end of	TTOTT
		program	execution	

Pseudo instruction	Name	Description
addow	ADD	R[cr] = M[sp+s1] +
	OverWrite	M[sp+s2]
call	Call	R[cr] = PC + 6
	branch	M[SP] = R[cr]
		PC = PC + s1
ld	Load	R[cr] = PC + s1
	label	

Core Instruction Formats

	15	14	10	9	5	4		0
С	const				opcode			
S	Χ		s2	s1			opcode	

RTL Instructions

Branches	Literal	PC-Relative	
Fetch &	IR <= Me	m[PC]	
Increment	PC <= PC	2 + 1	
Decode &	ALU1 <= SP +	PC <= PC +	
Early	imm(IR[9:5])	imm(IR[15:5])	
Writeback	ALU2 <= SP +		
	imm(IR[14:10])		
Memory	<pre>Mem1 <= Mem[ALU1]</pre>		
	<pre>Mem2 <= Mem[ALU2]</pre>		
Writeback	if $(Mem1 == Mem2)^*$		
	PC <= CR		

*Can be replaced with >=, >, !=, or no condition

ALU	S Type	C Type		
Fetch &	<pre>IR <= Mem[PC]</pre>			
Increment	PC <= PC + 1			
Decode &	ALU1 <= SP +	CR <= CR op		
Early	imm(IR[9:5])	imm(IR[15:5])*		
Writeback				
Memory	Mem1 <= Mem[ALU1]			
Writeback	CR <= CR op Mem1			

^{*}CR can be replaced with SP

Stack	lds	wrs		
Fetch &	<pre>IR <= Mem[PC]</pre>			
Increment	PC <=	PC + 1		
Decode &	ALU1 <= SP + imm(IR[9:5])			
Early				
Writeback				
Memory	CR <= Mem[ALU1]	Mem[ALU1] <= CR		
Writeback				

Register lpc		lsp		
Fetch &	<pre>IR <= Mem[PC]</pre>			
Increment	PC <= PC + 1			
Decode &	CR <= PC	CR <= SP		
Early				
Writeback				
Memory				
Writeback				

Stack Frame

Caller Local		
	arg	
Caller Setup for	arg1	
Callee	arg0	
	Return Address	SP During Caller
Callee Local		SP During Callee

