Project 1 Report

Digital VLSI Design

Estimating Leakage of ISCAS 74182 Circuit

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1 Introduction

Our project seeks to understand the principles underlying MOSFET behavior, focusing on fundamental aspects such as transistor characteristics, transistor stacks, and circuit leakage.

The project progresses through distinct stages, each building upon the knowledge from the previous one. We begin by characterizing individual MOSFETs, then investigate the behavior of MOSFET pairs, and finally estimate leakage in complex gate-level schematics.

Our exploration covers the behavior of MOSFETs during activation and deactivation, when stacked together, and the potential for electrical leakage in circuits.

2 Objectives

Our project, conducted with parameters including model files at 45nm MGK, a supply voltage of 1.1V, and a temperature of 25°C, aims to enhance understanding of MOSFET behavior, analyze transistor stacks, and estimate leakage in gate-level schematics. Specific objectives include:

1. **To Characterize MOSFETs:**
    - Investigate the behavior of MOSFETs under varying transistor widths and supply voltages.
    - Analyze MOSFET characteristics in both ON and OFF states to understand their performance.
2. **To Analyze Transistor Stacks:**
    - Explore the behavior of NMOS and PMOS transistor stacks consisting of two transistors.
    - Investigate the intermediate node voltages for different input combinations in transistor stacks.
3. **To Estimate Leakage in Gate-Level Schematics:**
    - Develop a script capable of estimating leakage in an ISCAS 74182 circuit using matrices generated in earlier stages.
    - Construct n-input gates using 2-input gates and/or inverters, and estimate leakage in the circuit.
    - Design the circuit netlist in Ngspice for cross-verification of leakage estimation.

3 Methodology and Stage-wise Analysis

The project is divided into several stages, each addressing different aspects of MOSFET behavior and circuit analysis. These stages are designed to progressively deepen our understanding of MOSFET-based circuits and their performance characteristics.

3.1 Stage 1: MOSFET Characterization

In Stage 1, we analyzed the performance of MOSFETs under different transistor widths and supply voltages. We will vary transistor widths ranging from W to 8W to comprehensively understand their influence on MOSFET performance.

3.1.1 Results

Stage 1 focused on understanding MOSFET behavior. This stage successfully characterized the transistors under these conditions, laying the groundwork for further exploration in upcoming stages.

MOSFET	State	Observation
NMOS	OFF	Leakage current increases with wider transistor width and higher source voltage.
	ON	Higher gate voltage leads to increased drain current.
PMOS	OFF	Leakage current increases with wider transistor width and more negative gate voltage.
	ON	Increase in drain current with more positive gate voltage.

Table 1: Observations for NMOS and PMOS transistors in different states.

3.1.2 Analysis and Inferences

NMOS OFF

- As the source voltage increases, there's a slight rise in the leakage current. This is likely because a stronger electric field across the depletion region aids conduction mechanisms like tunneling.
- The plot shows that NMOS transistors with larger widths (represented by wider curves) exhibit higher leakage currents.
- This is because wider transistors have a larger depletion region, resulting in a larger area for current flow.

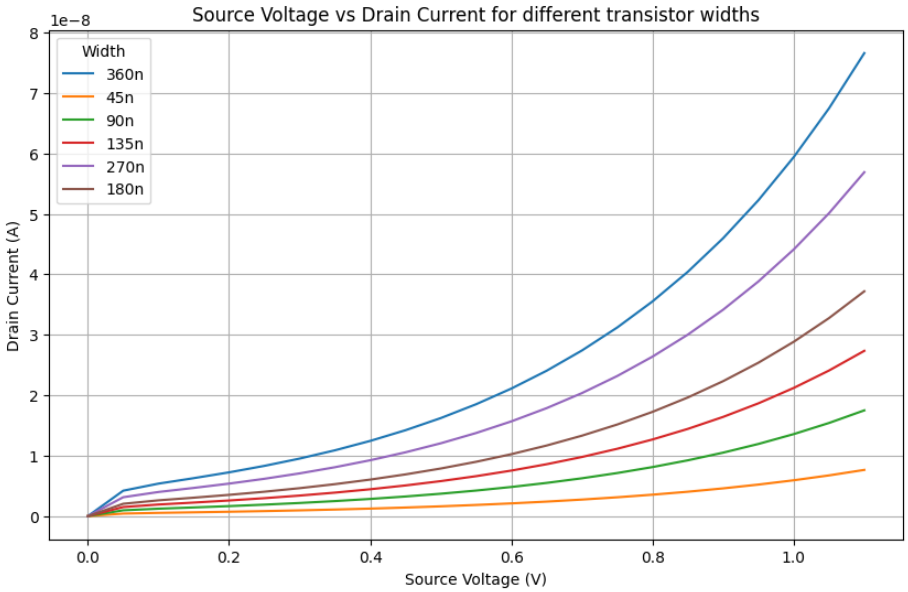

Figure 1: Source Voltage vs Drain Current for different transistor widths

Overall, the NMOS leakage current (OFF state) plot shows a slight rise in current with increasing source voltage and wider transistors also exhibit higher leakage currents due to a larger area for current flow in the depletion region.

NMOS ON

- As the gate voltage increases, the drain current also increases for each transistor width.
- This is because a higher gate voltage creates a stronger electric field between the gate and the channel, which induces more mobile charge carriers in the channel.
- The wider transistors have higher drain currents for a given gate voltage compared to narrower transistors.
- This is because wider transistors have a larger channel width, which allows more current to flow for the same electric field strength.

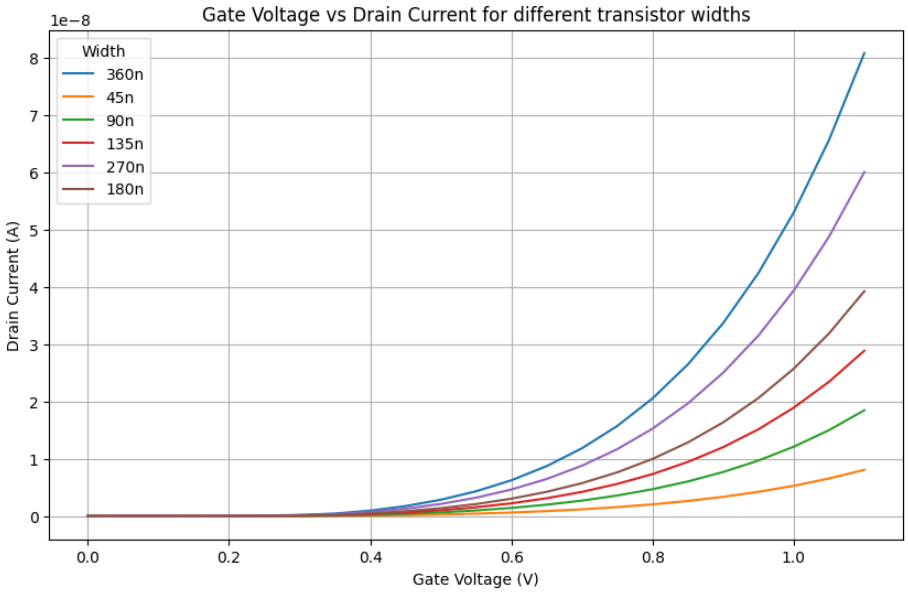

Figure 2: Gate Voltage vs Drain Current for different transistor widths

Overall, the NMOS ON plot demonstrates that both higher gate voltage and wider transistor width result in increased drain current.

PMOS OFF

- The plot shows the drain current for various PMOS transistor widths when the transistor is in the OFF state.
- The PMOS leakage current (OFF state) plot shows a rise in current with increasingly negative gate voltage.
- This is because a more negative gate voltage creates a stronger electric field across the depletion region, which can slightly increase the amount of tunneling or sub-threshold conduction.
- Wider PMOS transistors exhibit higher leakage currents even in the OFF state.

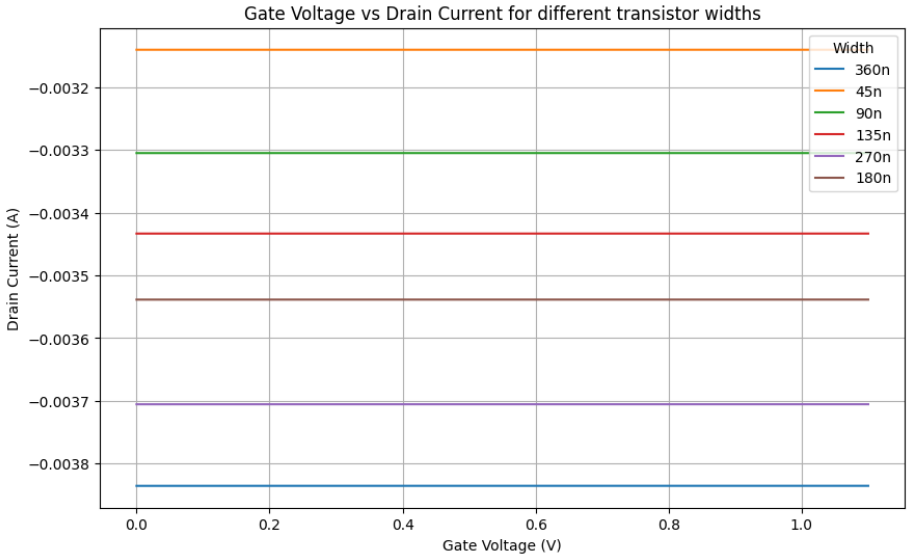

Figure 3: Gate Voltage vs Drain Current for different transistor widths

Overall, PMOS transistors with larger widths will have higher leakage currents in the OFF state than transistors with smaller widths.

PMOS ON

- For each curve, the drain current should increase as the gate voltage becomes more negative.
- Wider transistors generally have a higher current carrying capacity due to a larger channel area. This is because they can accommodate more mobile charge carriers (holes) for the same electric field strength.
- The difference in current levels between wider and narrower transistors reflects the impact of channel width on current carrying capacity.

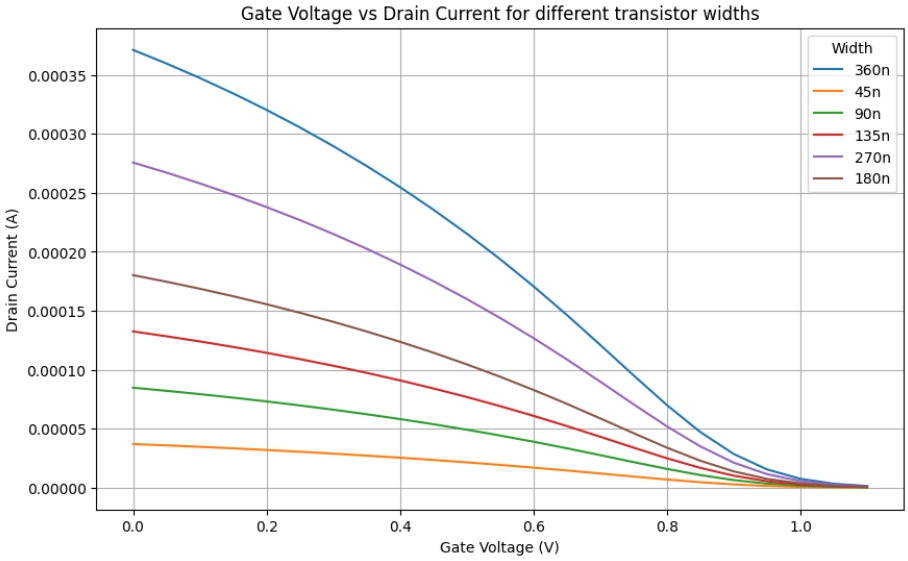

Figure 4: Gate Voltage vs Drain Current for different transistor widths

In PMOS ON transistors, increasing the gate voltage negatively should boost drain current. Wider transistors have a greater current capacity due to their larger channel area, accommodating more charge carriers.

3.2 Stage 2: Transistor Stack Analysis

Stage 2 of the project focuses on generating matrices of NMOS and PMOS stacks, each comprising two transistors with 2-PMOS in the pull-up network and 2-NMOS in the pull-down network.

The main objective is to analyze the behavior of NMOS and PMOS transistor stacks under varying input conditions. By considering four input combinations (00, 01, 10, and 11) and maintaining a constant supply voltage of 1.1V, we aim to extract intermediate node voltages from the transistor stacks.

3.2.1 Results

These voltage values represent the behavior of the transistor stacks under different input conditions, providing insights into their functionality and performance. It's important to note that these outcomes are influenced by parameters such as supply voltage (1.1V) and temperature (25°C).

3.2.2 Analysis and Inferences

1. **Input Case 00:**

Input Case	NMOS Stack (v(x))	PMOS Stack (v(x))
00	0.0795 V	0.381 V
01	0.0000755 V	0.228 V
10	0.917 V	0.900 V
11	0.0000388 V	0.0000388 V

Table 2: Intermediate node voltages for NMOS and PMOS stacks under different input conditions.

- **NMOS Stack:** The voltage at the intermediate node for the NMOS stack is 0.07954502 V. In this case, both NMOS transistors are OFF, resulting in minimal current flow. Therefore, the voltage at the intermediate node is relatively low.
- **PMOS Stack:** The voltage at the intermediate node for the PMOS stack is 0.3815347 V. Similarly, both PMOS transistors are OFF, leading to minimal current flow. However, the series connection of the PMOS transistors results in a higher voltage drop, leading to a relatively higher voltage at the intermediate node.

2. **Input Case 01:**

   - **NMOS Stack:** The voltage at the intermediate node for the NMOS stack is 7.548177×10^{-5} V. In this scenario, the first NMOS transistor is OFF, while the second NMOS transistor is ON. As a result, there is minimal current flow through the NMOS stack, leading to a voltage close to 0 V at the intermediate node.
   - **PMOS Stack:** The voltage at the intermediate node for the PMOS stack is 2.277686×10^{-1} V. With the first PMOS transistor ON and the second PMOS transistor OFF, there is significant current flow, leading to a higher voltage at the intermediate node compared to the NMOS stack.

3. **Input Case 10:**

   - **NMOS Stack:** The voltage at the intermediate node for the NMOS stack is 0.916781×10^{0} V. In this case, both NMOS transistors are ON, allowing significant current flow. Therefore, there is a higher voltage drop across each transistor, resulting in a relatively higher voltage at the intermediate node.
   - **PMOS Stack:** The voltage at the intermediate node for the PMOS stack is 0.8998845×10^{0} V. Conversely, both PMOS transistors are OFF, resulting in minimal current flow and a lower voltage at the intermediate node compared to the NMOS stack.

4. **Input Case 11:**

    - **NMOS Stack:** The voltage at the intermediate node for the NMOS stack is 3.884222×10^{-5} V. In this scenario, both NMOS transistors are OFF, leading to minimal current flow and a voltage close to 0 V at the intermediate node.
    - **PMOS Stack:** The voltage at the intermediate node for the PMOS stack is also 3.884222×10^{-5} V. Similarly, both PMOS transistors are OFF, resulting in minimal current flow and a voltage close to 0 V at the intermediate node.

3.3 Stage 3: Leakage Estimation

The Final Stage involves developing a script to estimate leakage in an ISCAS 74182 circuit using matrices generated in previous stages. The script replaces 3 or 4-input gates with 2-input gates for accuracy. Additionally, the circuit netlist is designed in Ngspice for cross-verification.
The leakage estimation is conducted using the following functions:

1. **Single NMOS Leakage Estimation:** Calculates leakage power, subthreshold current, body current, and gate current for a single NMOS transistor based on input voltage and configuration.
2. **Single PMOS Leakage Estimation:** Similar to single NMOS, calculates leakage power, subthreshold current, body current, and gate current for a single PMOS transistor.
3. **Stacked NMOS Leakage Estimation:** Computes leakage power, subthreshold current, body current, and gate current for stacked NMOS transistors in series configuration.
4. **Stacked PMOS Leakage Estimation:** Similar to stacked NMOS, calculates leakage power, subthreshold current, body current, and gate current for stacked PMOS transistors.

Using the results obtained in the above 2 stages, we see that we can construct all gates using either the single NMOS/PMOS configurations and/or pull-up and pull-down network configurations in different combinations.

We first obtain 2 input logic gates using the single CMOS and stacked CMOS configurations, and we also make an inverter. Using these 2 input logic gates and inverters, we can make logic gates that can correspond to any number of inputs. This is how we obtain the final ISCAS-74182 circuit.

The gates that we have constructed are as follows:

1. **Inverter:** Made using a single PMOS and single NMOS
2. **2-input NAND gate:** Made using 2 single PMOS and a stacked NMOS

3. **2-input NOR gate:** Made using 2 single NMOS and a stacked PMOS
4. **2-input AND gate:** Made using a 2-input NAND gate and an inverter
5. **2-input OR gate:** Made using a 2-input OR gate and an inverter
6. **3-input AND gate:** Made using two 2-input AND gates $[(A * B) * C]$
7. **3-input OR gate:** Made using two 2-input OR gates $[(A + B) + C]$
8. **3-input NOR gate:** Made using a 3-input OR gate and an inverter $[(A + B + C)']$
9. **4-input AND gate:** Made using three 2-input AND gates $[((A * B) * (C * D))]$
10. **4-input OR gate:** Made using three 2-input OR gates $[(A+B)+(C+D)]$
11. **4-input NOR gate:** Made using a 4-input OR gate and an inverter $[(A + B + C + D)']$

3.3.1 Results

The results, summarized in Table 3, illustrate the various parameters affecting leakage, including subthreshold current, body current, and gate current.

The leakage power of the NAND2 cell is approximately 3.86 µW, indicating the amount of power consumed due to leakage currents in the transistors. The subthreshold current, which represents the leakage current flowing through the transistors when they are in the OFF state, is around 1.20 µA. The bulk current (Ib) and gate current (Ig) are also provided, showing the current flowing through the bulk and gate terminals of the transistors, respectively. The ngspice simulation results provide further insights into the current and power consumption of the circuit.

Parameter	**Value**
Leakage Power (W)	3.860×10^{-6}
Subthreshold Current (A)	1.200×10^{-6}
Body Current (A)	4.565×10^{-8}
Gate Current (A)	2.294×10^{-6}

Table 3: Leakage estimation results

The Leakage current estimation for one of the cases

```
sand@LAPTOP-82F7CF0M:/mnt/e/DVD/DVD-Project-1/Stage_3$ python3 circuit_leakage.py
Enter the value of P3: 1
Enter the value of P2: 1
Enter the value of P1: 1
Enter the value of P0: 1
Enter the value of G3: 1
Enter the value of G2: 1
Enter the value of G1: 1
Enter the value of G0: 1
Enter the value of Cn: 1
Leakage Power:  3.860374961879706e-06 W.
Subthreshold Current:  1.199838936560002e-06 A.
Ib:  4.5645184629653345e-08
Ig:  2.2940036429619963e-06
```

Cross Verification with Netlist Simulations

```
******
** ngspice-36 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Copyright 2001-2020, The ngspice team.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Sat Jan  1 18:54:42 UTC 2022
******

No compatibility mode selected!

s
Circuit: *INCLUDE 45nm_MGK.pm

Doing analysis at TEMP = 25.000000 and TNOM = 27.000000

Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignored.
Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignored.
Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignored.
Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignored.

No. of Data Rows : 1
abs(v(vcc)*i(vcc1)) = 2.393049e-06
abs(i(va_1)+i(va_2)+i(va_3)+i(va_4)+i(vb_1)+i(vb_2)+i(vb_3)+i(vb_4)+i(vc1)) = 7.383624e-07
```

3.3.2 Analysis and Inferences

- We observe that the leakage power obtained after building the circuit using the single and stacked CMOS configurations is $3.86 * 10^{-6}$ W.
- We also notice that the leakage power obtained after simulating the circuit on NGSPICE on a gate level, is approximately $2.39 * 10^{-6}$ W.
- The results are in the same order of magnitude, indicating a good correlation between the estimation and simulation methods.
- There is an absolute error of approximately $1.47 * 10^{-6}$ W between the estimated and simulated values. This translates to a percentage error of around 38%.

4 Conclusion

Our project effectively addressed leakage current estimation in the ISCAS 74182 circuit using NGSPICE simulations, data processing, and Python scripting. We derived accurate estimations, cross-validated them with direct measurements, and gained insights into transistor behavior, circuit configurations, and voltage influences.

5 Acknowledgements

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6 Contributions

- **Sankalp S. Bhat** - Stage 1 Netlist Design, Stage 2 Netlist Design, Stage 3 Scripting (Python), Report
- **Sri Anvith Dosapati** - Stage 1 Netlist Design, Stage 2 Netlist Design, Stage 3 Scripting (Python), Report
- **Shreeya Singh** - Stage 1 Scripting and Analysis, Stage 3 Subcircuits (NGSPICE), Stage 3 Cross-Verification (NGSPICE), Report
- **Srujana Vanka** - Stage 1 Scripting and Analysis, Stage 3 Subcircuits (NGSPICE), Stage 3 Cross-Verification (NGSPICE), Report