UNIVERSITY OF SCIENCE - VNUHCM
FACULTY OF ELECTRONICS – TELECOMMUNICATIONS

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DESIGN AND IMPLEMENTATION OF TWO STAGE CMOS OPERATIONAL AMPLIFIER USING 90NM TECHNOLOGY

INTEGRATED CIRCUIT DESIGN LABS

Ho Chi Minh City - August 2024

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Most importantly, I would like to express my deepest gratitude to my beloved family. Their tremendous support and delectable meals have always been a solid spiritual pillar for me to go on this journey.

Tóm tắt

Bộ khuếch đại hoạt động được coi là thiết bị điện tử cấp thiết nhất. Quy trình được ghi trong bài báo này là thiết kế một bộ khuếch đại hoạt động CMOS hai tầng (Opamp) và phân tích tác động của các thông số khác nhau đến các đặc điểm của thiết kế Opamp. Bài báo này chủ yếu tập trung vào thiết kế độ lợi Opamp được tối ưu hóa. Coi đây là khía cạnh chính, các thông số kỹ thuật của Opamp được tính đến, tức là Độ lợi, biên độ pha, tốc độ thay đổi, tiêu tán công suất và các thông số khác. Bài báo này trình bày thiết kế và triển khai bộ khuếch đại hoạt động CMOS hai tầng hoạt động ở điện áp cung cấp ±1V và quy trình mô phỏng được thực hiện bằng cách sử dụng công cụ EDA Custom Compiler Synopsys với công nghệ 90nm. Độ lợi thu được là 84db với biên độ pha là 560 và tiêu tán công suất là 38,02μW

Abstract

Operational amplifier is consider to be the most imperative electronic device. The procedure inscribed in this paper is to design a two stage CMOS operational amplifier (Opamp) and analyze the effect of various parameters on the characteristics of Opamp design. This paper is mainly concentrating on design of optimized Opamp gain. Keeping this as a main aspect, Opamp specifications are taken into account, i.e., Gain, phase margin, slew rate, power dissipation and others. This work presents a design and implementation of two stage CMOS operational amplifier which operates at ±1V supply voltage and Simulation process is carried out by using an EDA tool Custom Compiler Synopsys with 90nm technology. The obtained gain is 84db with phase margin of 560 and the power dissipation is of 38,02μW

Contents

List of Figures

List of Tables

Chapter 1

Introduction Project

1.1 Research Overview

Opamps are the most commonly used devices in electronic circuits. Their applications are wide. They are used in Filters, Differentiators, Integrators, Digital-Analog convertors and Comparators. The challenge faced in CMOS technology is mainly about scaling these devices to decrease their size and power consumption. Opamps are of two types namely inverting Opamp and non-inverting Opamp with two inputs and single output. The main prospect in this report is to design, optimize the size in order to increase the gain of 90nm technology. The modulation made here leads to better efficiency and operating frequency. The problem lies in design and implementation of two stage CMOS Opamp keeping various parameters into consideration which are constraints. In this paper the specification which becomes the target is the (W/L) ratio which indirectly relates to gain. However increase in the gain improves the performance and keeps up the stability of device.

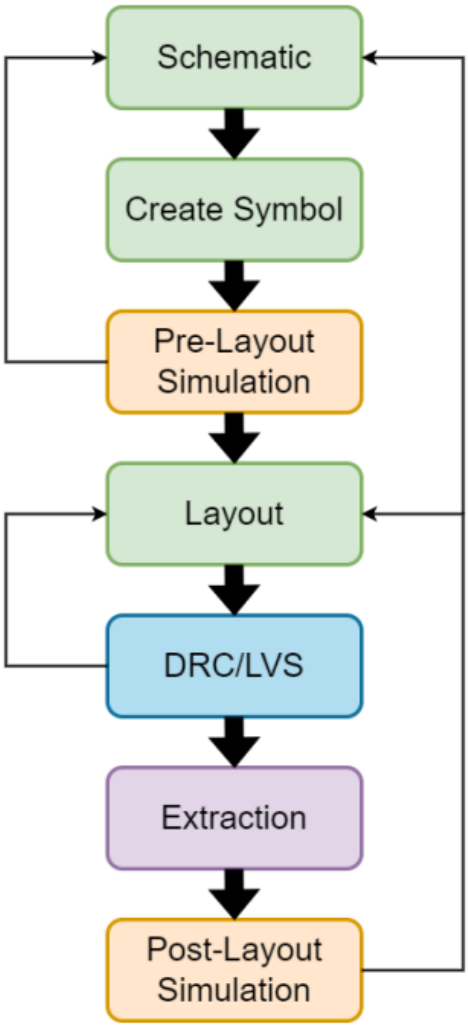

Figure 1.1: Overview of the Analog Integrated Circuit Design Process

1.2 Research Objectives

1.2.1 Analog Circuit Design Flow

The analog IC design flow includes 8 main steps: Schematic, Symbol, Pre-Layout Simulation, Layout, DRC/LVS, Extraction, and Post-Layout Simulation. This is the complete analog IC design flow using IC design tools, with the purpose of obtaining the Layout file (the physical representation of the circuit). After that, the physical layout file will be sent to the fabrication facility to produce the final, fully realized physical circuit.As this project we use Custom Comiler to design

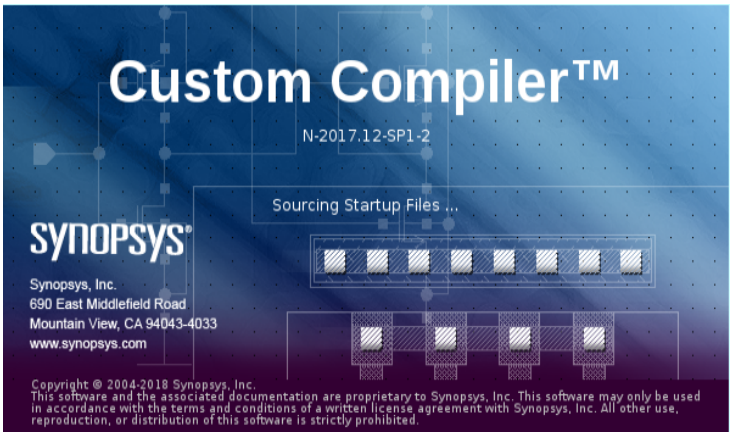

Figure 1.2: EDA tool Custom Compiler

Schematic: The first step is to design the schematic of the analog circuit.In this step, components such as resistors, capacitors, transistors, amplifiers, etc. are assembled together to create the analog circuit design.The schematic will serve as the basis for the subsequent steps.

Symbol: After completing the schematic, the designed components will be represented using corresponding symbols.These symbols will be used in the layout step to assemble the physical circuit.

Pre-Layout Simulation: Before performing the layout, the circuit will be simulated and analyzed to check the performance and operation.This simulation helps to verify and refine the design before moving to the layout stage.

Layout: This step involves converting the circuit schematic into the physical layout of the components on the chip. The components will be arranged and positioned on the chip to optimize for area, performance, and integration. DRC/LVS (Design Rule Check/Layout vs Schematic): After completing the layout, this step will check the compliance of the layout with the design rules (DRC) and compare it with the original schematic (LVS).This verification ensures that the layout matches the initial design. Extraction: From the layout, parameters such as resistance, capacitance, etc. will be extracted.These parameters will be used for the post-layout simulation.

Post-Layout Simulation: Based on the extracted parameters from step 6, the circuit

will be simulated again to verify the performance after the layout.This simulation provides a more accurate assessment compared to the pre-layout simulation.

Create Layout File: After completing all the above steps, the final layout file will be generated.This file contains the physical information about the circuit and will be sent to the fabrication facility to produce the actual circuit. For the full custom IC design using the Synopsys Custom Compiler, the above flow is applicable. The Synopsys Custom Compiler is a comprehensive design environment that supports the entire custom IC design flow, from schematic capture to layout. It provides advanced features for analog, mixed-signal, and custom digital design, allowing designers to optimize the design for performance, power, and area.

Chapter 2

Theoretical basis of Two-Stage Opamp

An operational amplifier (often op amp or opamp) is a DC-coupled electronic voltage amplifier with a differential input, a (usually) single-ended output,[1] and an extremely high gain. Its name comes from its original use of performing mathematical operations in analog computers.

By using negative feedback, an op amp circuit's characteristics (e.g. its gain, input and output impedance, bandwidth, and functionality) can be determined by external components and have little dependence on temperature coefficients or engineering tolerance in the op amp itself. This flexibility has made the op amp a popular building block in analog circuits. The op amp is one type of differential amplifier. Other differential amplifier types include the fully differential amplifier (an op amp with a differential rather than single-ended output), the instrumentation amplifier (usually built from three op amps), the isolation amplifier (with galvanic isolation between input and output), and negative-feedback amplifier (usually built from one or more op amps and a resistive feedback network).

2.1 General introduction to Operation

It has two stages, as shown in the block diagram where stage 1 is the differential amplifier and common source amplifier becomes stage 2. The differential amplifier has two

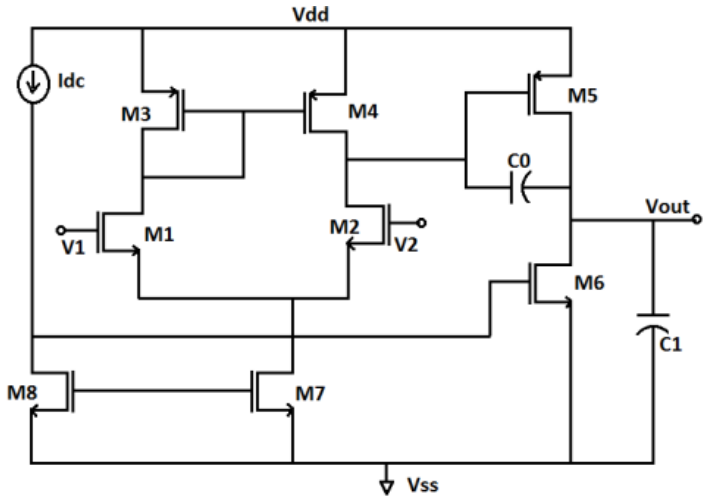

Figure 2.1: Circuit Diagram of Opamp

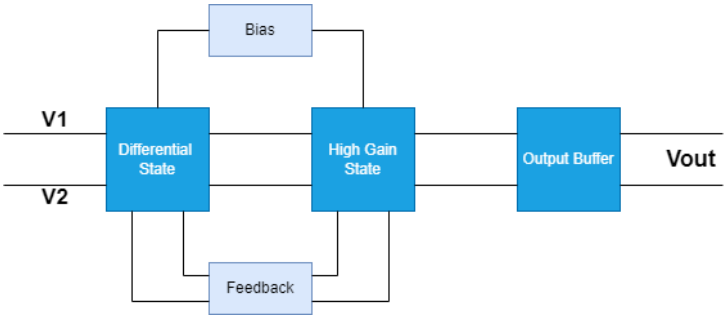

Figure 2.2: Block diagram of two stage Opamp

different voltage inputs vin+ and vin- which amplifies the differences between two input voltages. Since the gain obtained from the first stage is not sufficient, it uses common source amplifier at second stage. Thus, the output of this differential amplifier continues to enter the common source amplifier where further more gain is increased. In order to obtain low gain at high frequencies and maintain the device' stability, it includes compensation circuit whenever the device is in negative feedback condition.

Chapter 3

DESIGN PROCEDURE

3.1 Design Diode-Connected

A diode-connected transistor is a method of creating a two-terminal rectifying device (a diode) out of a three-terminal transistor. A characteristic of diode-connected transistors is that they are always in the saturation region for metal–oxide–semiconductor field-effect transistors (MOSFETs) and junction-gate field-effect transistors (JFETs), and in the active region for bipolar junction transistors (BJTs).

A diode-connected transistor is made by connecting

The base and collector of a BJT

The drain and source of a JFET

The gate and drain of a MOSFET

Diode-connected transistors are used in current mirrors to provide a voltage drop that tracks that of the other transistor as temperature changes.They also have very low reverse leakage currents.

To put the MOSFET in the saturation region, we can connect the gate (G) to the drain (D). This is known as the *diode-connected configuration*.

In this configuration, the voltages at the gate (G) and drain (D) are equal: $V_g = V_d$. This means that the gate-source voltage (V_{gs}) is equal to the drain-source voltage (V_{ds}),

i.e., $V_{gs} = V_{ds}$.

For the MOSFET to be in the saturation region, the following condition must be met:

$$V_{gs} - V_{th} < V_{ds} \tag{3.1}$$

Where V_{th} is the threshold voltage of the MOSFET.

In the diode-connected configuration, the above condition becomes:

$$V_{gs} - V_{th} < V_{ds} \implies V_{th} > 0 \tag{3.2}$$

This means that in the saturation region, the gate-source voltage (V_{gs}) is equal to the drain-source voltage (V_{ds}), and the threshold voltage (V_{th}) must be greater than 0.

We can take the threshold voltage (V_{th}) from the model in the library, which is 0.397 V for the TT12 (1.2V) technology. Then, we can recalculate the V_{th} of our own MOSFET to ensure that it meets the saturation region condition.

In the CC Synopsys tool we designed a circuit for finding β effective and Vth values for NMOS and PMOS

NMOS	PMOS
W = 0.2 um	W=0.2m
L = 0.1 um	L=0.1m

Table 3.1: Parameters W & L of PMOS NMOS

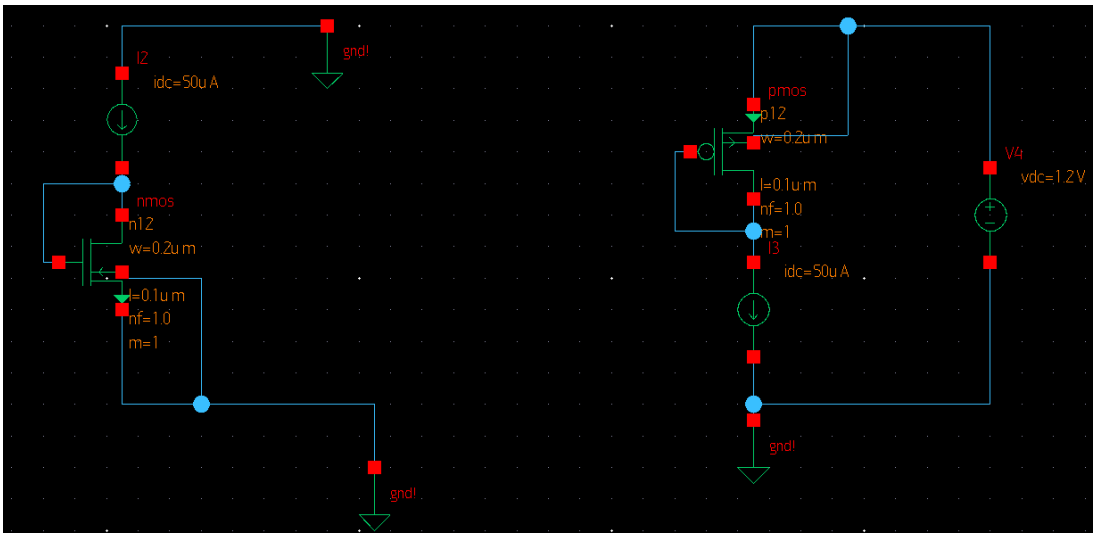

Figure 3.1: Circuit Diagram of Opamp

3.2 NMOS and PMOS Bias circuit

For calculating βeff and Vth values, we use the NMOS and PMOS bias circuit. To determine μnCox and μpCox for 90nm βeta = μ.Cox(W/L) Where βeta is the MOSFET transconductance effective factor, μ is the mobility of electrons and Cox is the oxide capacitance

We assume Width & Length based on library 90nm and model file TT12: Table 3.1

Proceed to run the operating point simulation of the diode-connected circuit to obtain the parameters. Schematic below Figure 3.1.

For calculating βeta and Vth values, we use the NMOS and PMOS bias circuit. To determine μnCox and μpCox for 90nm βeta = μ.Cox(W/L) Where μeta is the MOSFET transconductance effective factor, μ is the mobility of electrons and Cox is the oxide capacitance.

NMOS	PMOS
$\beta_n = 3.14 \times 10^{-3}$	$\beta_P = 0.29 \times 10^{-3}$
$K'_n = 1570\mu$	$K'_p = 150\mu$
$\mu_n C_{\text{ox}} = 3.14$	$\mu_p C_{\text{ox}} = 0.29$

Table 3.2: Process information values of NMOS and PMOS

Assume: $V_{DD} = 1.2\,\text{V}$ (Because we use model file TT-12) .

We have:

$V_{thn} = 0.3562\,\text{V}$

$V_{thp} = -0.2184\,\text{V}$

$\beta_n = \mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_n = 3.14\,\text{m}$

$\beta_p = \mu_n C_{\text{ox}} \cdot (W/L)_p = 0.29\text{m}$

$\implies \mu_n C_{\text{ox}} = 3.14 \times 10^{-3} : \left(\frac{0.2}{0.1}\right)_n = 1570\mu = K'_n$

$\implies \mu_p C_{\text{ox}} = 0.29 \times 10^{-3} : \left(\frac{0.2}{0.1}\right)_n = 150\mu = K'_p$

3.3 Design of Opamp

3.3.1 Calculator Schematic

The total gain of two stage CMOS Opamp is defined by Av. The corresponding equation is given by the product of Av1 and Av2.

Where Av1 is called as differential amplifier gain and Av2 is called as common source amplifier gain.

The overall voltage gain of the two-stage op-amp is given by:

$$A_v = A_{v1} \cdot A_{v2} \tag{3.3}$$

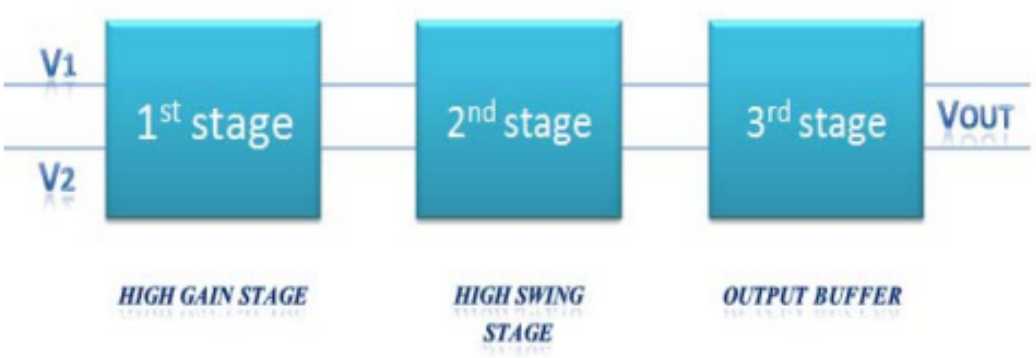

Figure 3.2: Source amplifier gain

where:

$$A_{v1} = \frac{V_{o1}}{V_{in}} \tag{3.4}$$

$$A_{v2} = \frac{V_{out}}{V_{o1}} \tag{3.5}$$

For a common-source amplifier, we have $V_{o1} = V_{in}$, so:

$$A_{v2} = \frac{V_{out}}{V_{o1}} \tag{3.6}$$

The transconductance of the MOSFETs is given by:

$$g_{m1} = \sqrt{2\beta_1 \cdot I_{ds1}} = \sqrt{2\beta_2 \cdot I_{ds2}} = g_{m2} \tag{3.7}$$

where $I_{ds1} = I_{ds2} = I_{ss}/2$ and I_{ss} is the total bias current.

Assuming that M_1 and M_2 are identical MOSFETs, we have:

$$g_{m1} = g_{m2} \tag{3.8}$$

For stability requirement, the phase margin should be greater than 45 degrees. This can be expressed as:

$$\frac{g_{m6}}{C_0} \geq 2.2\left(\frac{g_{m1}}{C_1}\right) \tag{3.9}$$

Rearranging, we get:

$$C_0 \geq \frac{2.2 g_{m1} C_1}{g_{m6}} \tag{3.10}$$

Additionally, we have the condition:

$$\frac{g_{m1}}{g_{m6}} \leq 0.1 \tag{3.11}$$

Combining the two conditions, we get:

$$C_0 \geq 0.22C_1 \tag{3.12}$$

From the slew rate requirement:

$$\left(\frac{dV_0}{dt}\right) \geq 10 \text{ V}/\mu\text{s} \tag{3.13}$$

and the relation $I_{DS7} = C_0\left(\frac{dV_0}{dt}\right)$, we have:

$$I_{DS1} = I_{DS2} = \frac{I_{SS}}{2} \tag{3.14}$$

Neglecting λ from the saturated transistor current, we have:

$$V_{GS} = V_t + \sqrt{\frac{2I_{DS}}{\beta\left(\frac{W}{L}\right)}} \tag{3.15}$$

For the input common-mode range (ICMR) evaluation:

$$V_{in,min} = V_{SS} + V_{dsat7} + V_{t1} + \sqrt{\frac{2I_{DS1}}{\beta_1\left(\frac{W}{L}\right)_1}} \tag{3.16}$$

$$V_{in,max} = V_{DD} - V_{t3} - \sqrt{\frac{2I_{DS3}}{\beta_3\left(\frac{W}{L}\right)_3}} - V_{DS1} + V_{GS1} \tag{3.17}$$

Using the relation $V_{dsat} = V_{GS} - V_t$, we can express $V_{in,max}$ as:

$$V_{in,max} = V_{DD} - V_{tp3} + V_{tn1} - \sqrt{\frac{2I_{DS3}}{\beta_3\left(\frac{W}{L}\right)_3}} \tag{3.18}$$

Assuming M_1 and M_2 are identical, we have:

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 \tag{3.19}$$

From the gain-bandwidth (GBW) requirement:

$$\text{GBW} = \frac{g_{m1}}{C_1} = \frac{g_{m2}}{C_0} \tag{3.20}$$

Finally, for the output stage transistor M_8:

$$\frac{dI_{DS8}}{dV_{GS8}} = g_{m8} \tag{3.21}$$

$$= \beta_p 8(V_{GS8} - V_{t8}) \tag{3.22}$$

$$= \beta_p 8 V_{dsat8} \tag{3.23}$$

Therefore,

$$\left(\frac{W}{L}\right)_8 = \frac{g_{m8}}{\beta_p 8 V_{dsat8}} \tag{3.24}$$

where $V_{dsat8} = V_{DD} - V_{out,max}$. Similarly, the channel width to length ratios for the other transistors can be calculated as follows:

et's define a function f(x, y) such that:

f(x, y) = $\left(\frac{W}{L}\right)_x = \left(\frac{W}{L}\right)_y$

Then, we can express the given relationships as:

f(3, 4) = $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$

f(7, 8) = $\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_8$

Additionally, we have:

f(1, 2) = $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$

3.3.2 Schematic of Two-Stage Opamp

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Chapter 4

Schematic & Testbench & Layout

4.1 Schematic and Symbol of Two-Stage Opamp

4.1.1 Schematic of Two-Stage Opamp

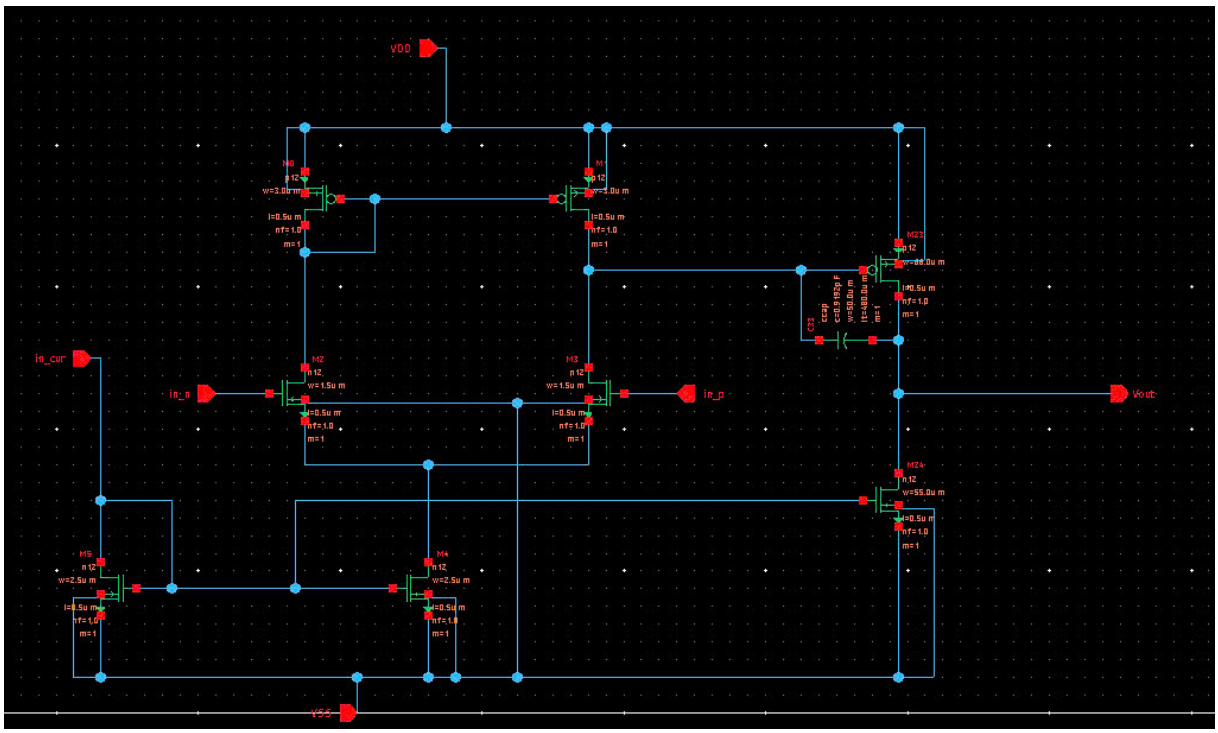

Figure 4.1: Schematic of two stage Opamp

4.1.2 Symbol of Two-Stage Opamp

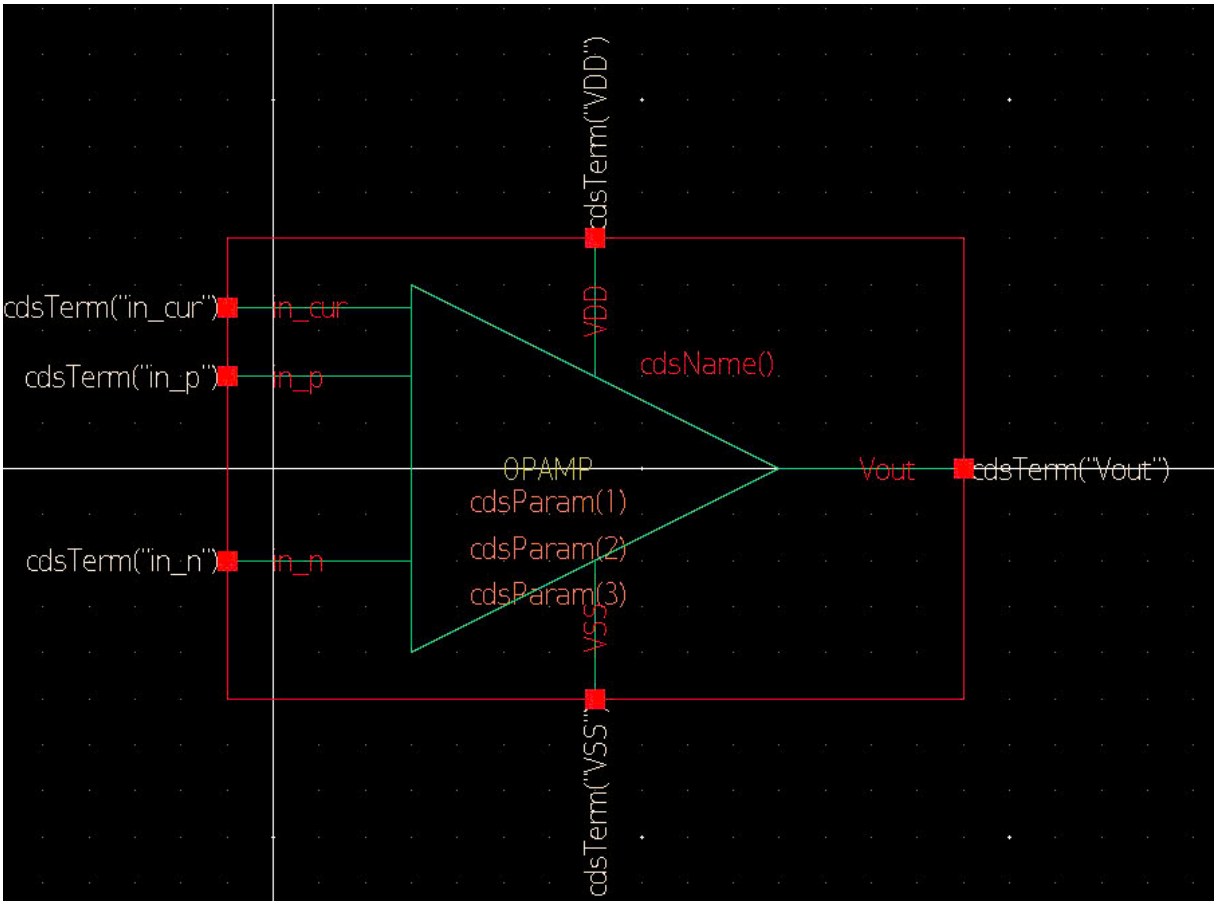

Figure 4.2: Symbol of two stage Opamp

4.2 The Testbench of two stage Opamp

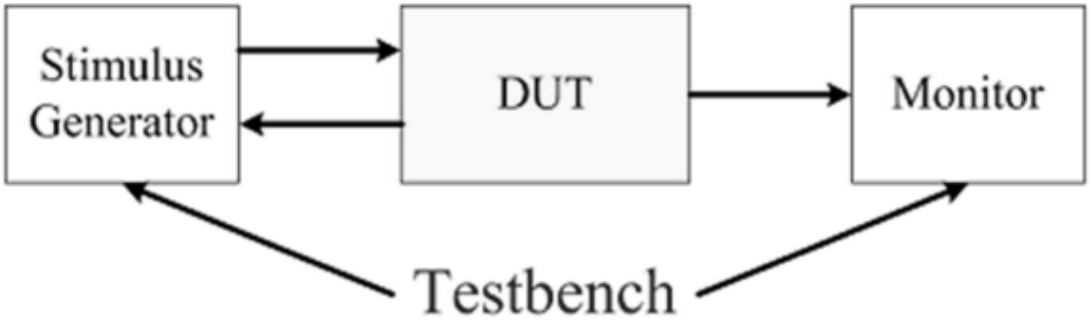

Figure 4.3: Testbench of two stage Opamp

4.2.1 Testbench AC of two stage Opamp

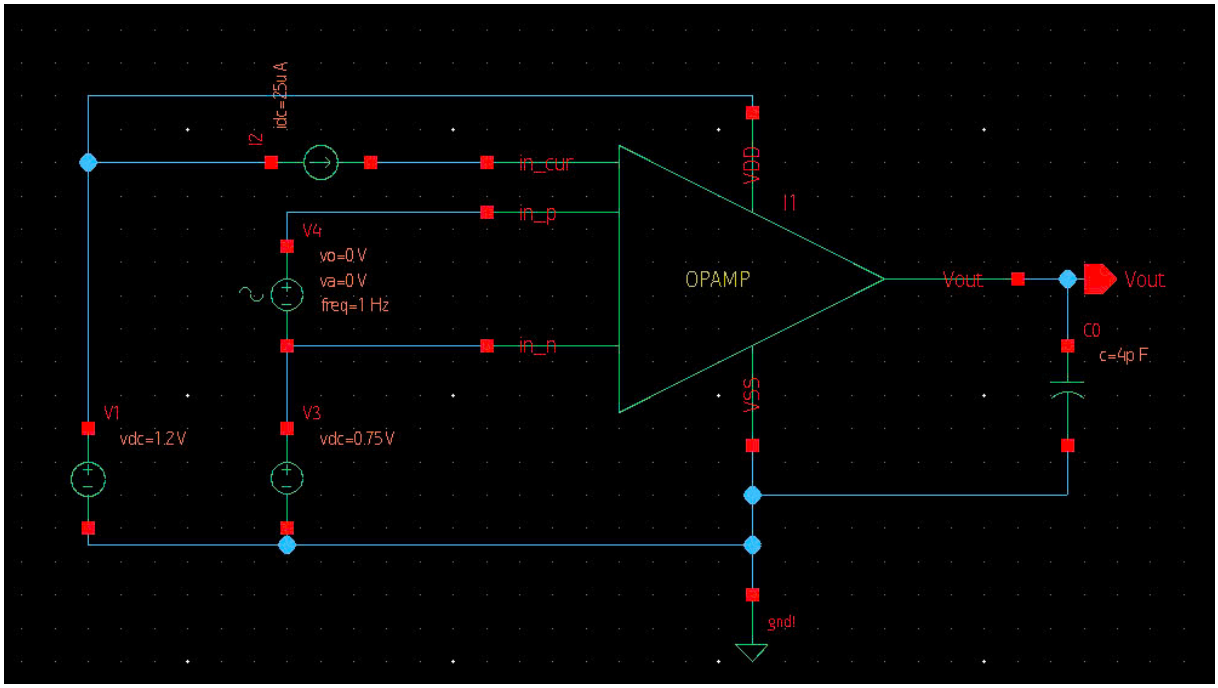

Figure 4.4: Testbench AC of two stage Opamp

4.2.2 Testbench Transient of two stage Opamp

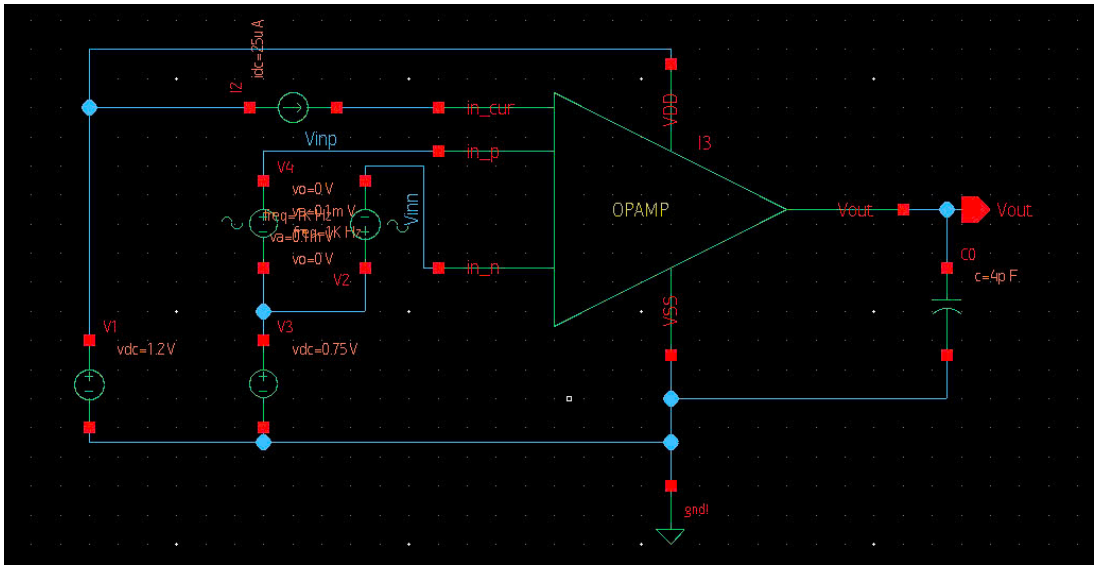

Figure 4.5: Testbench Transient of two stage Opamp

4.2.3 Transient of two stage Opamp

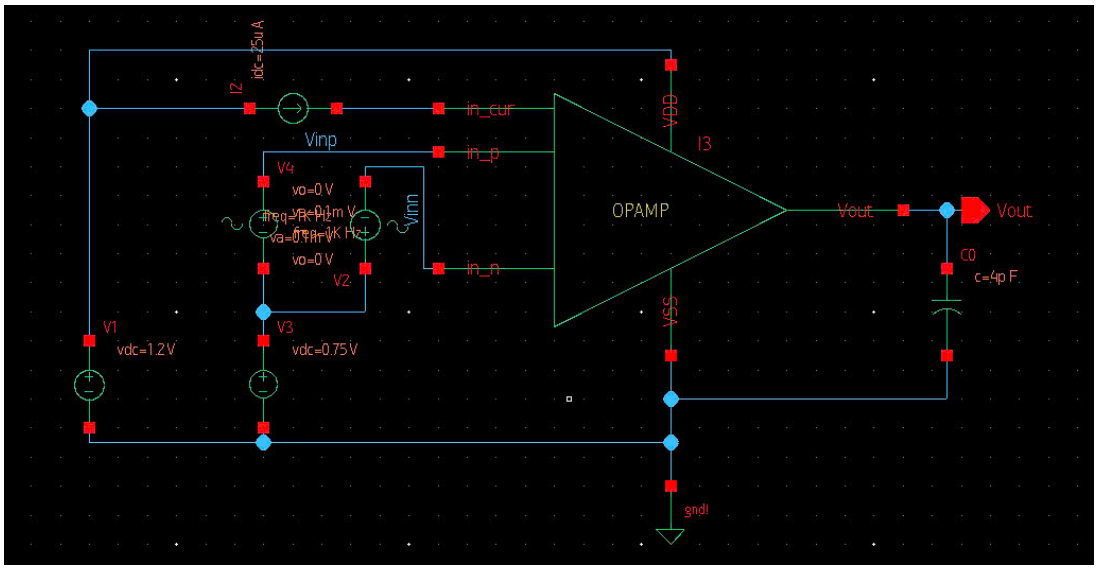

Figure 4.6: Transient of two stage Opamp

4.2.4 Transient response of two stage Opamp

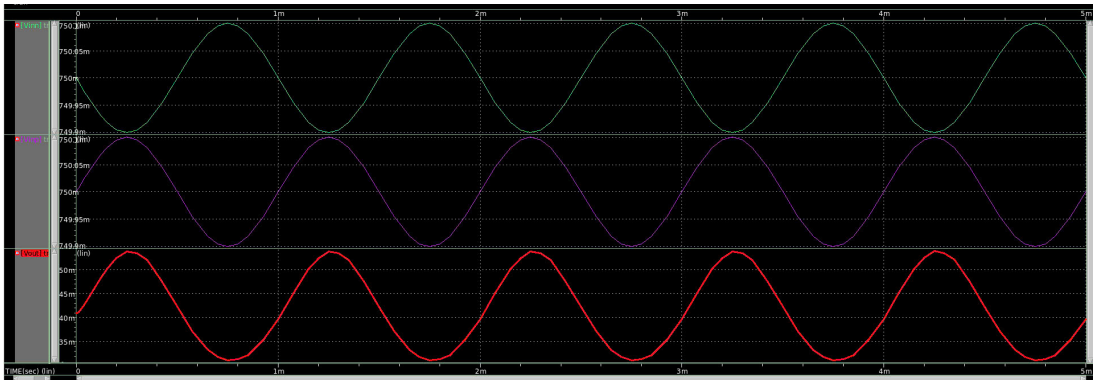

Figure 4.7: Transient response of two stage Opamp

4.3 Layout

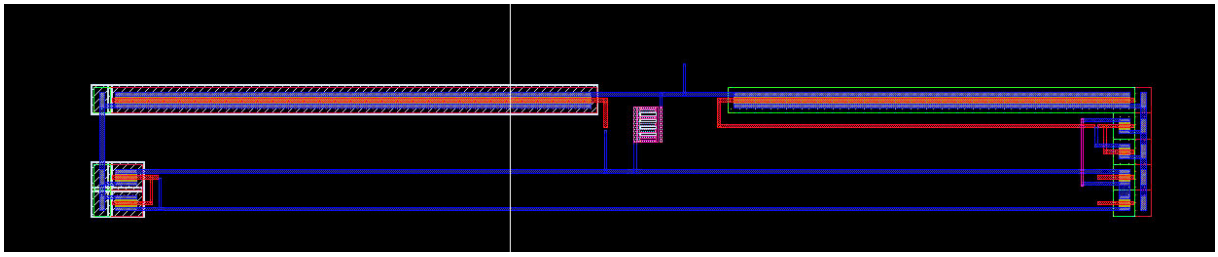

Figure 4.8: Layout of two stage Opamp

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Chapter 5

Conclusion and future development of the topic

5.1 Conclusion

The simulation has been carried out using Custom Compiler Synopsys with 90nm technology. The gain has been increased by optimizing the parameters like (W/L) values. Using the design equations, by choosing and carefully sizing the structure of the circuit. The design performs a gain of 84db with phase margin of 560 under unity gain feedback configuration and the power dissipation is of 38.02μW.

5.2 Future work

In future work, further enhancements can be made to improve the overall performance of the circuit. Some potential areas of focus include:

1. **Technology Scaling:** Exploring the impact of using more advanced technology nodes (e.g., 65nm, 45nm) on the gain, phase margin, and power dissipation of the circuit.
2. **Temperature Variability:** Investigating the circuit's performance across different temperature ranges to ensure reliability under various operating conditions.
3. **Noise Reduction:** Implementing advanced noise reduction techniques to improve

the signal-to-noise ratio, which could further enhance the circuit's performance in sensitive applications.

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