Tin Thurein

EIT License: 166315 · Electrical Engineer · Hardware Enthusiast

San Francisco

415-699-1146 tin.thurein@outlook.com in/tinthurein github.com/tthurein tthurein.github.io

Summary

Highly motivated electrical engineer with expertise in Electrical, Mechanical, and Communication engineering with hands-on experience focused on solving challenges in energy, transportation, and sustainability.

Skills

- **Software Engineering:** C,C++, Python, Java, VHDL
- **H/W Engineering:** Xilinx FPGA, Analog, Mixed Signal & Power electronics circuit design, Logic Design, DSP, Circuit & PCB Simulation
- **Embedded Systems:** AVR, STM32, PIC, CAN, I2C, UART, SPI, SpW, JESD204, Sensor interface, Protocol debugging hardware
- **Software:** Orcad, Allegro PCB Design, Eagle CAD, Mentor Graphics Xpedition, SPICE, HyperLynx, Vivado, National Instrument Circuit Suite, SolidWorks, Autodesk Inventor, MATLAB

Professional Experience

Sr. R&D Electrical Engineer *at Sandia National Laboratories* **Livermore, CA** *08/2023 - present*

- Hardware engineer for high-speed, high-performance telemetry interfacing board.

Electrical Design Engineer *at KLA-Tencor* **Milpitas, CA** *06/2022 - 08/2023*

- Designed functional test fixtures (FUT) for stage motion controller PCBs, integrating high-speed ADCs, DACs, LVDS transceivers, and digital communication protocols including UART, SPI, and I2C to interface with FPGA.
- Developed embedded firmware and libraries for Functional Test Fixtures (FUT) and FPGA test-mode firmware.
- Authored Interface Control Document (ICD) specifications, and maintained Python scripts for automating test procedures and GUI.
- Conducted SPICE simulations, Power and Signal Integrity analyses utilizing HyperLynx.
- Designed high-speed stage motion controller board, managing the entire PCB design cycle from schematics capture, reviewing layout, PCB manufacturing to hardware bring-up and functional verification.

Sr. Reliability Hardware & ESD/Latch-up Engineer *at Analog Devices* **Milpitas, CA** *07/2019 - 06/2022*

- Responsible for reliability circuit designs and test setup development for accelerated testing of packaged and wafer-level chip-scale packaged devices.
- Developed and implemented reliability test plans for new products, including High-Temperature Operating Life (HTOL), Highly Accelerated Temperature and Humidity Stress (HAST), and Early Life Failure Rate (EFLR) tests.
- Troubleshooted PCB boards to identify root causes of failures occurring during burn-in or HAST cycles.
- Defined and developed ESD and Latch-up methodologies for new, existing, and fab-transferred products, ensuring characterization of ESD and Latch-up properties in accordance with JESD and AECQ standards.
- Developed and executed ESD/Latch-up device characterization plans, and conducted comprehensive data analysis on ESD/Latch-up related failures.

Engineering: R&D Product Development *at Nordson March* **Concord, CA** *10/2017 - 07/2019*

- Responsible for integrating EFEM (Equipment Front End Module) systems with plasma modules.
- Configured high-power RF generators and RF matching networks, and developed process recipes for various plasma and chemical deposition applications.
- Designed and tested new vacuum chambers and High-Flux Electrode (HFE) configurations.
- Enhanced process cycle time for customers by developing process recipes and optimizing RF power delivery systems and RF matching networks, achieving superior plasma treatment, uniformity, and throughput.
- Conducted Factory Acceptance Tests (FAT), trained customers, and performed QA and QC procedures on product shipments.

Education

M.S. in Electrical Engineering *at University of California, Santa Cruz* **Santa Cruz, CA** *2020-2022*

Research Areas: Neuromorphic computing, Memristors, Spiking Neural Networks, Memristive Integrate-and-Fire

B.E. in Electrical Engineering *at University of California, Santa Cruz* **Santa Cruz, CA** *2017-2019*

Concentration: Electronics/ Optoelectronics