

Tin Thurein

EIT LICENSE: 166315 · ELECTRICAL ENGINEER · HARDWARE ENTHUSIAST

San Francisco, CA

☎ (+1) 415-699-1146 | ✉ tinthurein@outlook.com | 🏠 tthurein.github.io | 📷 tthurein | 🌐 tinthurein

Summary

Highly motivated electrical engineer who possesses Electrical, Mechanical and Communication engineering knowledge with hands-on experience, with a focus on finding solutions to the energy, transportation, and sustainability problems.

Professional Experience

KLA-Tencor

Milpitas, CA

ELECTRICAL DESIGN ENGINEER

06/2022 - Present

- Design functional test fixtures (FUT) for stage motion controller PCBs using high-speed ADCs, DACs, LVDS transceivers, and other digital protocols such as UART, SPI, and I2C.
- Perform SPICE simulations, PI/SI analysis using HyperLynx, schematic capture, layout design and review, hardware bring-up, and initial board-level testing and verification.
- Develop embedded firmware and libraries for FUT, FPGA test-mode firmware, and maintain python scripts for automating test procedures and GUI.
- Define test parameters and FPGA registers, interface control document (ICD) specification, and component selection.

Analog Devices

Santa Clara, CA

SR. RELIABILITY HARDWARE & ESD/LATCH-UP ENGINEER

07/2019 - 06/2022

- Responsible for developing and implementing reliability test plans for new products, conducting accelerated testing of packaged and wafer-level chip-scale packaged devices including board designs and setup of reliability tests.
- Troubleshoot PCB boards and component level failures occurring during burn-in or HAST cycles.
- Define and develop ESD and Latch-up methodologies for all new, existing, and fab transferred products to characterize ESD & Latch-up properties per JESD & AECQ standards.
- Generate ESD/Latch-up device characterization plans and perform data analysis on ESD/Latch-up related failures.

Nordson March

Concord, CA

ENGINEERING: R&D PRODUCT DEVELOPMENT

10/2017 - 07/2019

- Built and tested new vacuum chamber and HFE (High-Flux Electrode) designs, configured high power RF generators along with RF matching networks, and developed process recipe configurations for various plasma applications and chemical depositions.
- Improved process cycle time for customers by developing process recipes, optimizing RF power delivery systems, and RF matching networks for the highest plasma treatment, uniformity, and throughput.

Skills

- **Software Engineering:** C, C++, Java, Python, MIPS, Verilog, PLC, HMI
- **Engineering:** FPGA/ CPLD, Analog/ Power Electronics, Logic Design, DSP, Optical Communication, Analog & Digital Communication, PCB, Circuit Simulation
- **Embedded Systems:** I2C, UART, SPI, MicroControllers, Sensors, Protocol debugging hardware
- **Software:** SolidWorks, Autodesk Inventor, MATLAB, Allegro PCB Design, Cadence Suite, HyperLynx, LTSPICE, Eagle CAD, National Instrument Circuit Suite.

Education

UC Santa Cruz

Santa Cruz, CA

M.S. IN ELECTRICAL ENGINEERING

09/2020 - 03/2022

- **Research Areas:** Neuromorphic computing, Memristors, Spiking Neural Networks, Memristive Integrate-and-Fire

UC Santa Cruz

Santa Cruz, CA

B.S. IN ELECTRICAL ENGINEERING

09/2015 - 06/2017

- **Concentration:** Electronics/ Optoelectronics

Projects

HAST and Burn-in oven DUT monitoring system

- Designed power distribution controller boards, wireless GPIB cards for scopes, as well as interface cards for in-situ DUT voltage and current monitoring, and custom vector drivers.
- Responsible for developing GUI written in java, firmware in micropython, and system-level automation implementation over a wide range of HAST and Burn-in ovens.

High speed, Low power 16:1 Mux

- Collaborated with design engineer to design a 16-bit multiplexer with bandgap reference and internal LDOs for low-power operation.
- Other responsibility included: analyzing switching times, leakage current, bandwidth and $R_{ds\ ON}$.