

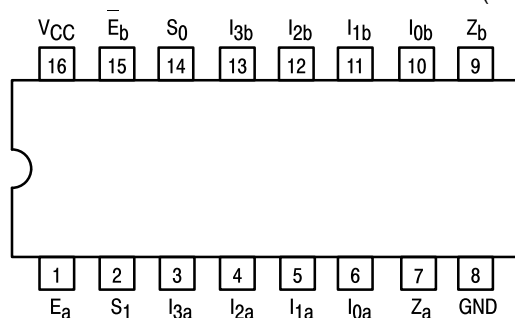


# DUAL 4-INPUT MULTIPLEXER

The LSTTL/MSI SN54/74LS153 is a very high speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the LS153 can generate any two functions of three variables. The LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Multifunction Capability
- Non-Inverting Outputs
- Separate Enable for Each Multiplexer
- Input Clamp Diodes Limit High Speed Termination Effects

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

## PIN NAMES

$S_0$  Common Select Input  
 $E$  Enable (Active LOW) Input  
 $I_0, I_1$  Multiplexer Inputs  
 $Z$  Multiplexer Output (Note b)

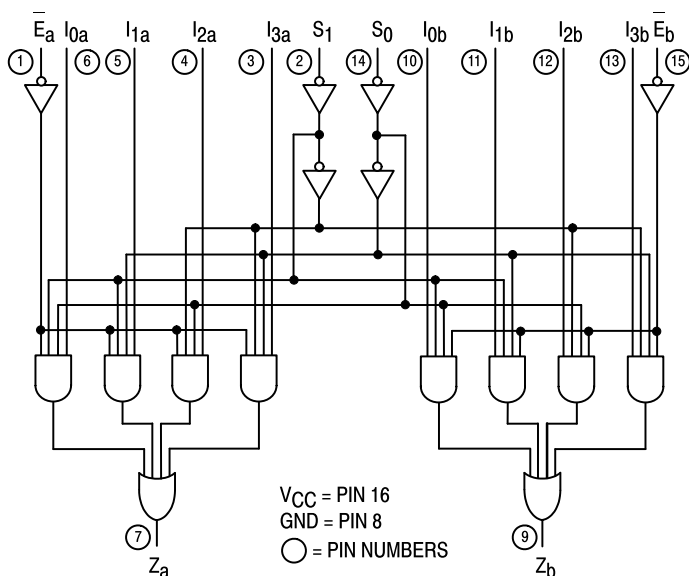
## LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.

## NOTES:

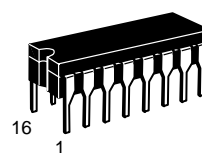
- a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

## LOGIC DIAGRAM

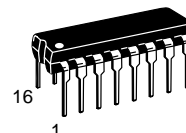


# SN54/74LS153

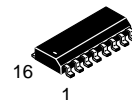
## DUAL 4-INPUT MULTIPLEXER LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

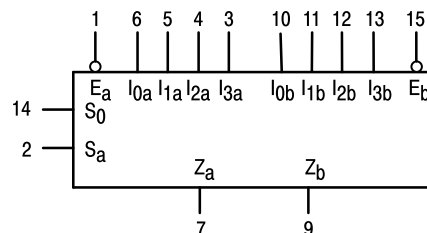


**D SUFFIX**  
SOIC  
CASE 751B-03

## ORDERING INFORMATION

SN54LSXXXJ Ceramic  
 SN74LSXXXN Plastic  
 SN74LSXXXD SOIC

## LOGIC SYMBOL



$V_{CC}$  = PIN 16  
 $GND$  = PIN 8

# SN54/74LS153

## FUNCTIONAL DESCRIPTION

The LS153 is a Dual 4-input Multiplexer fabricated with Low Power, Schottky barrier diode process for high speed. It can select two bits of data from up to four sources under the control of the common Select Inputs ( $S_0$ ,  $S_1$ ). The two 4-input multiplexer circuits have individual active LOW Enables ( $E_a$ ,  $E_b$ ) which can be used to strobe the outputs independently. When the Enables ( $E_a$ ,  $E_b$ ) are HIGH, the corresponding outputs ( $Z_a$ ,  $Z_b$ ) are forced LOW.

The LS153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The LS153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The LS153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
$S_0$	$S_1$	$E$	$I_0$	$I_1$	$I_2$	$I_3$	$Z$
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
$T_A$	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
$I_{OH}$	Output Current — High	54, 74			-0.4	mA
$I_{OL}$	Output Current — Low	54 74			4.0 8.0	mA

# SN54/74LS153

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage			−0.65	−1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = −18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.7	3.5		V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	I <sub>OL</sub> = 8.0 mA	
I <sub>IH</sub>	Input HIGH Current				20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
					0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current				−0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)		−20		−100	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current				10	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output			10 17	15 26	ns	Figure 2	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PLH}$ $t_{PHL}$	Propagation Delay Select to Output			19 25	29 38	ns	Figure 1	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output			16 21	24 32	ns	Figure 2	

## AC WAVEFORMS

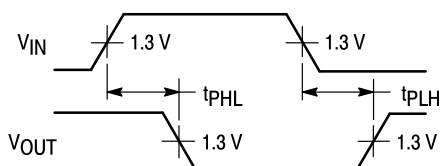


Figure 1

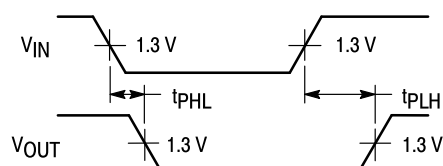
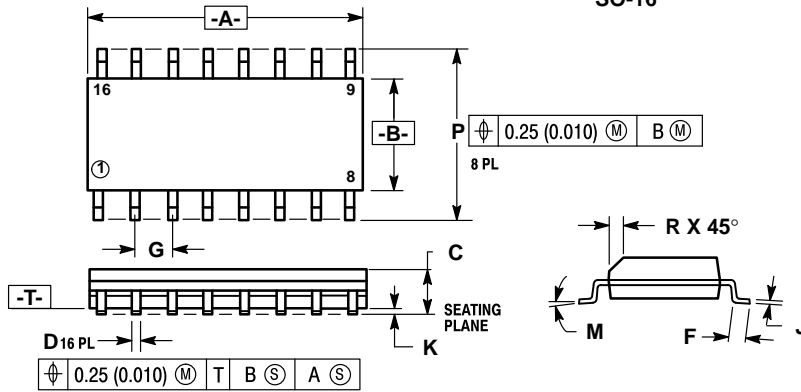


Figure 2

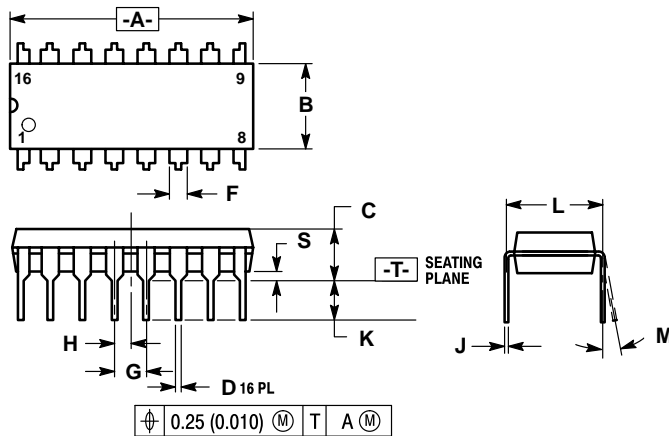
**Case 751B-03 D Suffix**  
**16-Pin Plastic**  
**SO-16**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

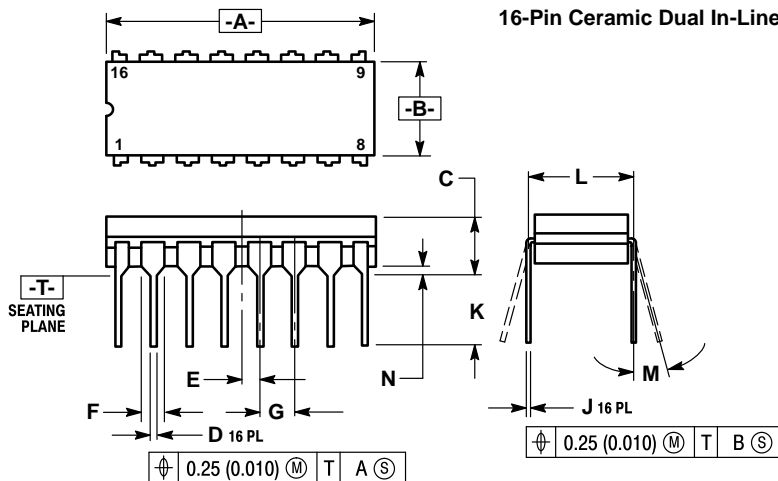
**Case 648-08 N Suffix**  
**16-Pin Plastic**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.
  6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

**Case 620-09 J Suffix**  
**16-Pin Ceramic Dual In-Line**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
  5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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