LSI Design (fundamentals)

BF001

To learn behavior of MOS transistors and circuits is essential before starting LSI designs

Tsuneo Funabashi
tsuneo.funabashi.zc@renesas.com
1st Design & Development Support Department
(concurrent)
Technology Planning Department

thanh.tran.jz@renesas.com
(add my email to your report today)

Renesas Electronics Corporation
Technology Planning Div.
Technology Development Unit

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Contents

Guideline of this course

1. Intended audience

h/w and s/w engineers who have mastered science and engineering

2. Purpose of this course

*** to understand common sense (basic, but much information)**

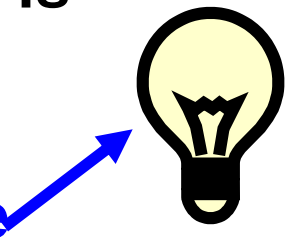
*** to fill knowledge gap between automated designs and actual device behavior**

3. Recommendations

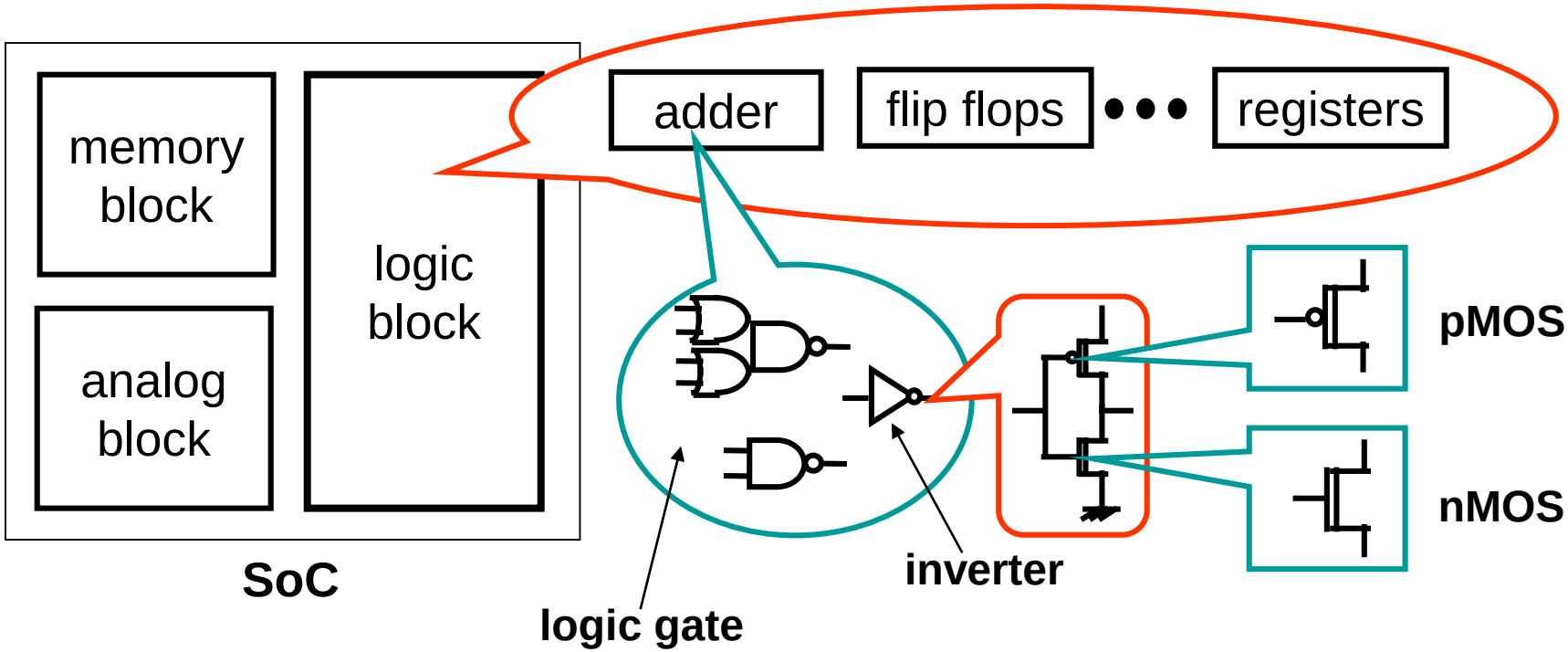
*** to memorize every information in this course is NOT necessary**

*** but to recall it in your future design activities**

*** the light symbol indicates the important slide**



SoC Hierarchy



BF001

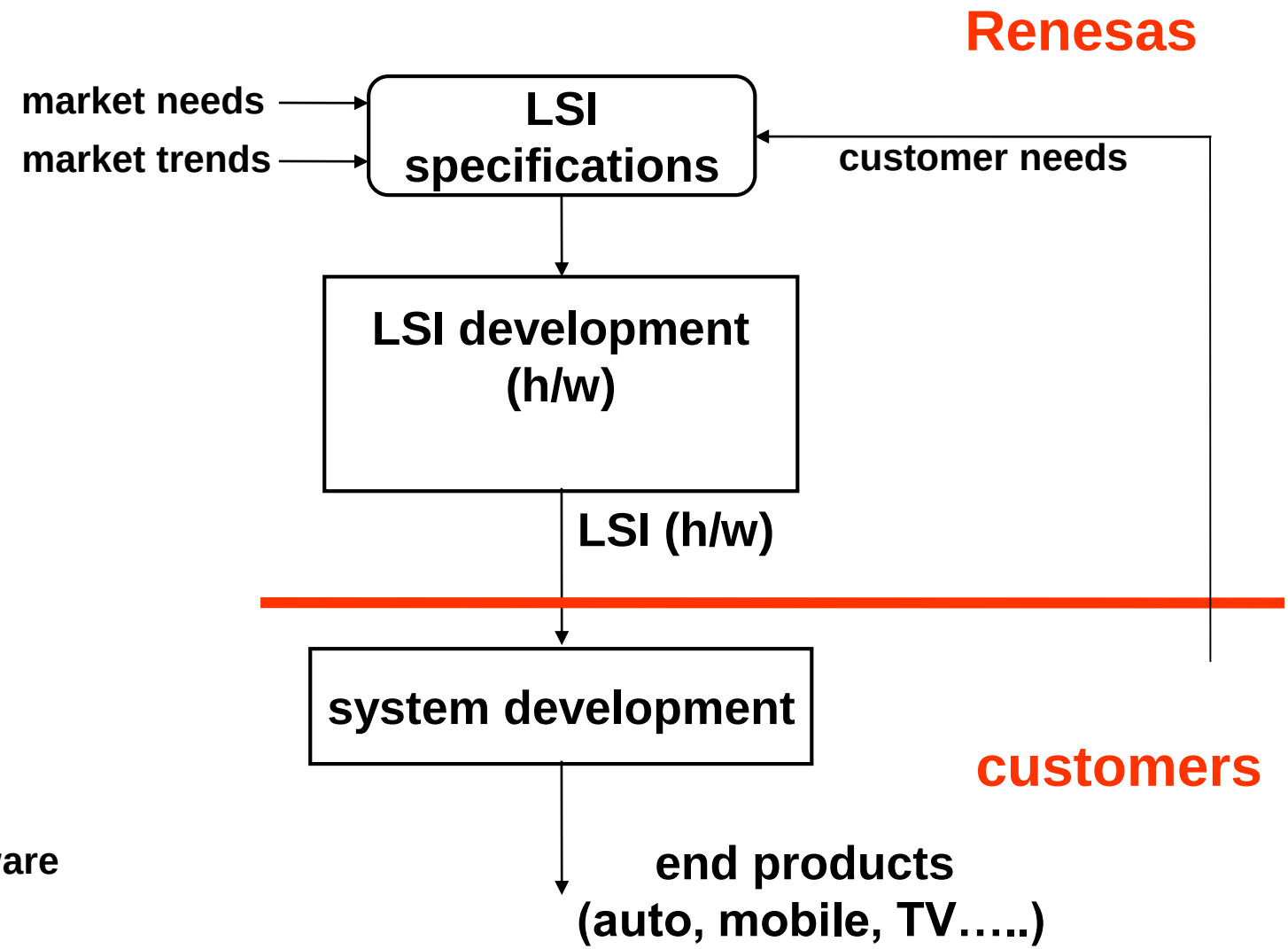
What is LSI design?

LSI design is intended to form semiconductor circuits on a silicon chip to meet growing market needs for performance and features within reasonable time frame and price range.

Design goals

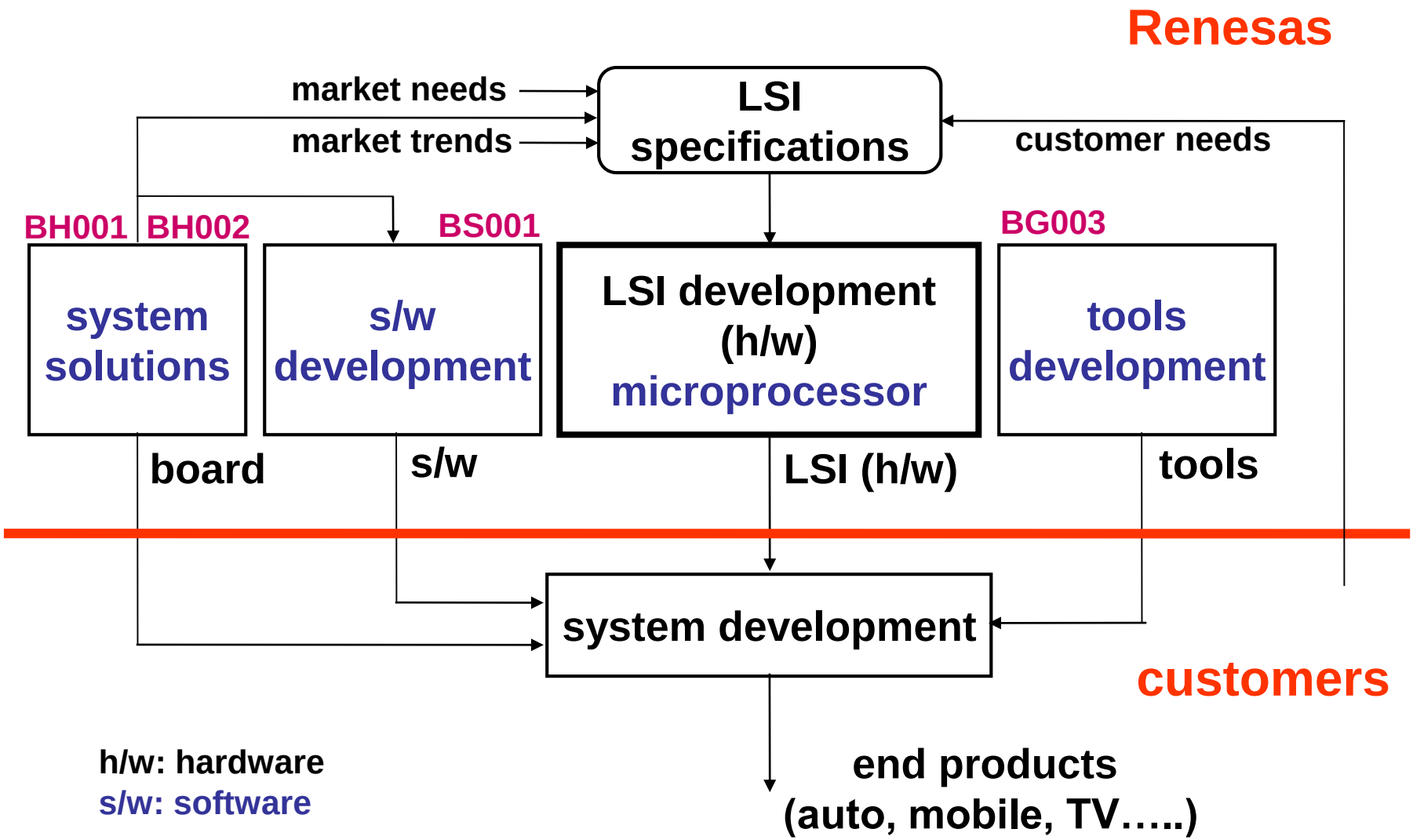
- **functional**
- **performance**
- **time-to-market**
- **profitable**

Activities of Renesas (1)

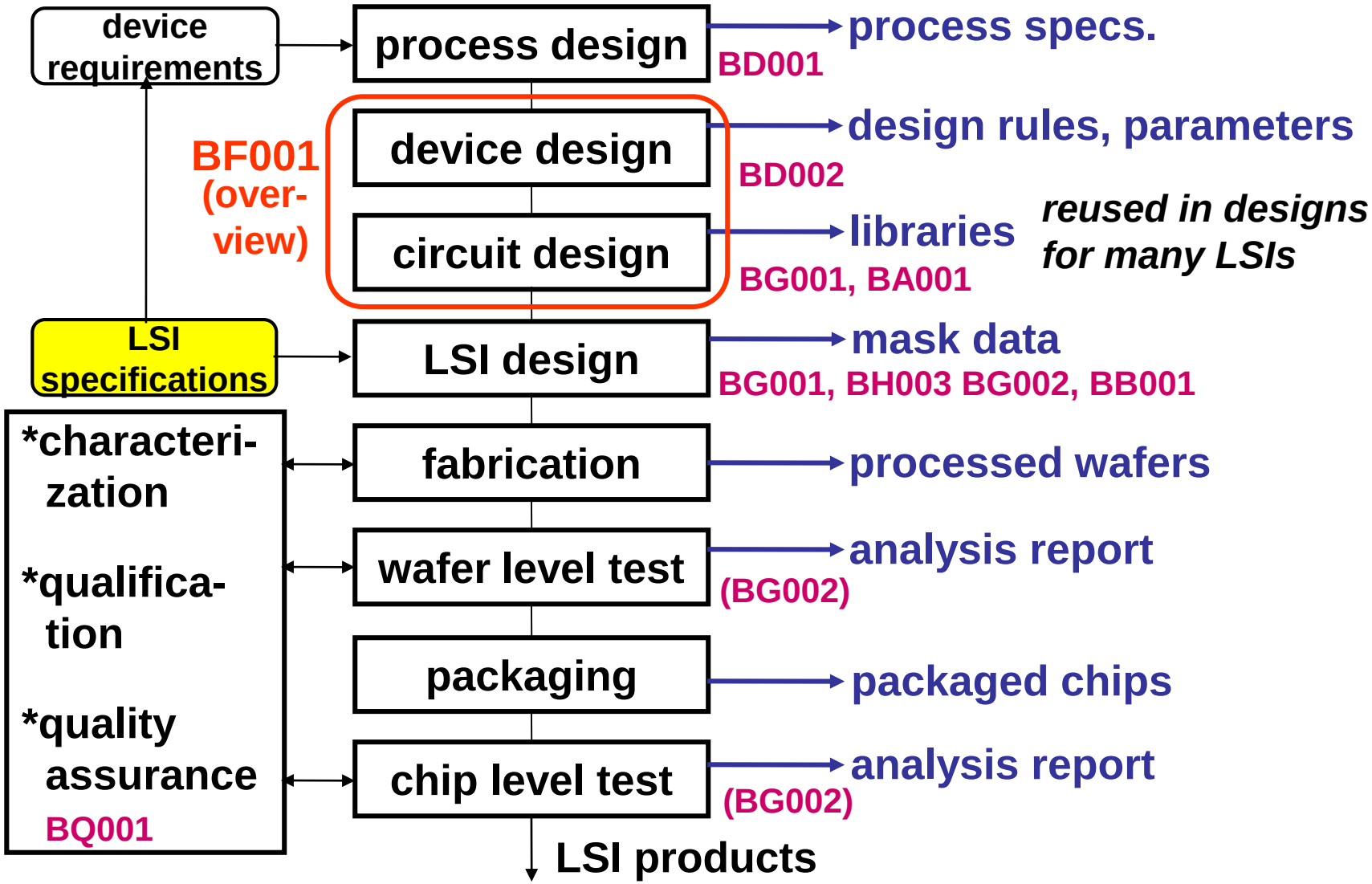


h/w: hardware

Activities of Renesas (2)



LSI Development

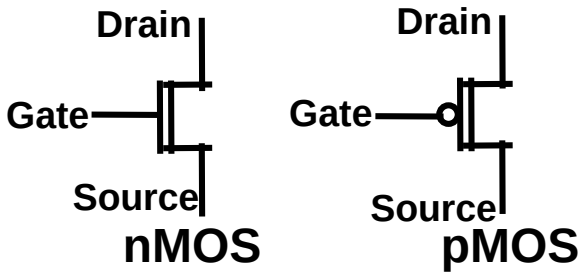


Contents

Devices Implemented in LSI

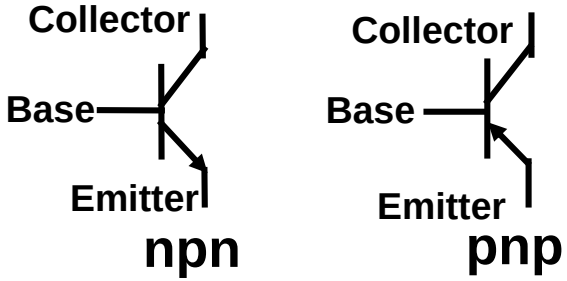
○ MOS Transistor

Broadly used owing to the properties of high-speed, low-voltage, and high-integration.



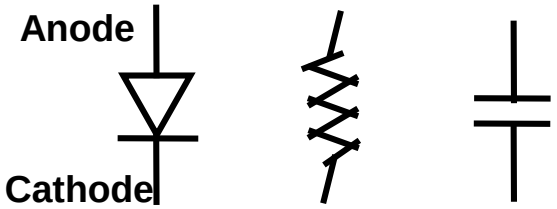
○ Bipolar Transistor

Used in RF and analog applications owing to its high-driveability.



○ Other devices

Diode, resistors, capacitors etc.

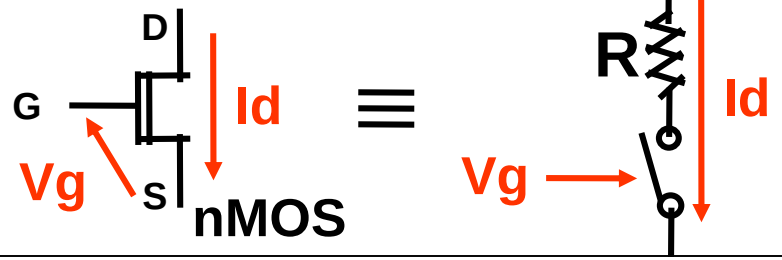


MOS: Metal Oxide Semiconductor

Simplified Operations of semiconductors

"s" is eliminated: Vg, Vd, Id
Vg = Vgs; Vd = Vds; Id = Ids

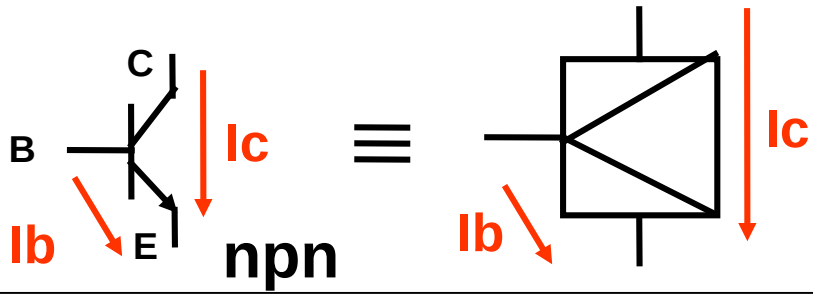
MOS Transistor



Switch

Vg >>0 : ON
Vg ≅ 0 : OFF

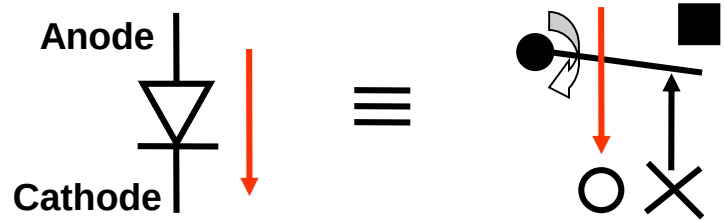
Bipolar Transistor



Magnifier

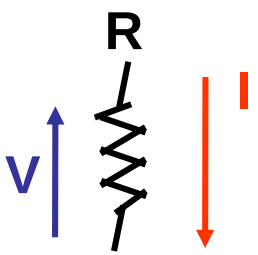
Ic=hfe x Ib
(hfe: constant)

Diode

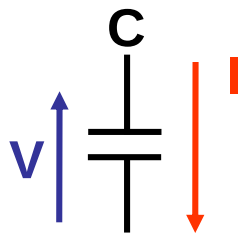


Single Swinging Door

Passive Devices

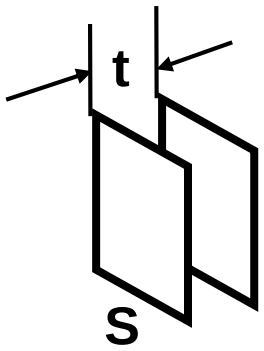


$$V = I \times R$$



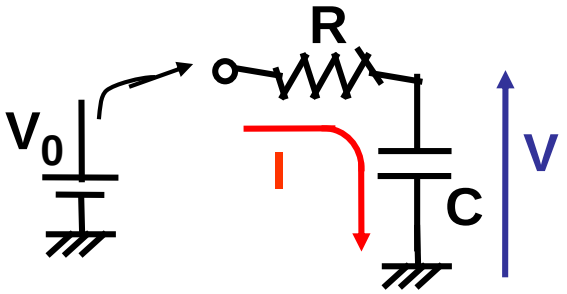
$$Q = C \times V$$

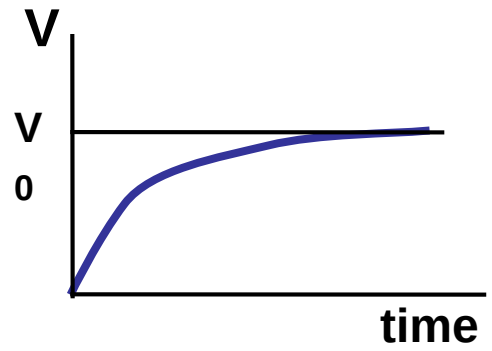
$$I = \frac{dQ}{dt} = C\frac{dV}{dt}$$

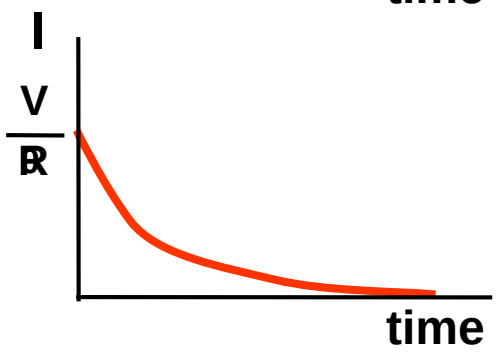


$$C = a \times \frac{S}{t}$$

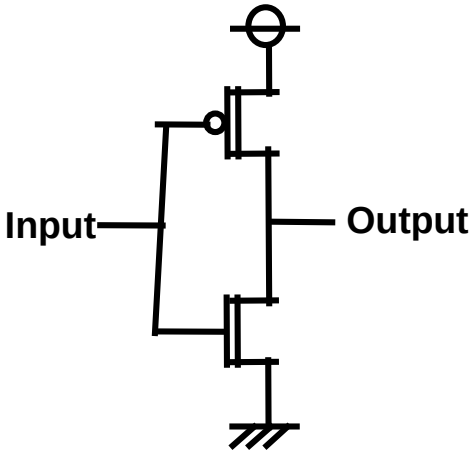
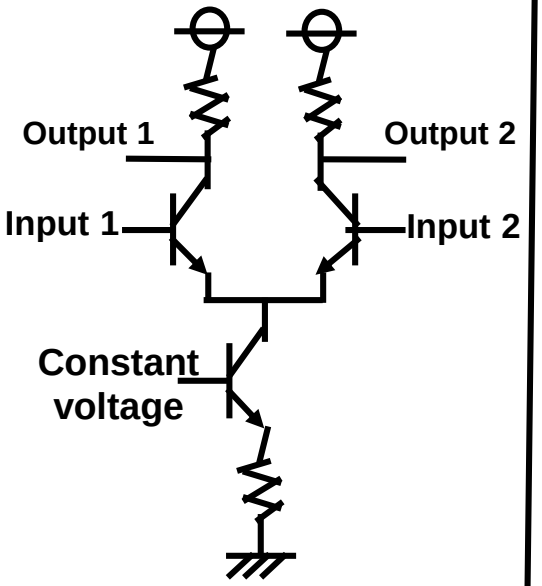
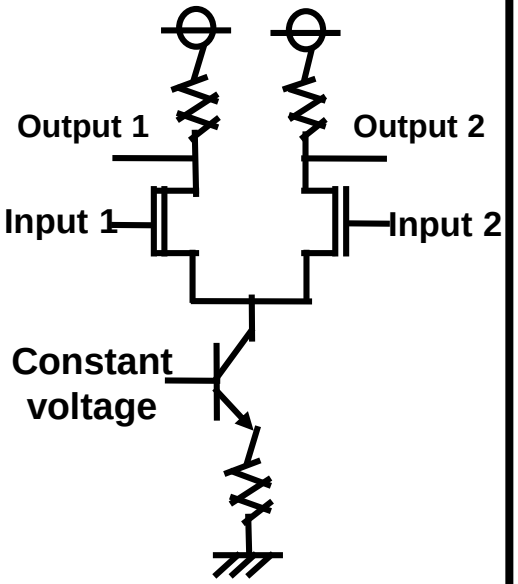
(a: constant)







Circuits configured in LSI

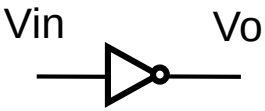
CMOS Circuit	Bipolar Circuit	BiCMOS Circuit
		
Entirely applicable to any LSI	Applicable to analog, ultra-high speed (RF) LSI	Applicable to analog, ultra-high speed (RF) LSI

CMOS: Complementary MOS

Logic Circuit on Silicon Chip

Inverter

<cell symbol>



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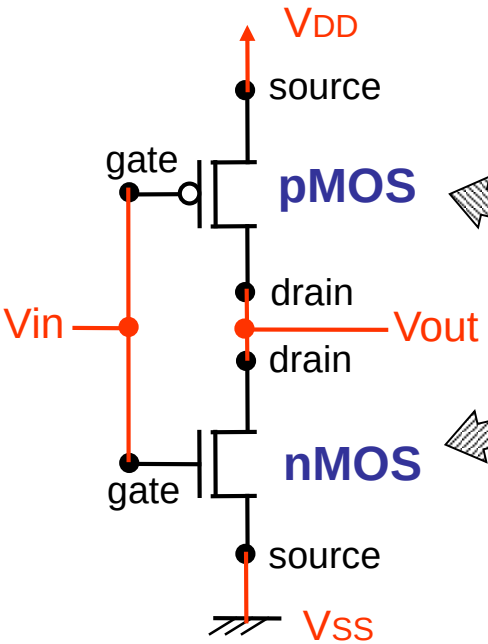

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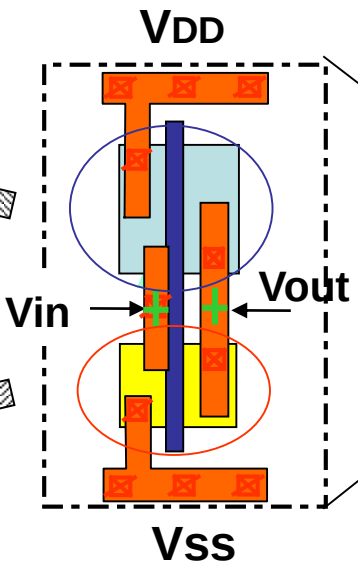
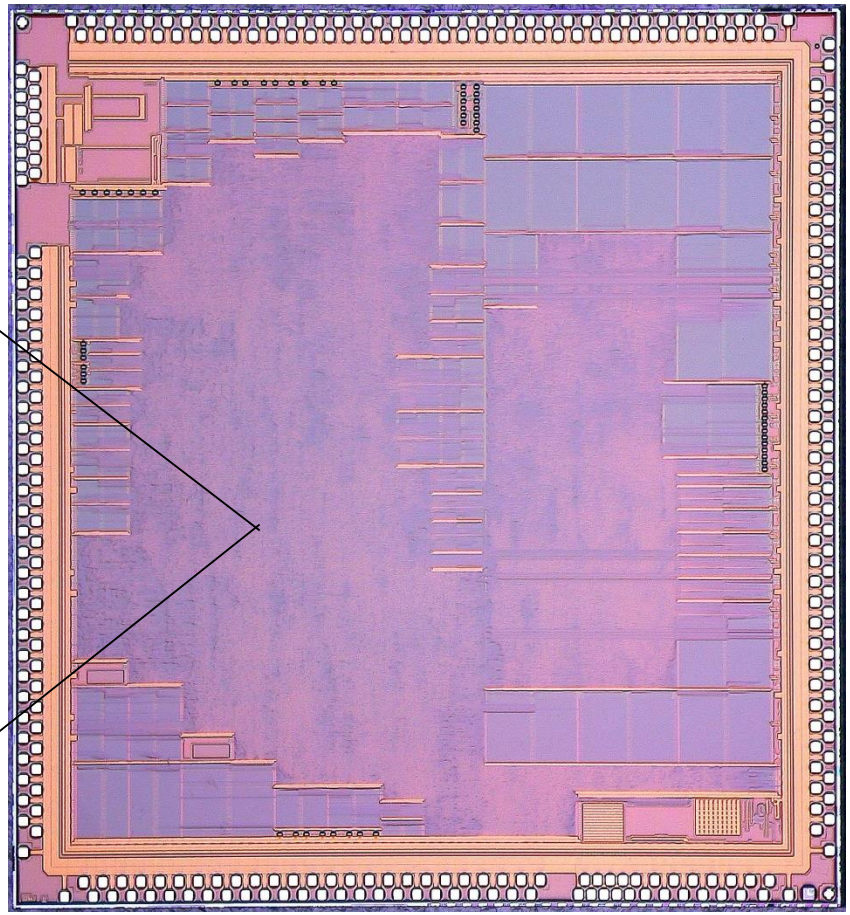
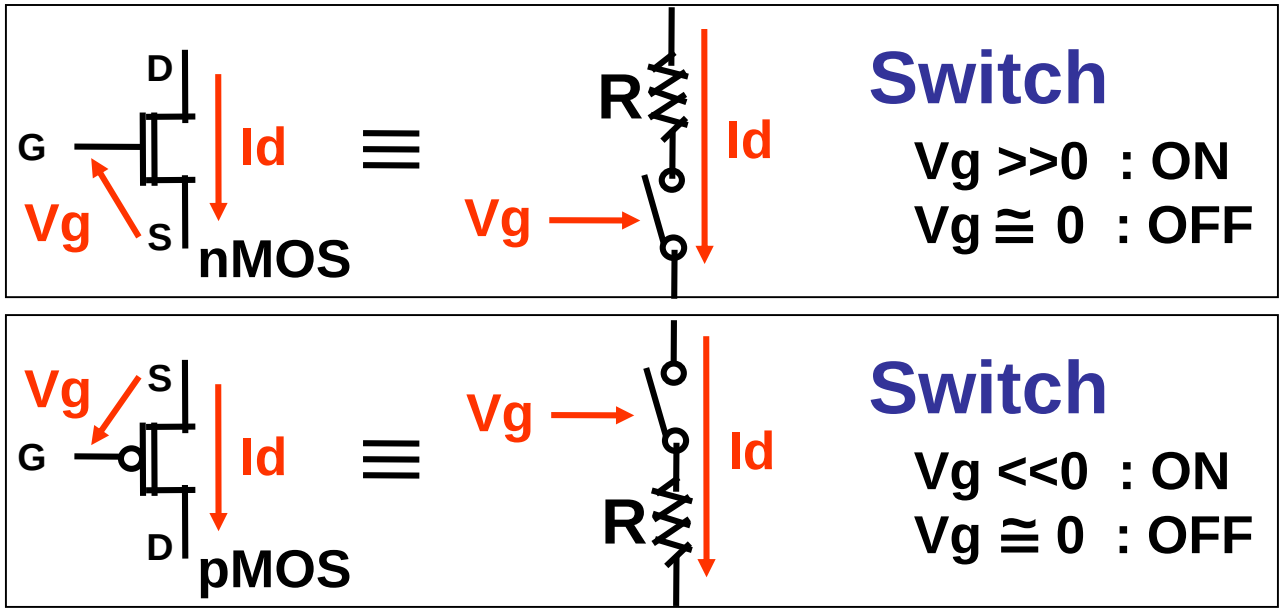


<CMOS die photo>

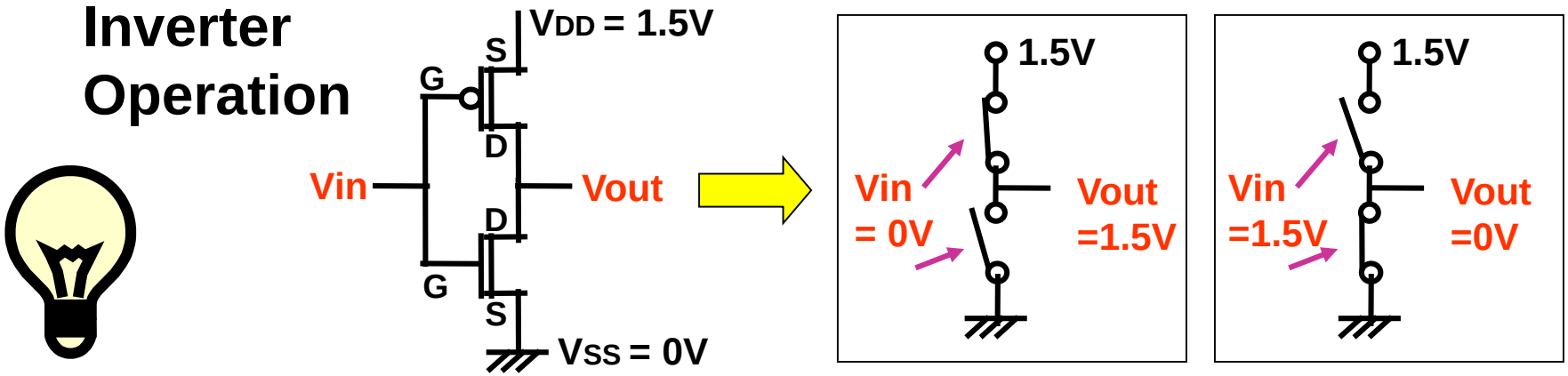


Simplified Operation of Inverter

MOS Switches



Inverter Operation



Contents

3.1 MOS Physics

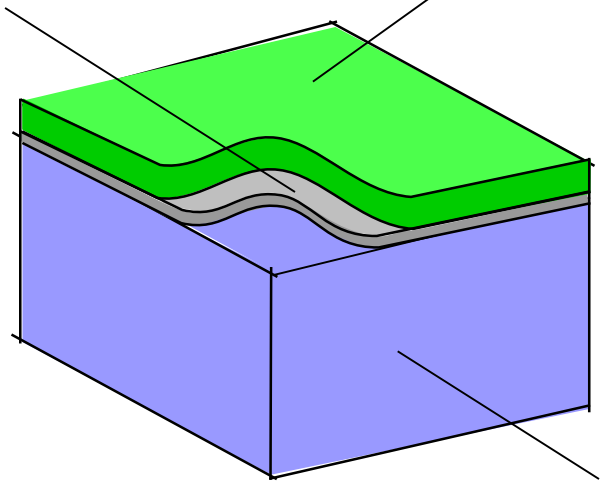
- **MOS Capacitor**
- **MOSFET**

These will be further lectured in BD002.

MOS Capacitor

Oxide (insulator)

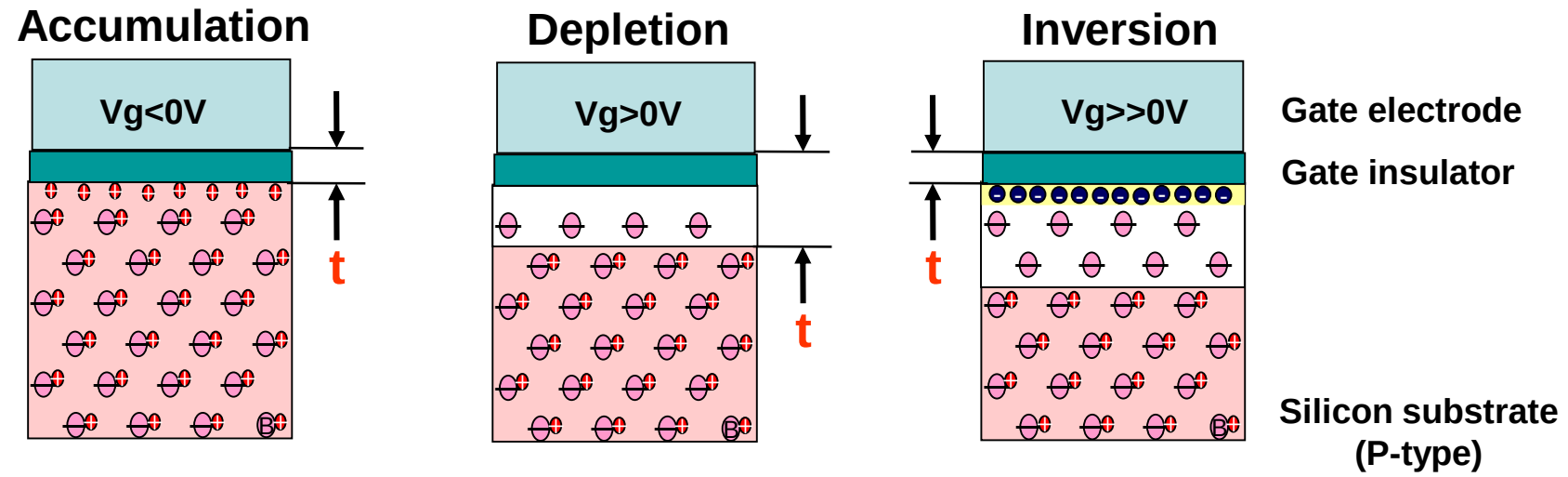
Metal* (gate electrode)

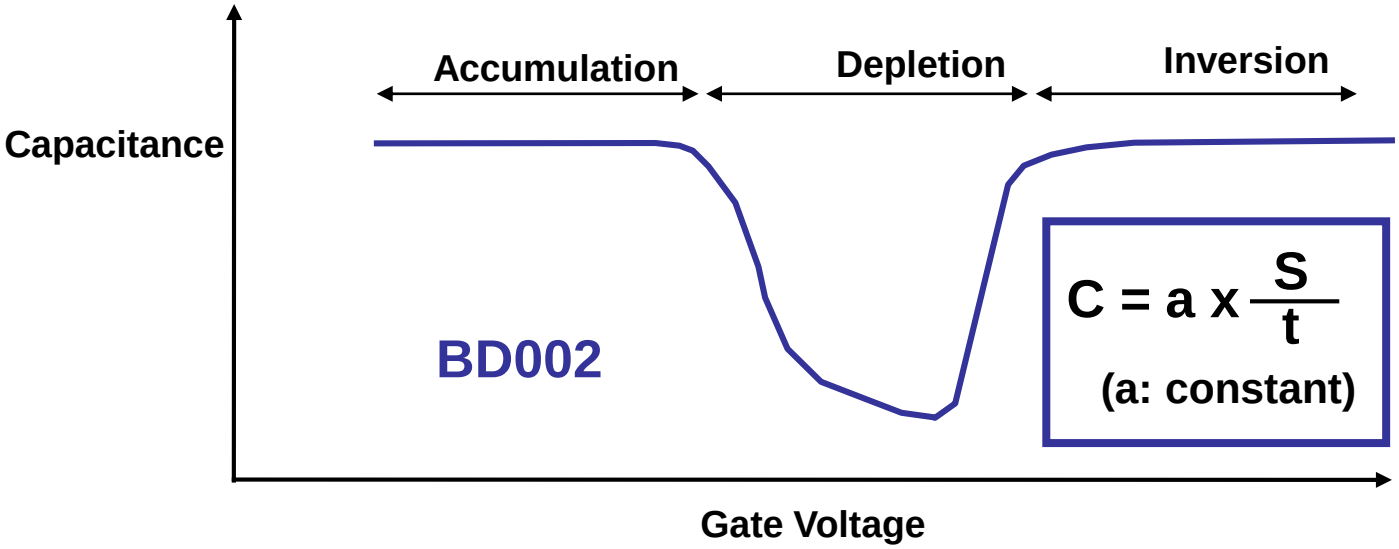


Semiconductor (substrate)

** actual metal or heavily doped polysilicon*

Behavior of MOS Capacitor





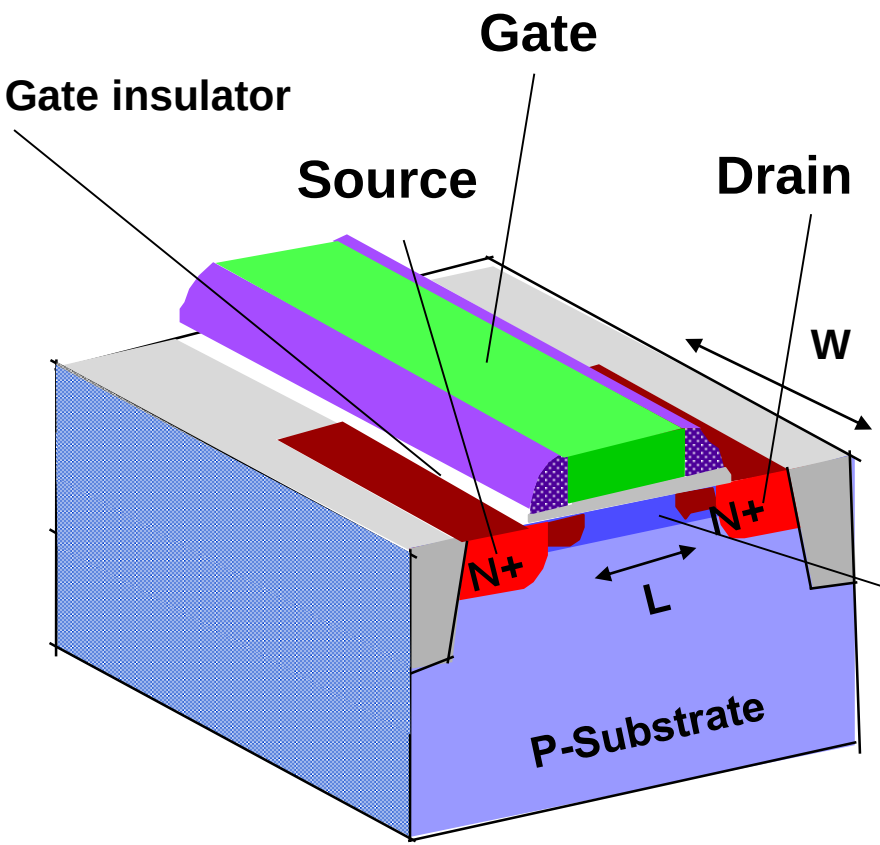
$$C = a \times \frac{S}{t}$$

(a: constant)

ex.
t …10nm
C….pico F

MOSFET

*** focusing on n-channel transistor ***



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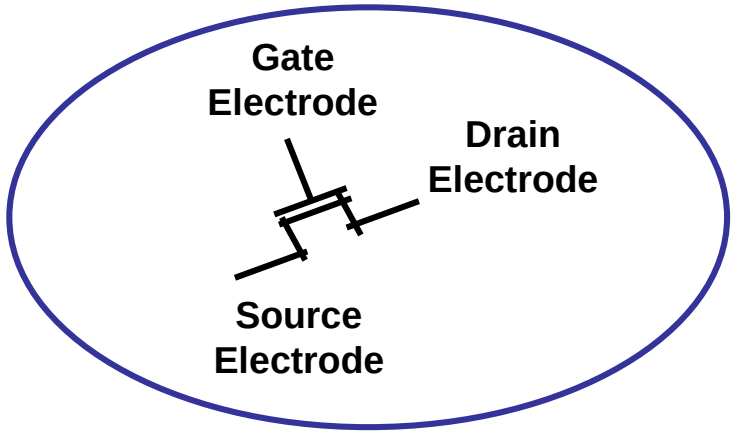


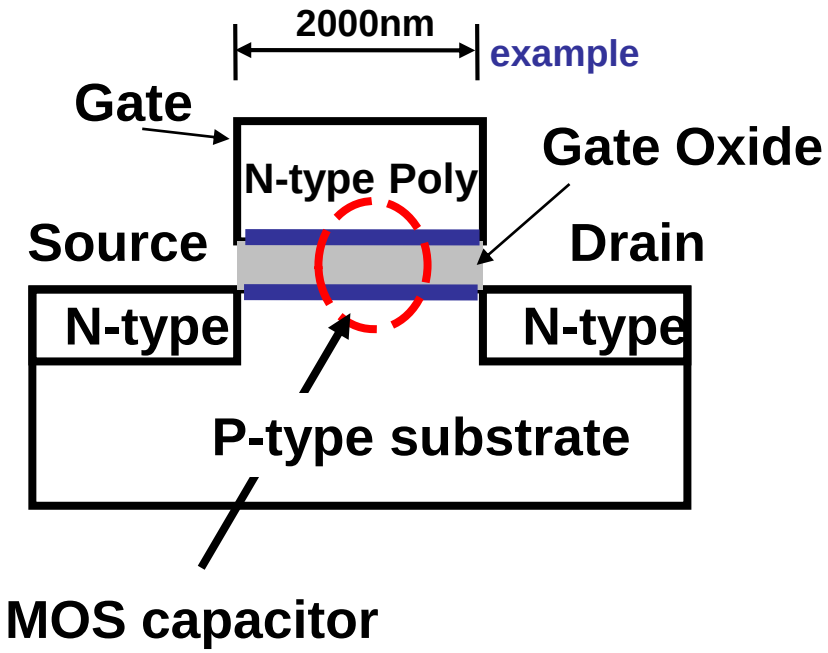
Channel

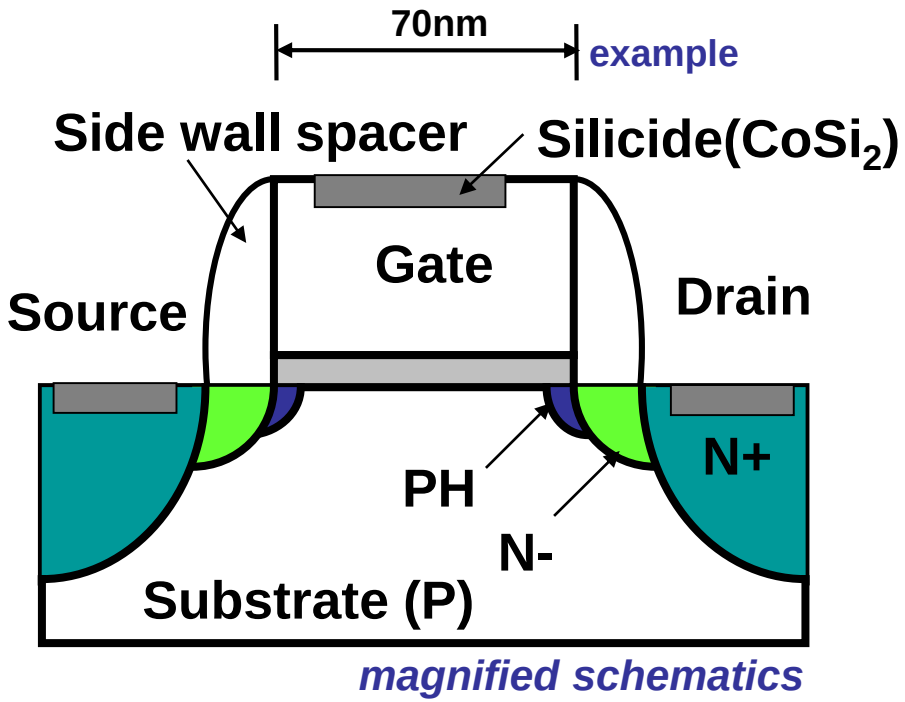
N+: heavily doped silicon
= low resistive electrode

L: Channel length
W: Channel width
FET: Field Effect Transistor

Basic MOSFET structure

By applying voltage to Gate, charges are induced at the capacitor edge. These charges are pulled out by Drain.





magnified schematics

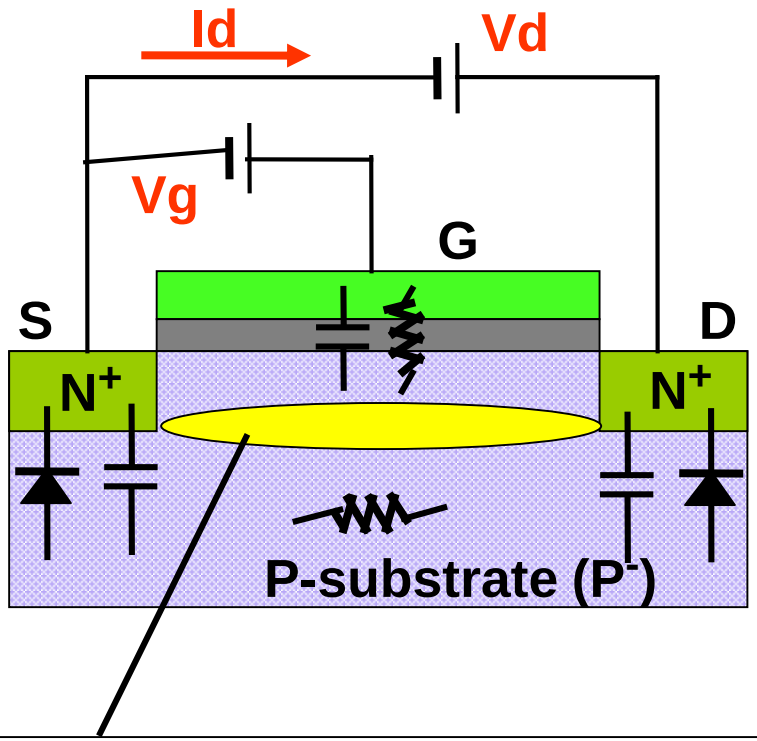
Basic structure

to be used in BF001 for simplicity

Advanced structure

to be explained in BD002

Channel and Parasitic Devices



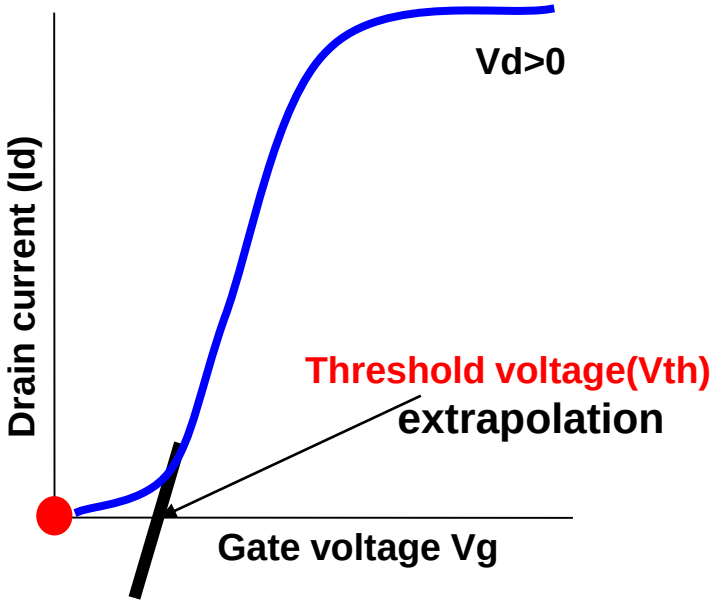
channel

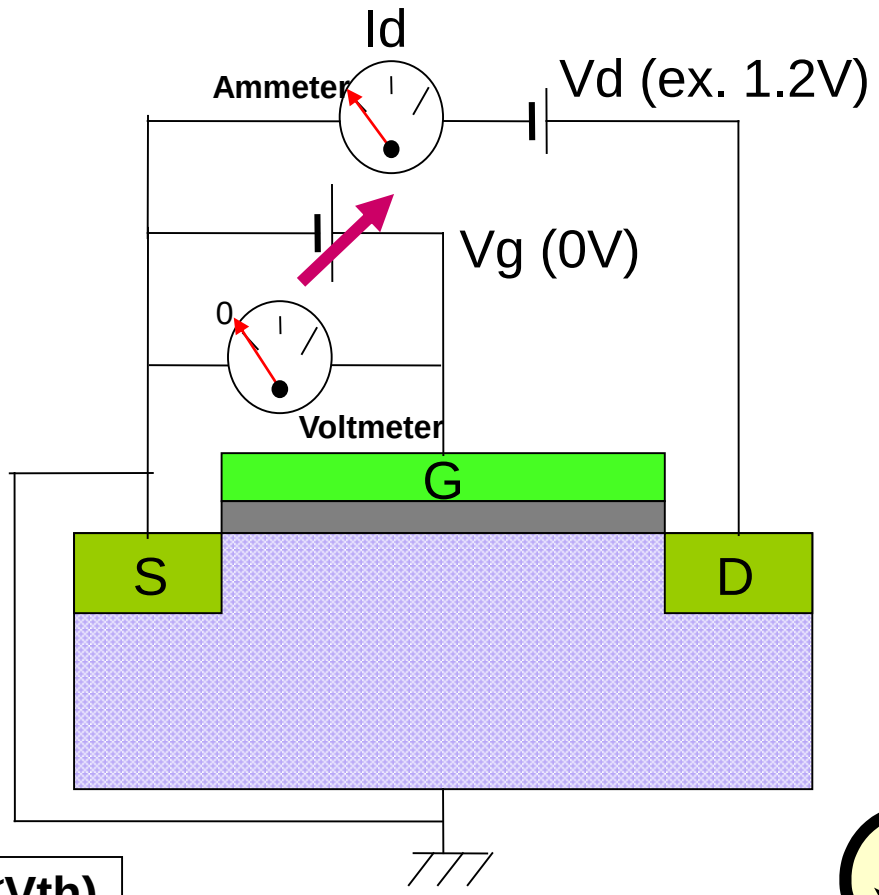
Id = f (Vd, Vg)

Gate characteristics: Id vs. Vg
Drain characteristics: Id vs. Vd

Operation of N-channel MOSFET (1)

- Gate characteristics



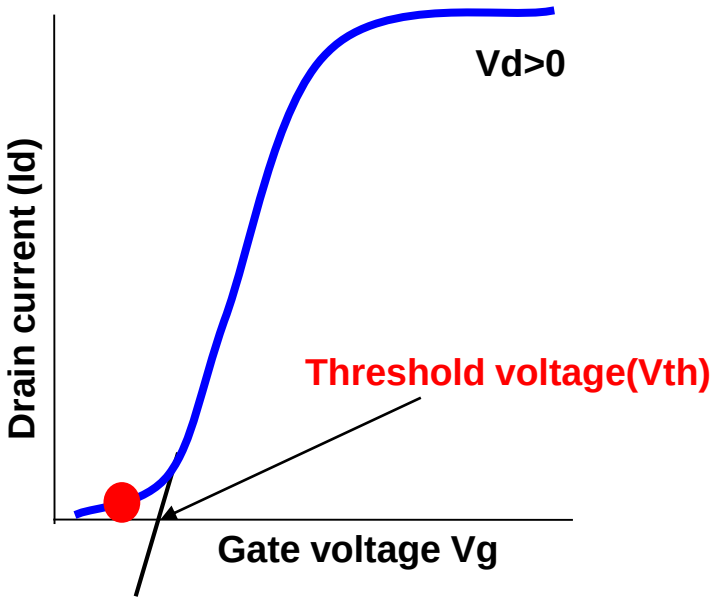


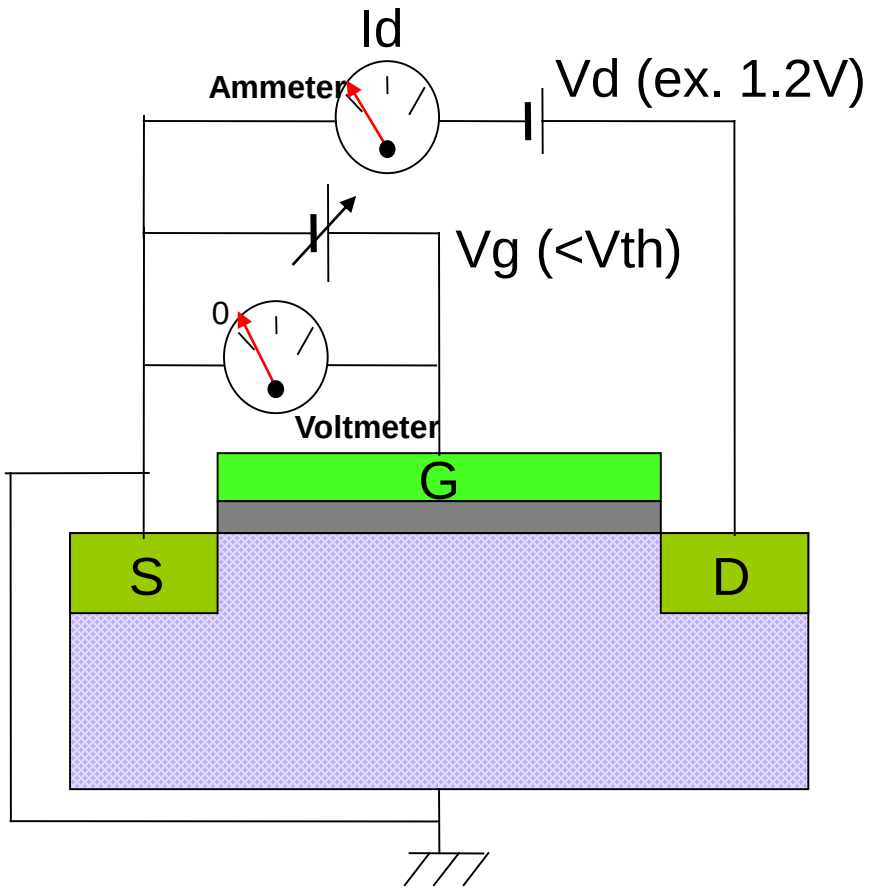
Sub-threshold region **(0≦Vg≦Vth)**

Id= 0 (nearly)

Operation of N-channel MOSFET (2)

- Gate characteristics

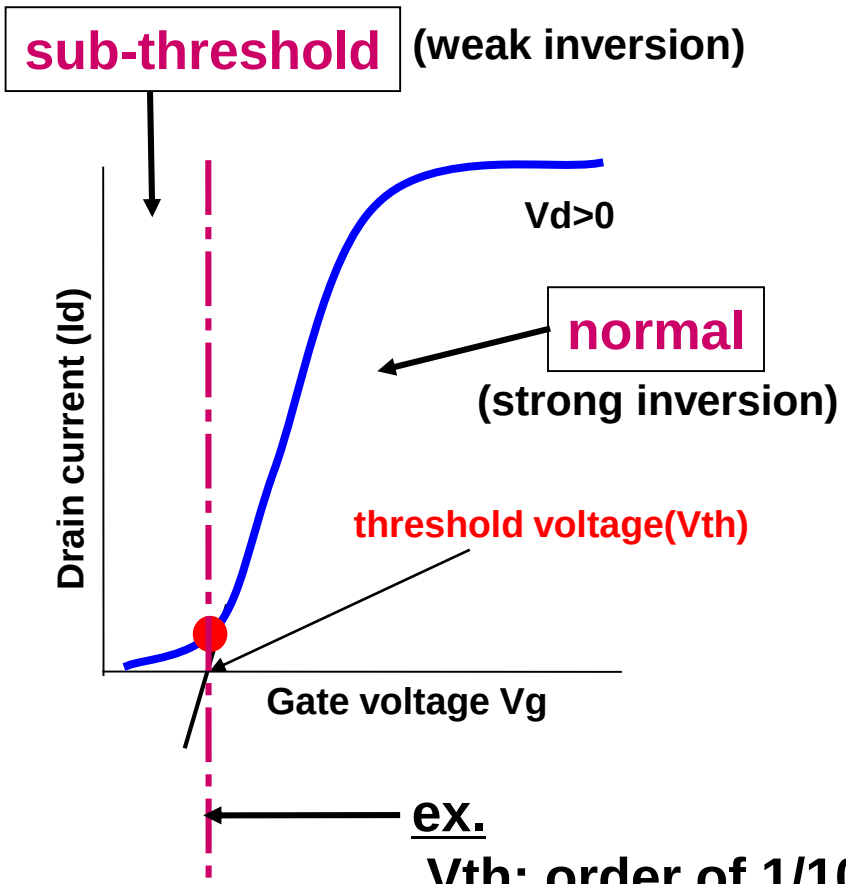




When Vg<Vth, the electric current is called sub-threshold current. This is one of the leakage currents.

Operation of N-channel MOSFET (3)

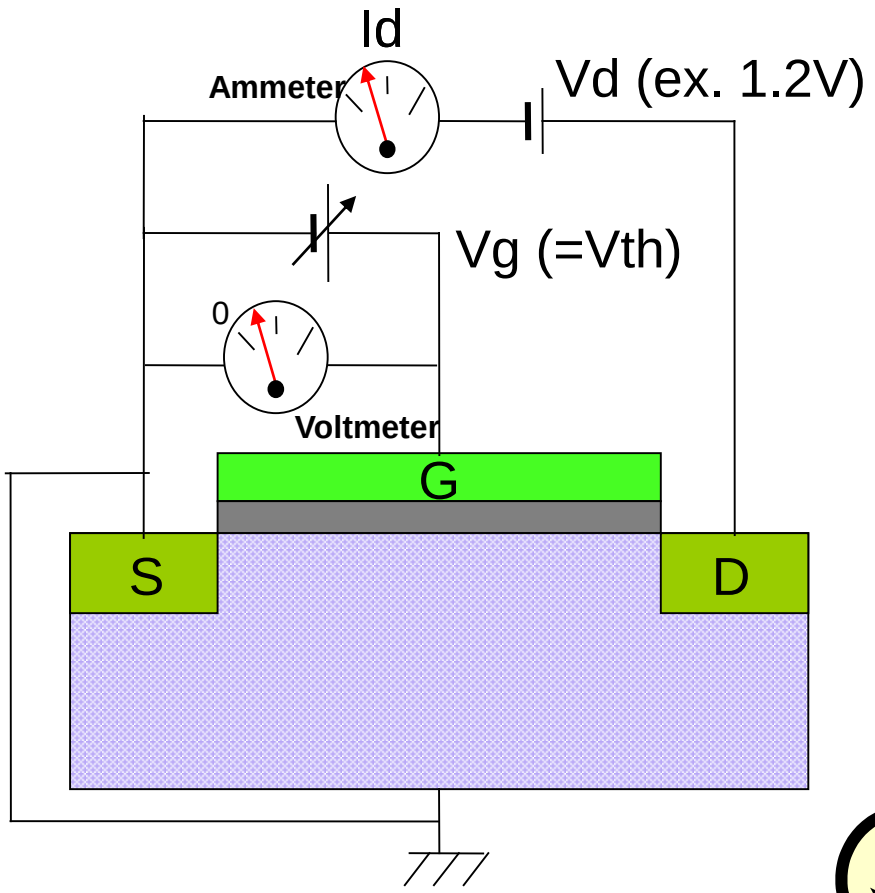
- Gate characteristics



ex.

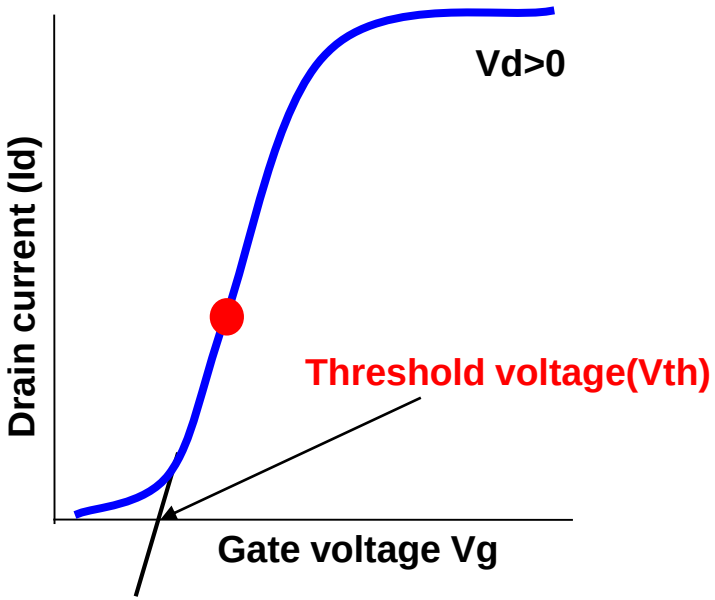
Vth: order of 1/10 V

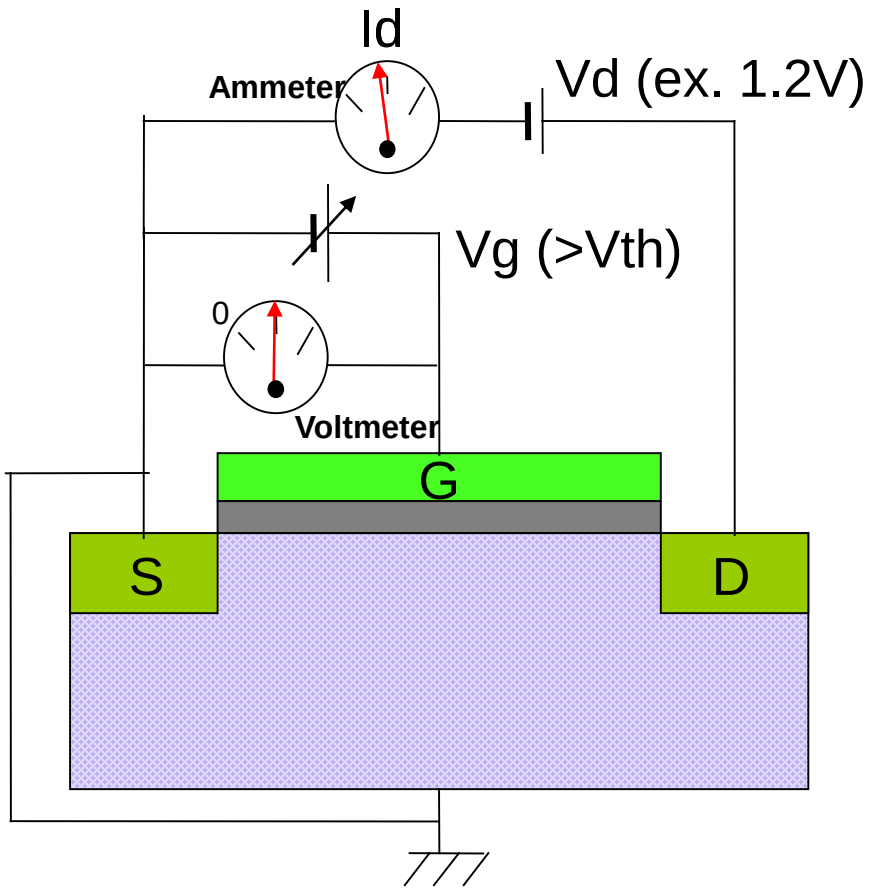
Id : order of nA



Operation of N-channel MOSFET (4)

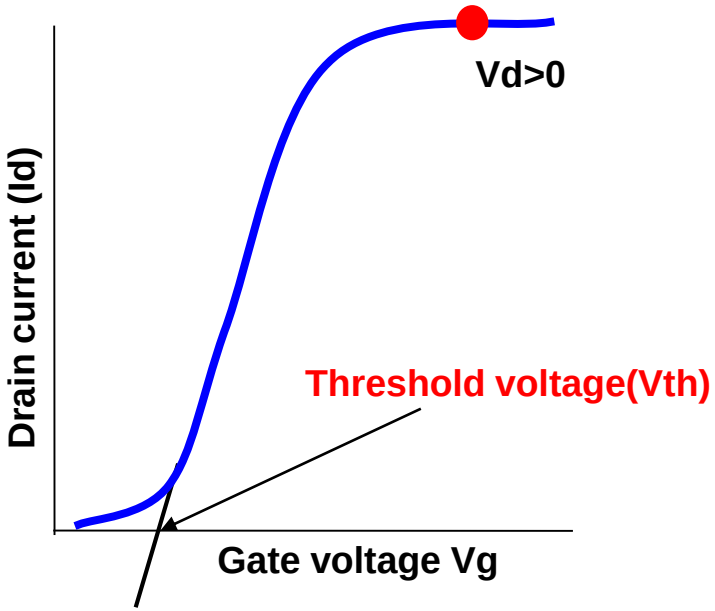
- Gate characteristics

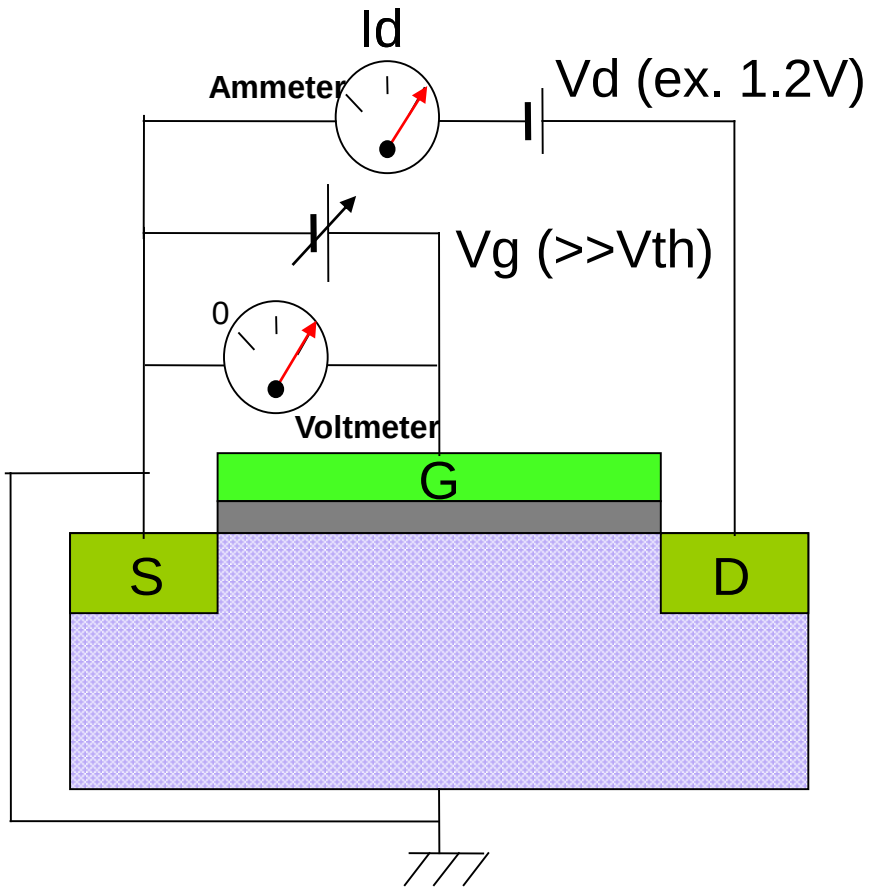




Operation of N-channel MOSFET (5)

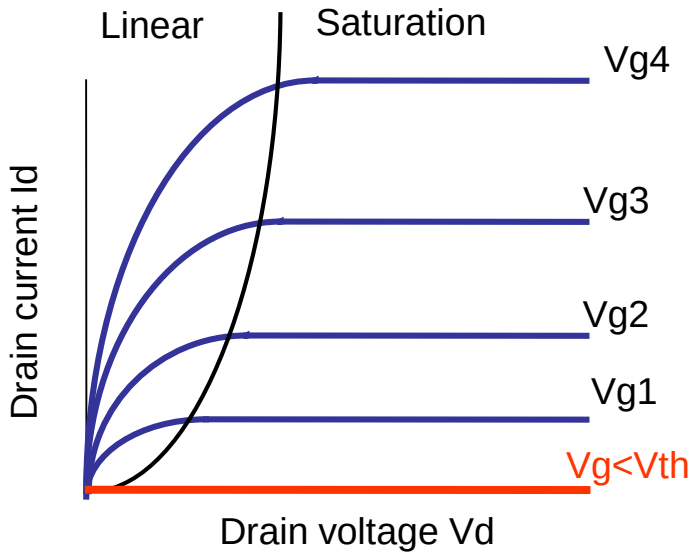
- Gate characteristics

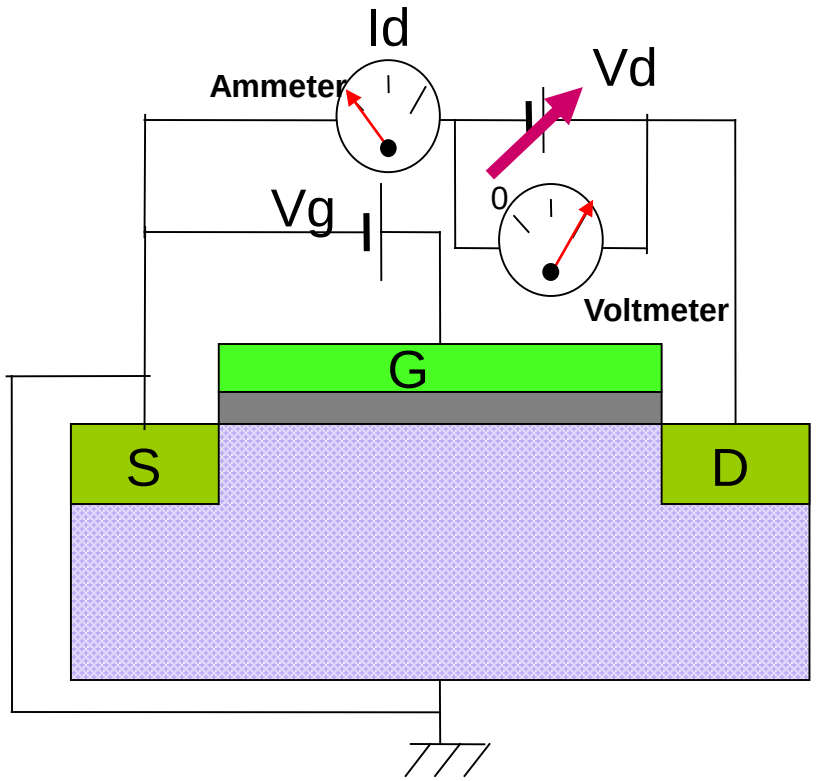




Operation of N-channel MOSFET (6)

- Drain characteristics

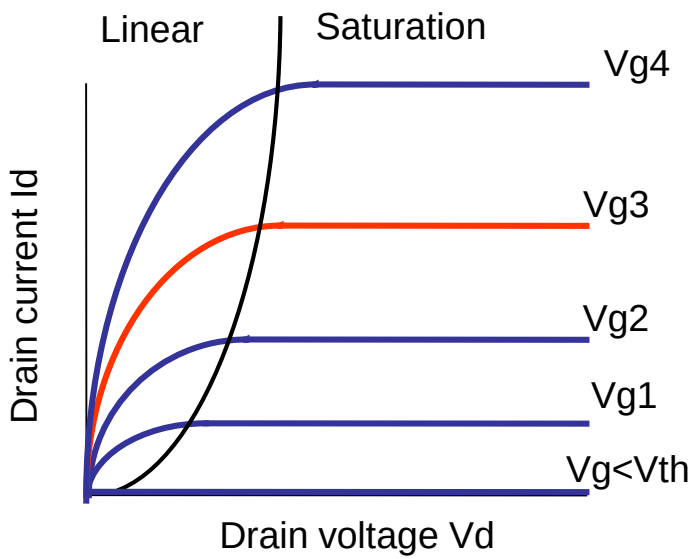


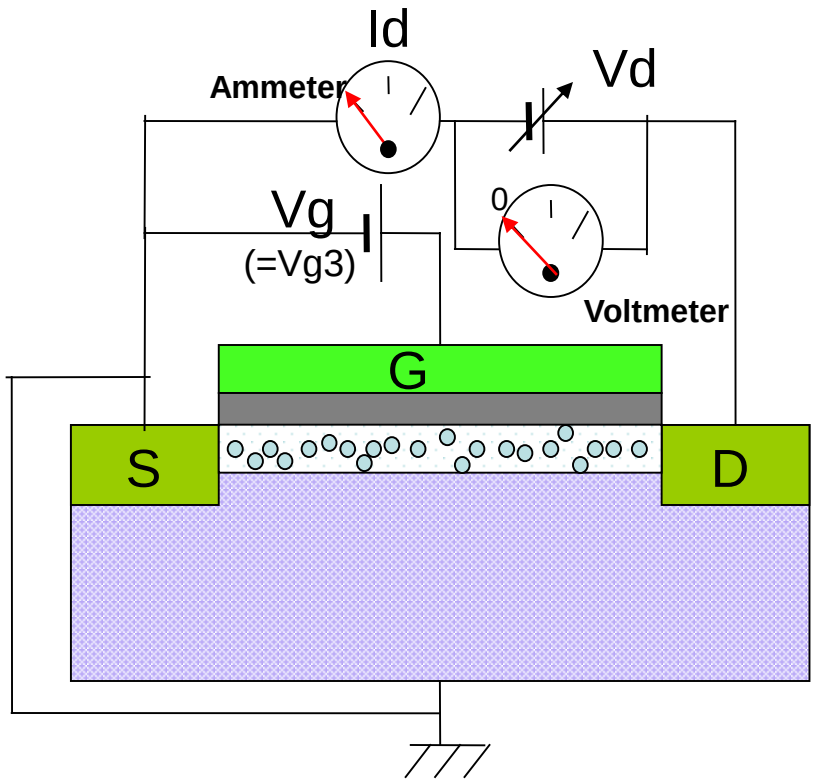


Even if Vd>0, there is no current (except leakage) when Vg<Vth.

Operation of N-channel MOSFET (7)

- Drain characteristics

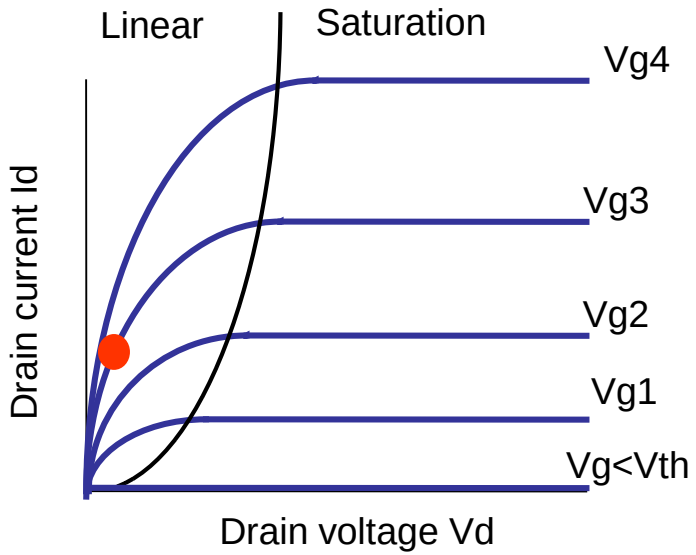


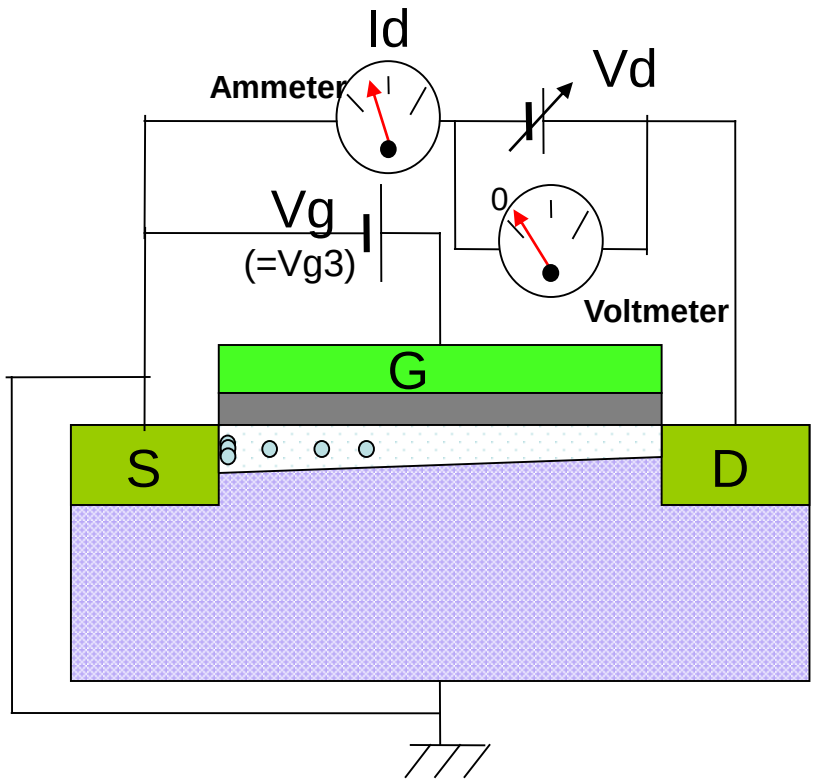


Apply Vg=Vg3, and watch what happens.

Operation of N-channel MOSFET (8)

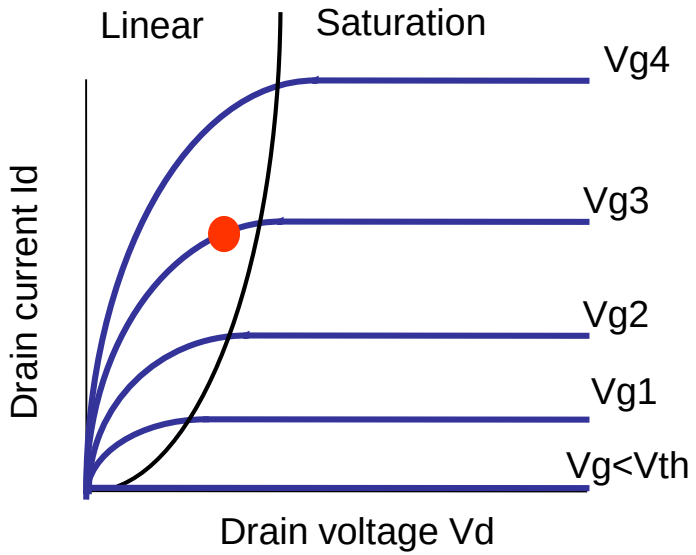
- Drain characteristics

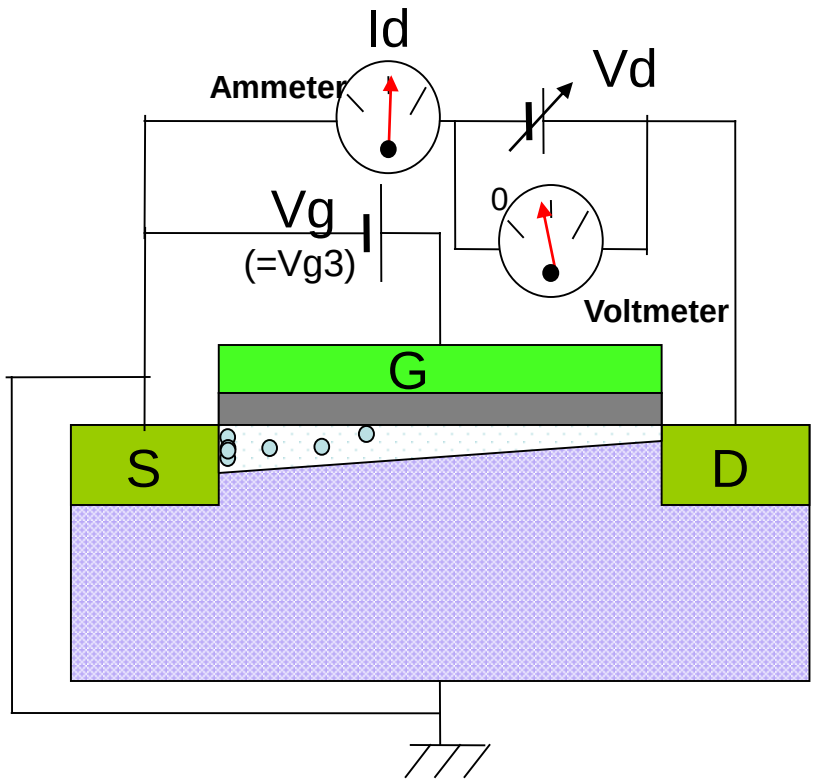




Operation of N-channel MOSFET (9)

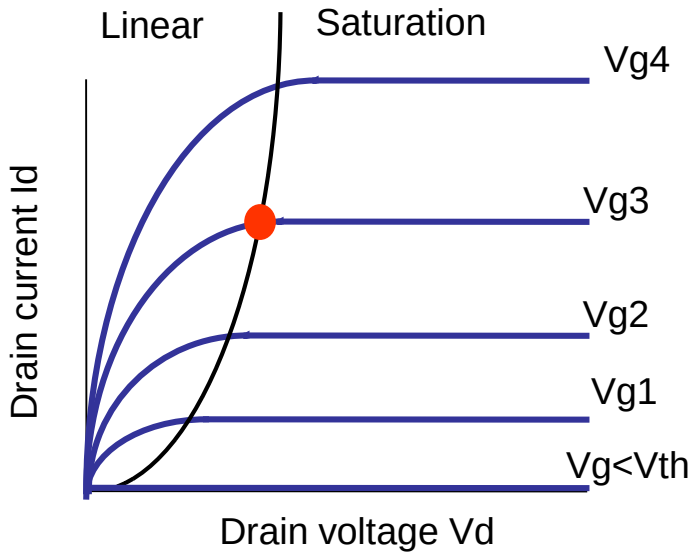
- Drain characteristics

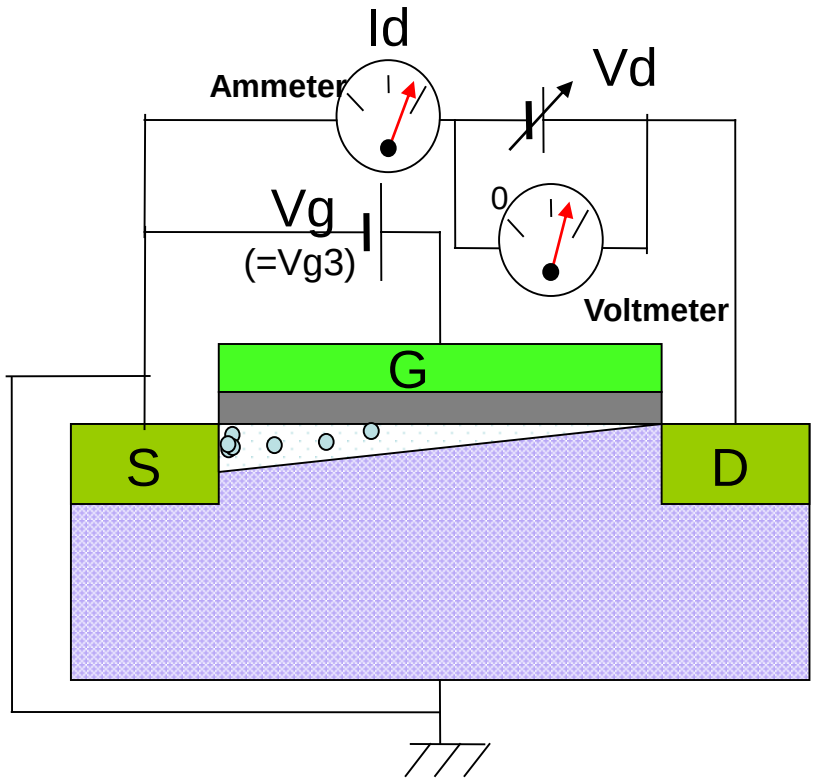




Operation of N-channel MOSFET (10)

- Drain characteristics



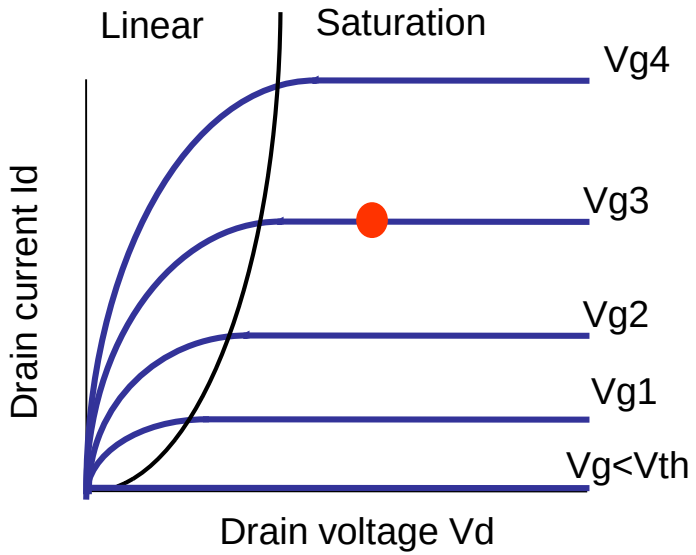


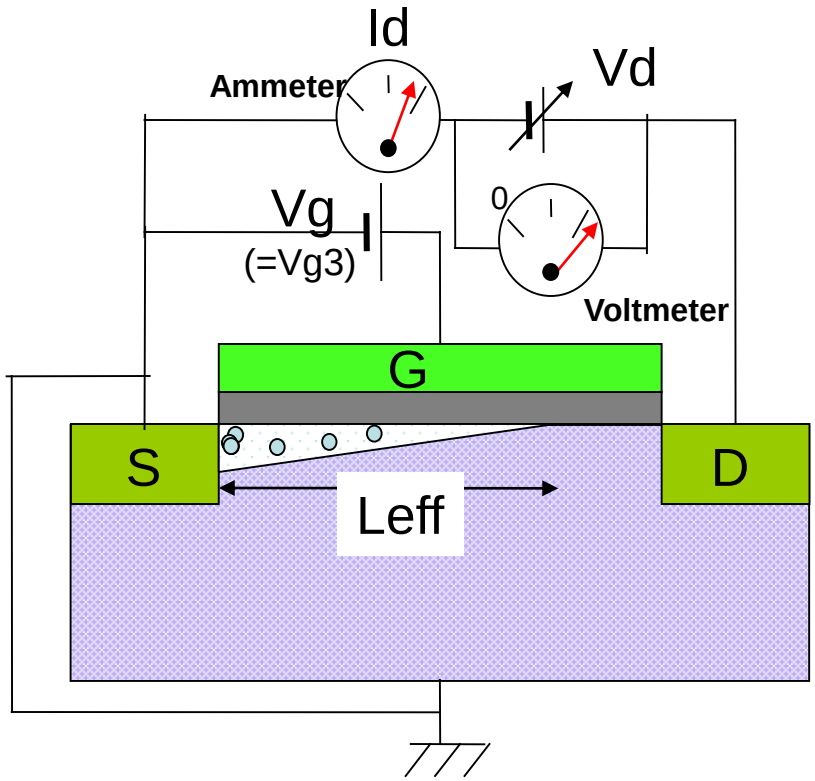
When Vd=Vg-Vth, it is called “pinch-off point”.
Vd=Vg-Vth is boundary of linear region & saturation region

BD002

Operation of N-channel MOSFET (11)

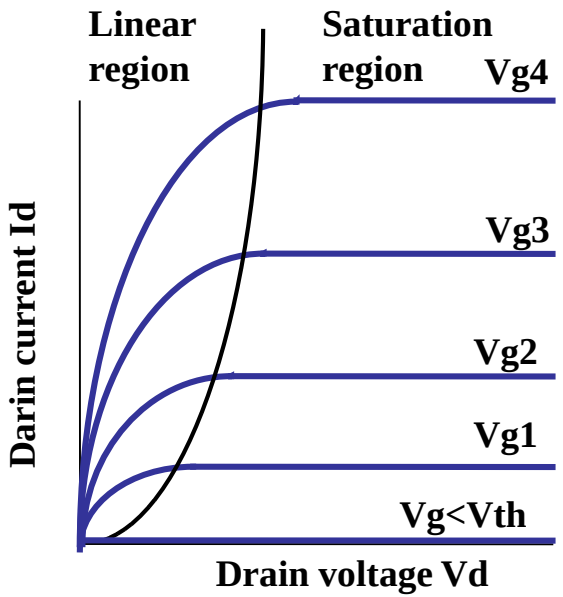
- Drain characteristics





After pinch-off, the current becomes constant.
Electrons are attracted by drain field and flow through the depletion region.

Current characteristics of MOSFET (Summary)



Id: Drain current
W:Channel width
L: Channel length
Vth: Threshold voltage
Cox: Gate capacitance
$= \varepsilon * \varepsilon_0 / Tox$
Vg: Gate voltage
μ : Mobility of carrier
ε: Relative permittivity
ε_0 : Permittivity of vacuum
Tox: Gate Oxide thickness

Linear region $(0 \leqq Vd \leqq Vg-Vth)$

$$Id = \mu Cox \frac{W}{L}\left\{(Vg-Vth)Vd - \frac{1}{2}Vd^2\right\}$$ (parabolic)

Saturation region $(Vd > Vg-Vth)$

$$Id = \frac{W}{2L}\mu\, Cox\, (Vg-Vth)^2$$

Short Quiz

1/ What are two regions in the Ids-Vds curves, and what are their boundaries ?

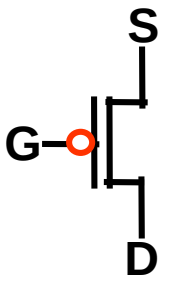
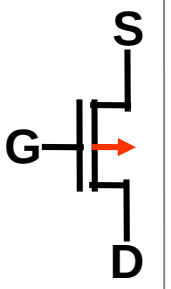
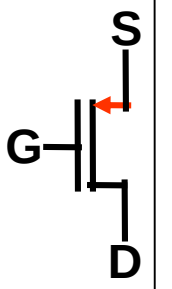
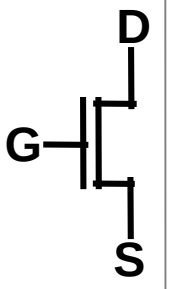
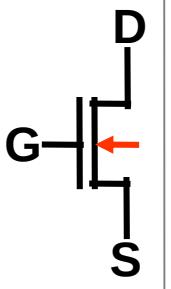
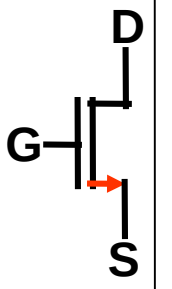
References

- Physics of Semiconductor Devices 2nd Edition by S.M.Sze,1981
- Fundamentals of MODERN VLSI DEVICES by Y.Taur and T.H.Ning,1998

Let's take a 15-minutes BREAK

3.2 MOS Operations

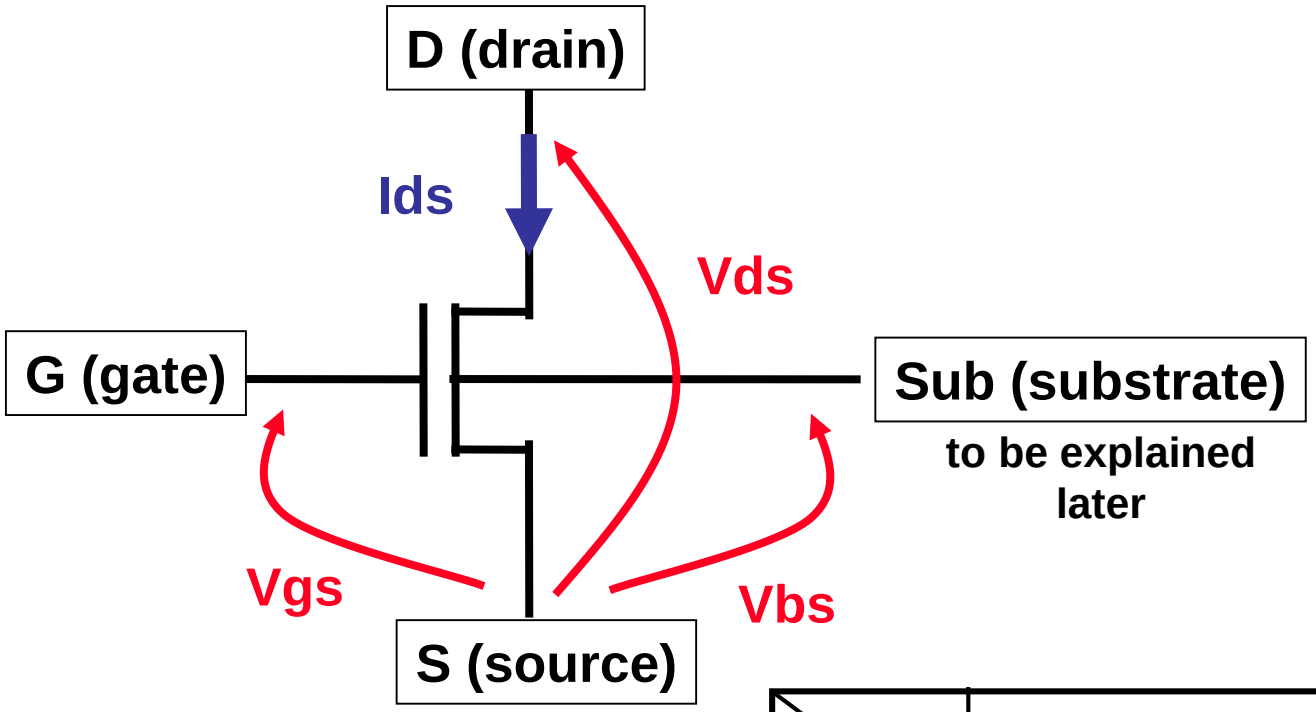
Notations and Operations of MOS Transistors

	Notations			Operations
pMOS transistor				**When electric potential of gate (G) decreases* from potential level of source (S), current flows from source (S) to drain (D).**
nMOS transistor				**When electric potential of gate (G) exceeds* that of potential level of source (S), current flows from drain (D) to source (S).**

All three notations are commonly used.

* Accurately, threshold voltages must be considered as biases.

Naming Convention



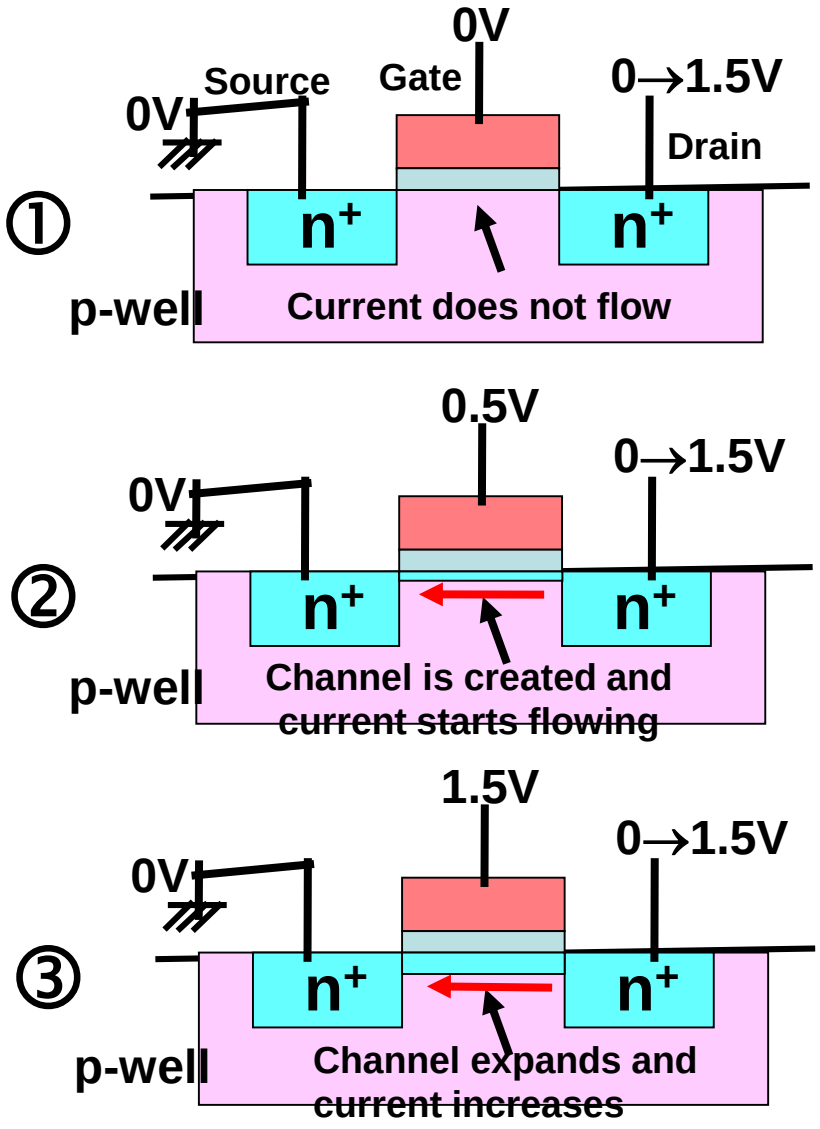
	Sign (polarity)			
	Vgs	Vds	Ids	Vbs
nMOS	+	+	+	-
pMOS	-	-	-	+

Sometimes “s” is eliminated, such as Vg, Vd, Id, and Vb.

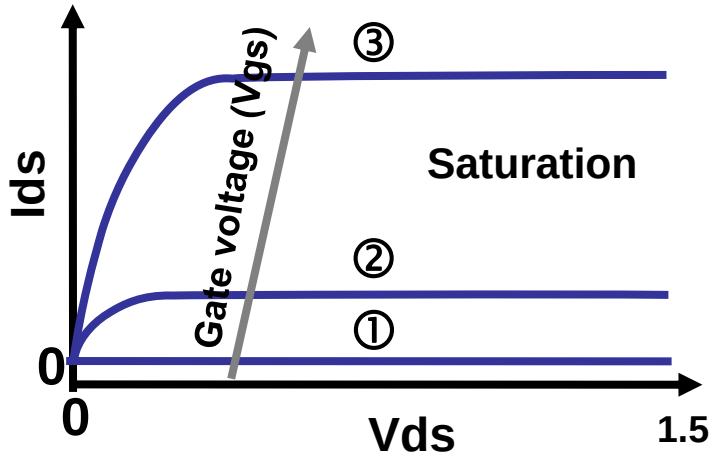
3.2 MOS Operations

- nMOS Operation
- pMOS Operation
- CMOS Structure

Operations of nMOS Transistor



<Characteristics of drain current >



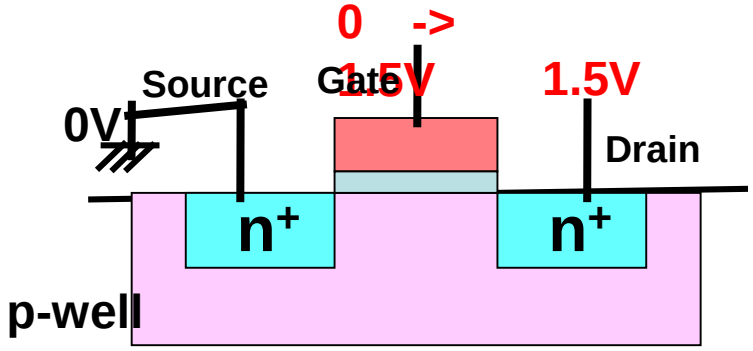
<Formula of drain current>

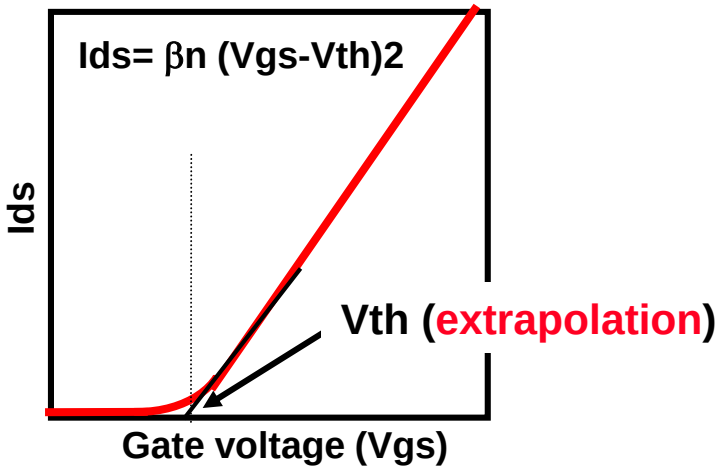
$$Ids = \begin{cases} \beta n\{2Vds\cdot(Vgs-Vthn)-Vds^2\} \\ \quad (\text{when } 0 \leqq Vds \leqq Vgs-Vthn) \\ \beta n(Vgs-Vthn)^2 \\ \quad (\text{when } Vds > Vgs-Vthn) \end{cases}$$

βn : proportionality coefficient
Vthn : threshold voltage (gate voltage required to switch ON transistor)

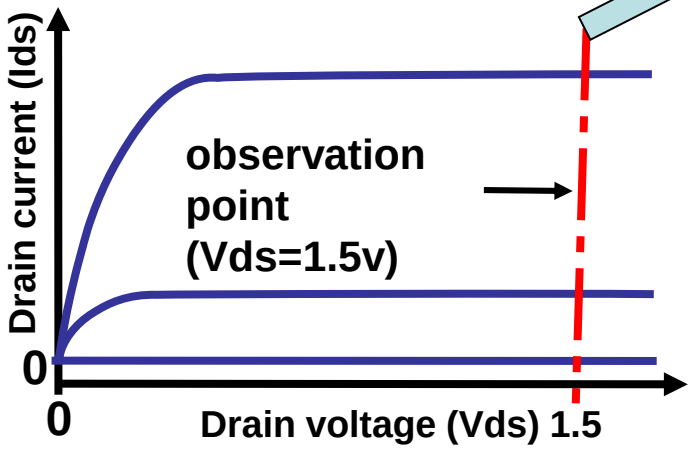
Relationship between threshold voltage and drain current (1)

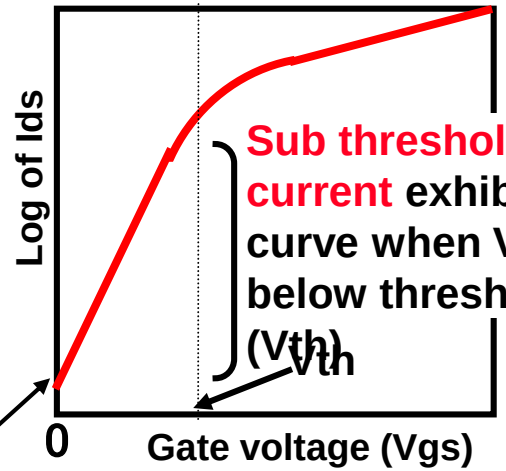
- Changing gate voltage with holding drain voltage constant





<Characteristics of drain current>





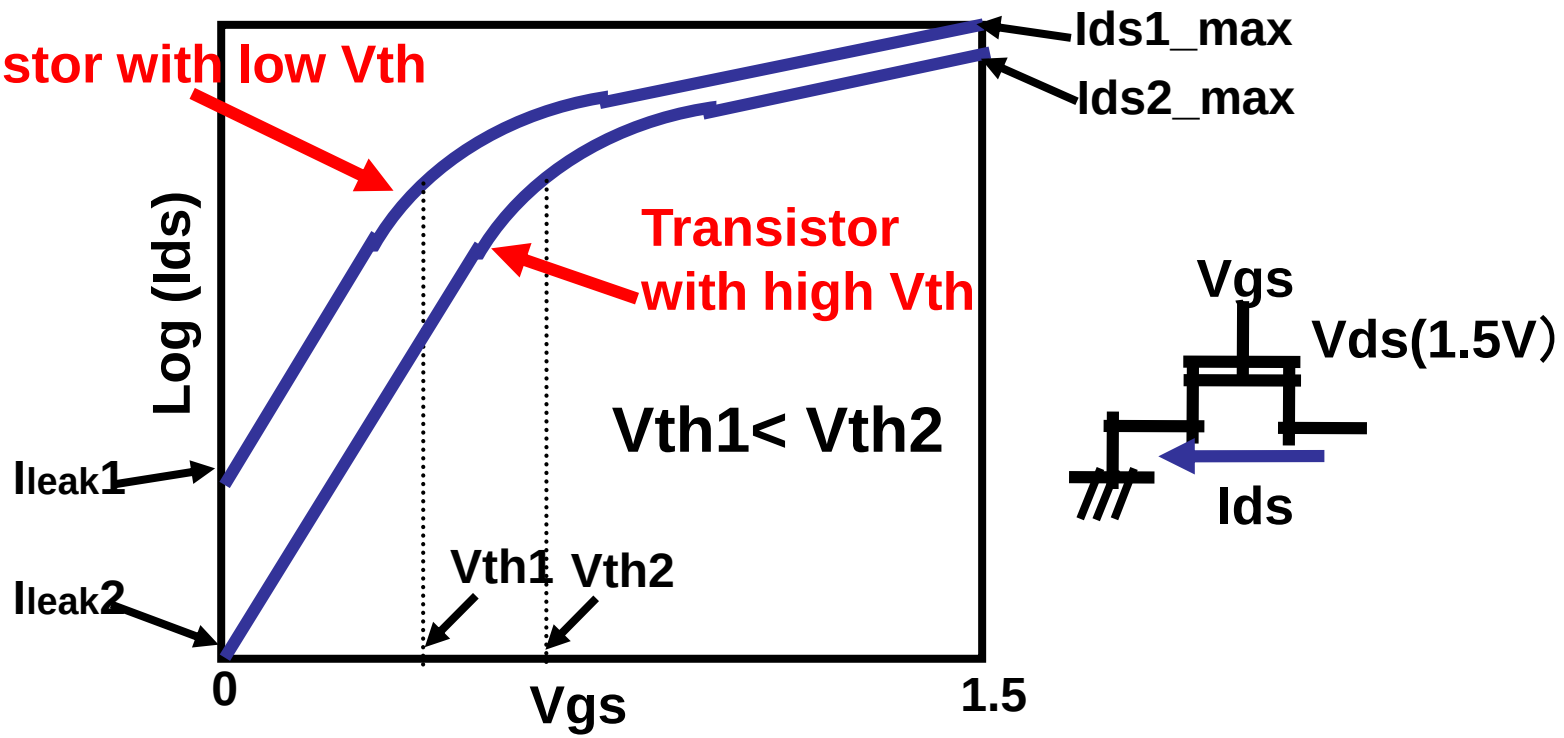
S (mV/dec)

OFF state leakage current

When Vthn varies, 'OFF state leakage current' also changes exponentially

Relationship between threshold voltage and drain current (2)

< Different transistor characteristics according to different Vth>

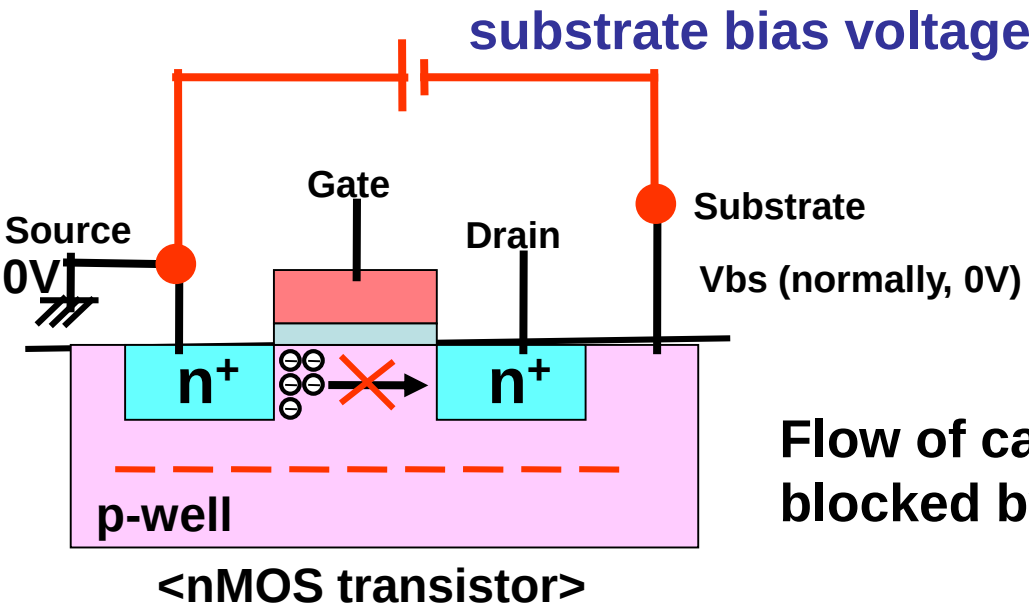


- Vth can be tuned during fabrication by ion implantation.
- Transistor with lower Vth is ….?

Vth, Important Parameter

Vth is determined by impurity concentration below gate oxide.
➔LSI designers cannot change its value?

Yes, we can!

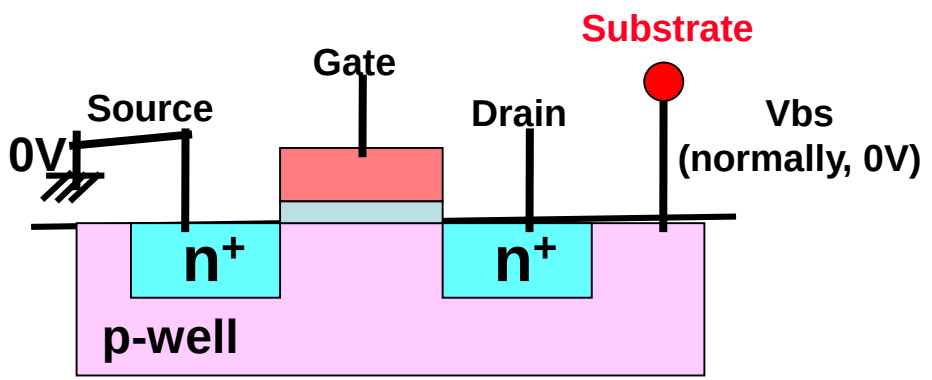


<nMOS transistor>

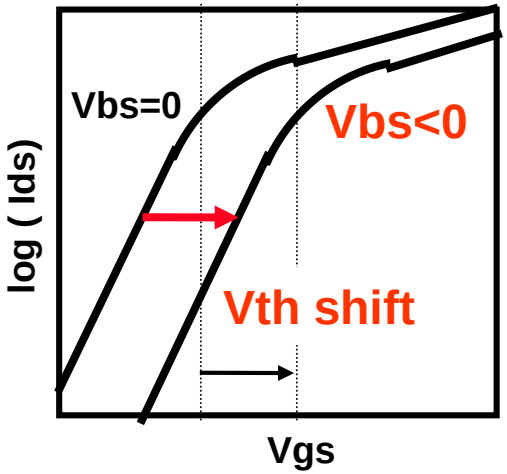
Flow of carriers (electron) is blocked by negative voltage.

Substrate Node Potential

○Electrical potential of substrate (formed by WELL structure) as 4th electrode also affects transistor characteristics.



<nMOS transistor>



< threshold voltage dependency on substrate voltage >

$$Vth = Vt0 + k(\sqrt{-Vbs + 2\phi} - \sqrt{2\phi})$$

Vt0, k, ϕ: constants

BD002

Body Effect

<nMOS>
* Vbs <<0, then …?
* speed, leakage…?

<pMOS>
* Vbs >>0, then …?
* speed, leakage…?

Short Quiz

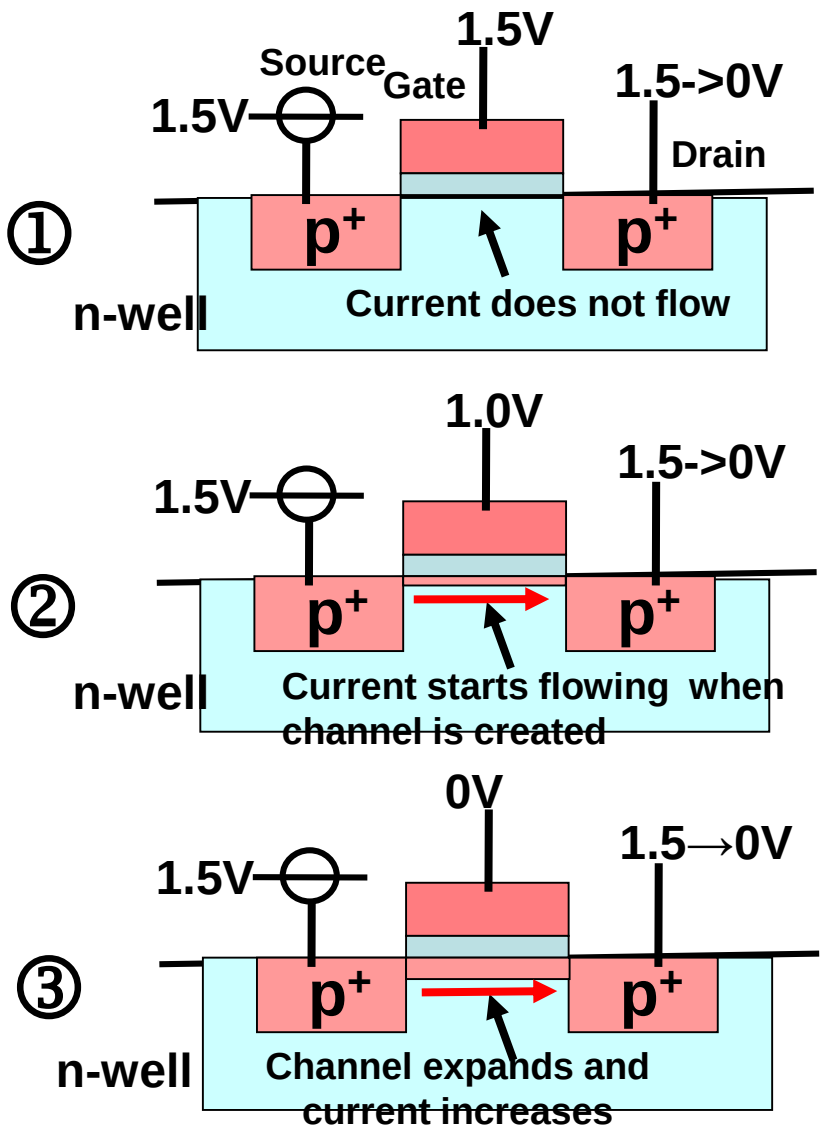
<nMOS>

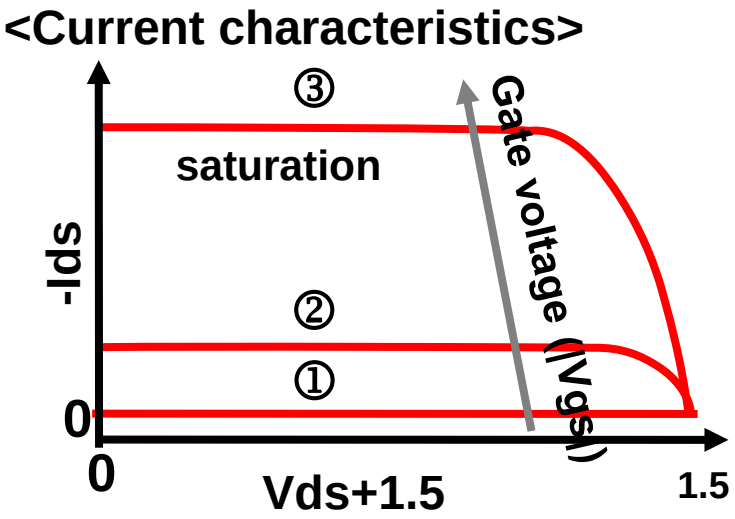
* Vbs <<0, then …?
* speed, leakage…?

3.2 MOS Circuit Fundamentals

- nMOS Operation
- pMOS Operation
- CMOS Structure

Operations of pMOS Transistor





<Formula of current>

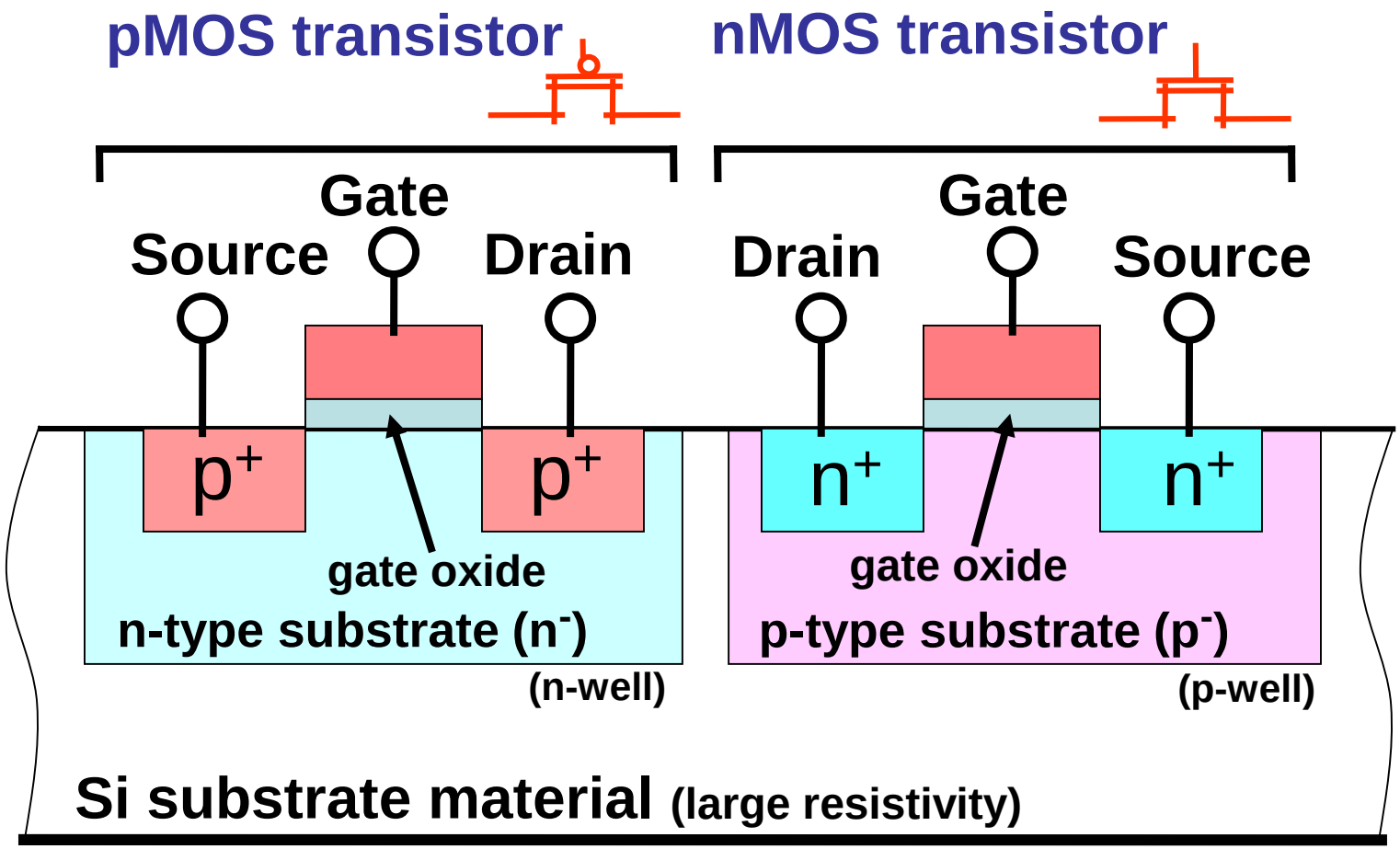
$$Ids = \begin{cases} -\beta\rho\{2Vds\cdot(Vgs-Vthp)-Vds^2\} \\ \quad (\text{when } Vgs-Vthp \leqq Vds \leqq 0) \\ -\beta\rho(Vgs-Vthp)^2 \\ \quad (\text{when } Vds<Vgs-Vthp) \end{cases}$$

βρ : **proportionality coefficient**
Vthp: threshold voltage (gate voltage required to switch ON transistor)

3.2 MOS Circuit Fundamentals

- nMOS Operation
- pMOS Operation
- CMOS Structure

Structure of CMOS Transistor



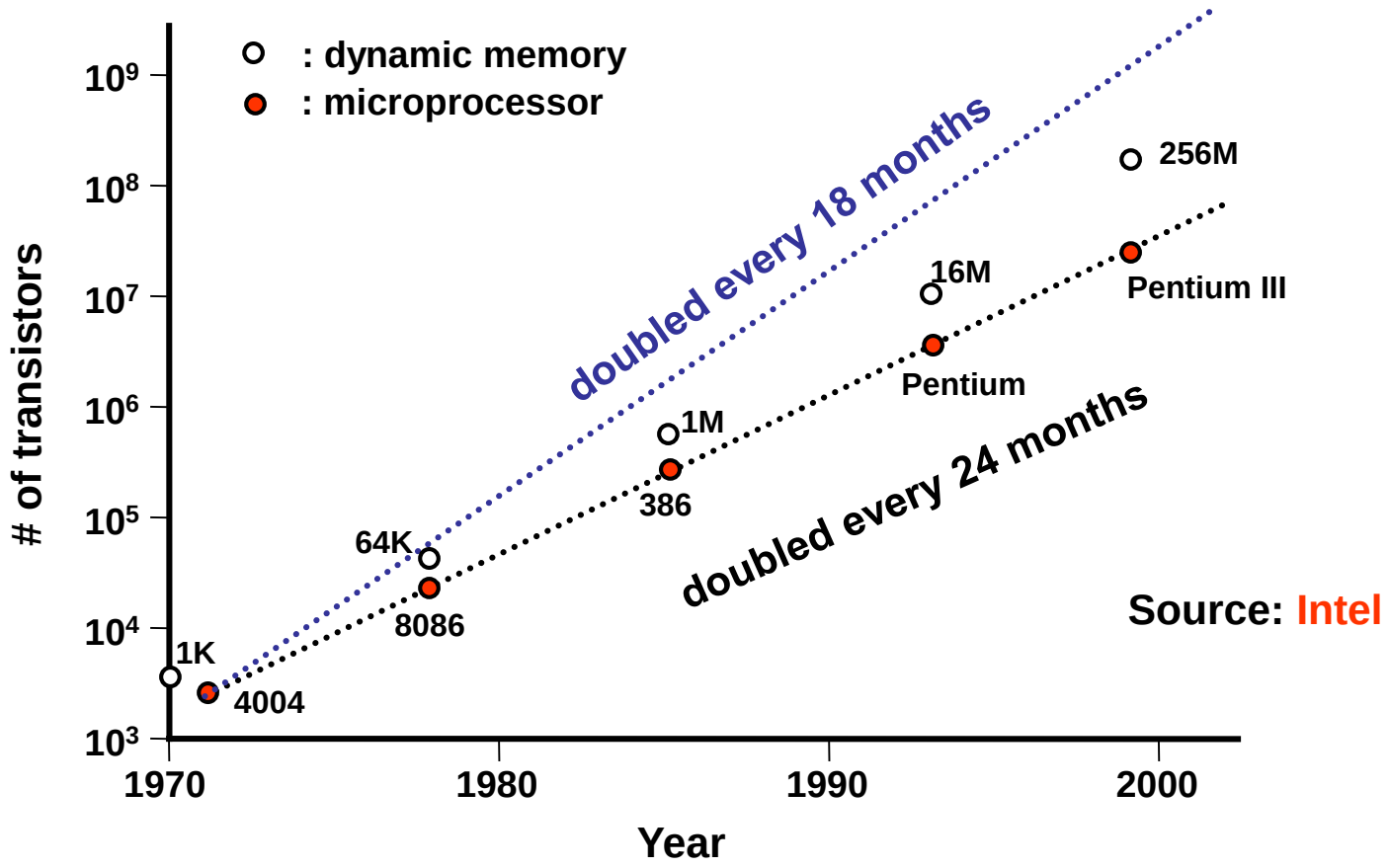
MOS: Metal-Oxide Semiconductor
CMOS: Complementally MOS

3.3 Scaling

- Moore’s Law
- Scaling Rule

Moore's Law

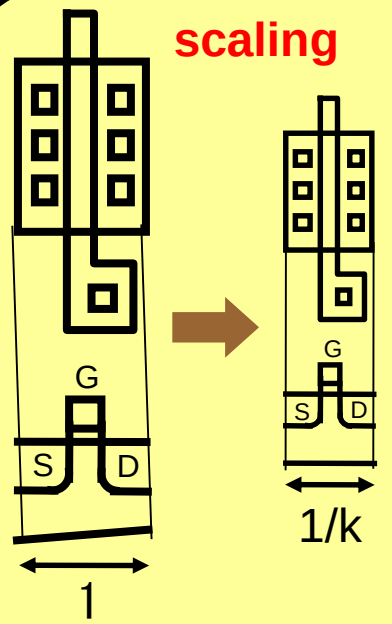
Gordon Moore predicted that the number of transistors that could be inexpensively placed on an IC chip would be doubled every 1.5-2 years.



Scaling Rule

k: scaling factor

	To keep voltage constant (Old)	To keep electric field Constant (Now)
One side of length (X)	1/k	1/k
Gate oxide thickness (tox)	1/k	1/k
Power supply voltage (V)	1	1/k
Electric field strength (E)	k	1
Electric current (I)	k	1/k
Capacity (C)	1/k	1/k
Delay time (Td)	$1/k^2$	1/k
Power consumption (P)	k	$1/k^2$
Power density (P/X^2)	k^3	1



$I \propto V^2/ tox$

$Td \propto CV/ I$

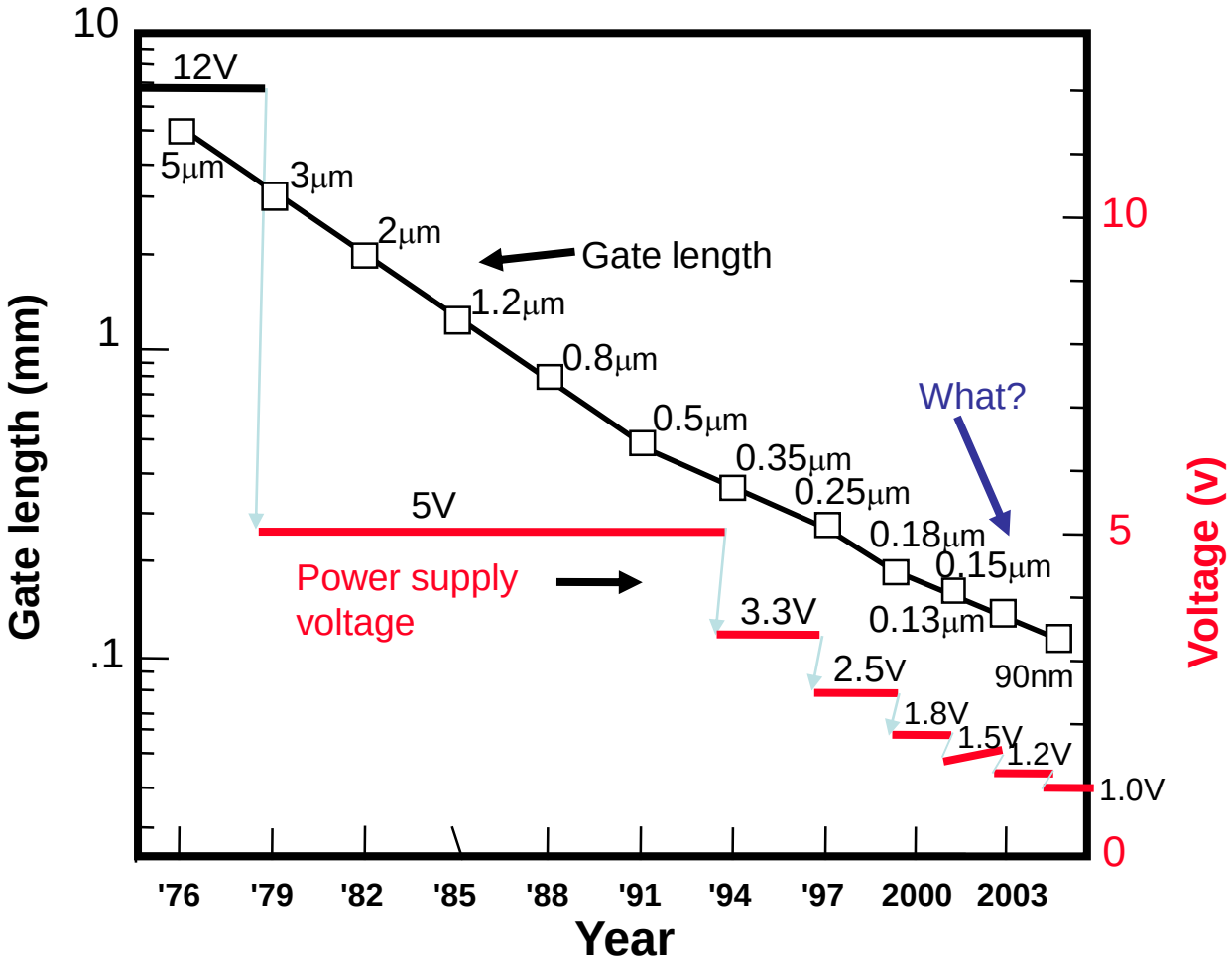
$P \propto fCV^2=CV^2/ Td$

◆The effects of scaling are prominent in establishing high speed, low power consumption, and high density.

◆Till now, these effects have been realized by continuously developed process generations.

Success history of semiconductor development !! However…

Trend of Power Supply Voltage vs. Scaling



After 0.35 μm generation, power supply voltage has been reduced to maintain electric field constant in gate oxide.

Limitation on Scaling Rule

1. Some items are not fully scaled

L: 1.0um -> 0.06um (1/17)
Tox: 20nm -> 1.5nm (1/13)
Vdd: 5V -> 1.2V (1/4)

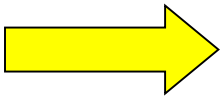
2. Driveability

I: 1/k
I/W: 1

3. Unscalable factors

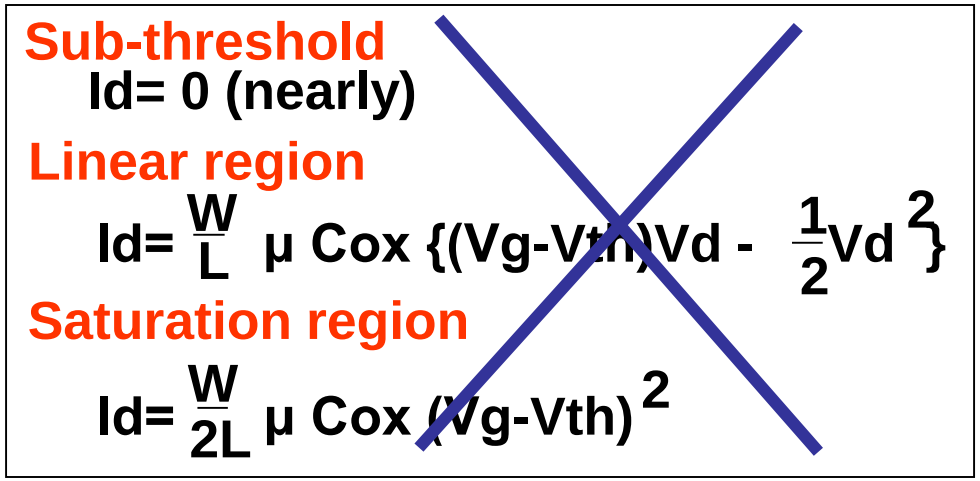
Vth
(S factor)
(Surface potential….)

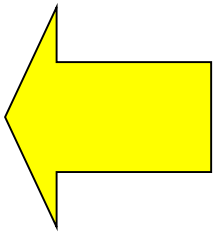
BD002



Short Channel Effect becomes glaring

Short Channel Effect





"L" becomes shorter

BD002

1. Increase in off state leakage current

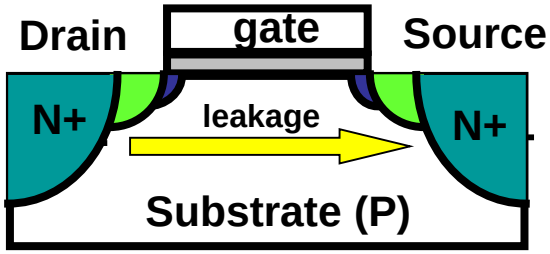
- Vth decrease (roll off)
- S factor increase (slack of Ids-Vgs curve)
- Vth is varied by drain voltage (Vth decrease)

2. Ids does not increase in proportion to 1/L

How to prevent?

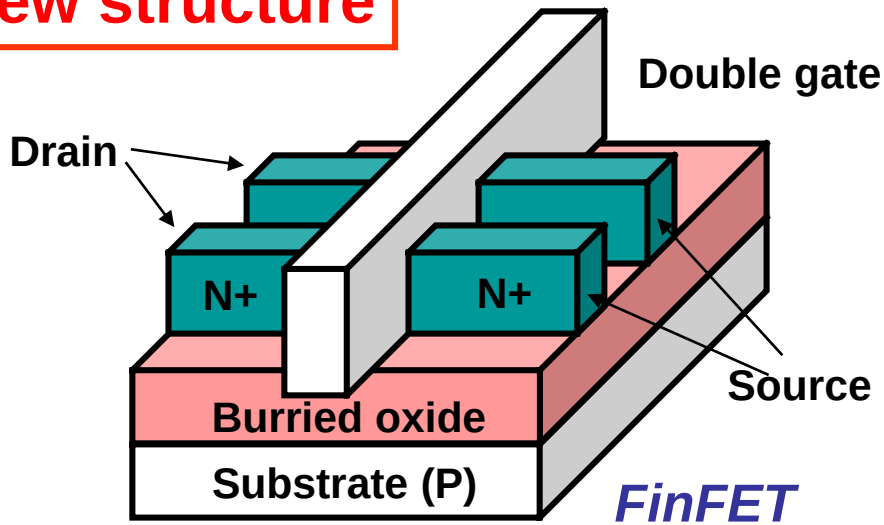
Non-classical CMOS

<More Moore>



bulk MOSFET

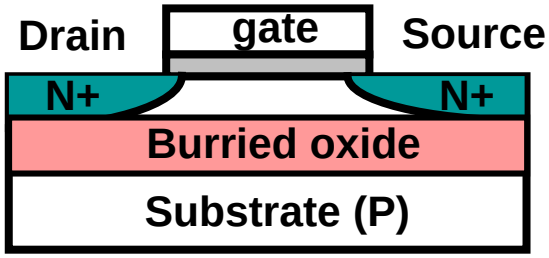
New structure



FinFET

New material

- high-k metal gate (HKMG)
- strained silicon
- 110 wafer (surface orientation)



SOI MOSFET

SOI (Silicon On Insulator)

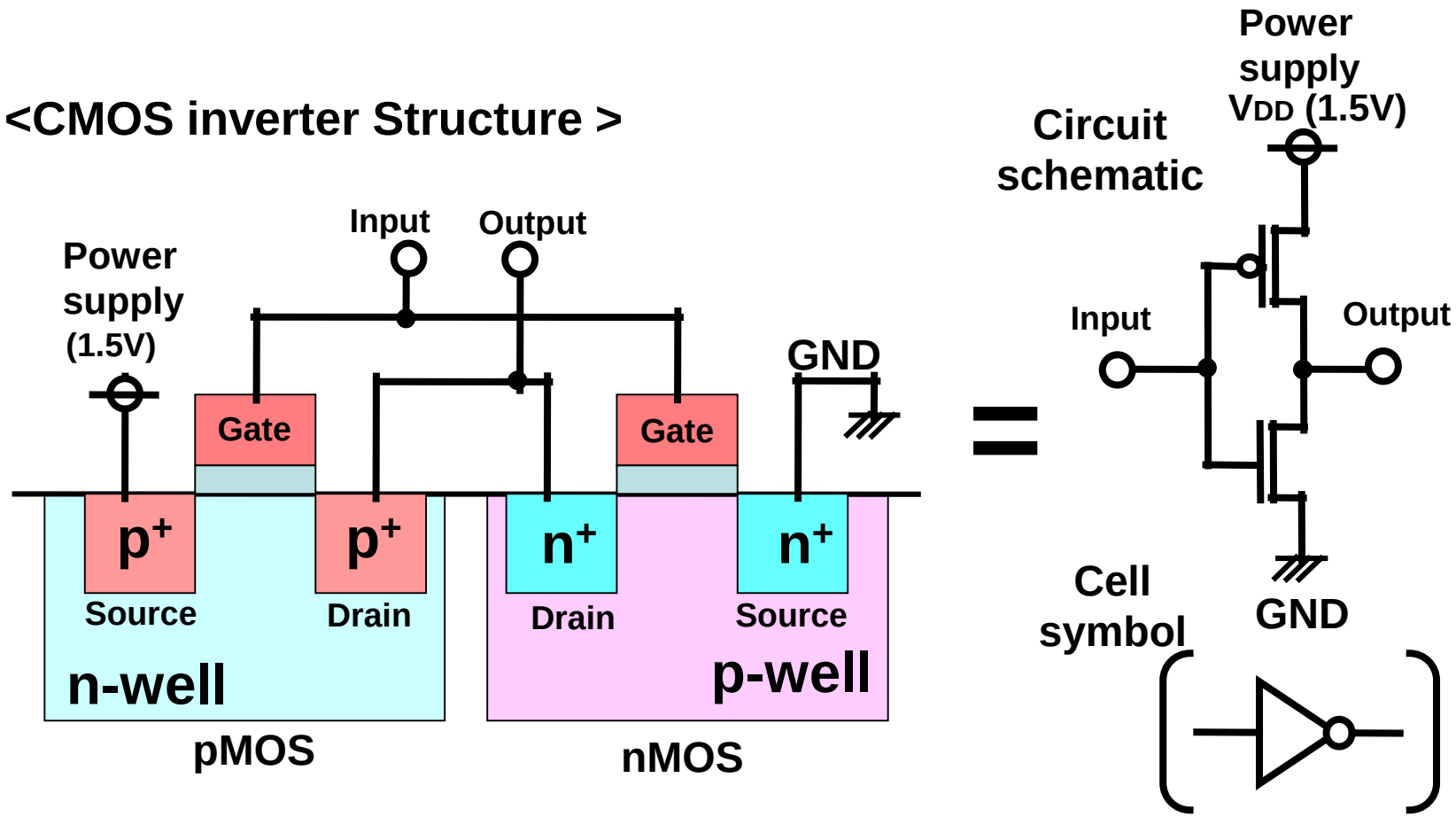
Summary of MOS Transistor

- Characteristics of nMOS and pMOS transistors are symmetrical, and polarity of signals is opposite.
- Ids/Vds curves are divided into linear and saturation regions, where their boundary is Vds= Vgs-Vth.
- Ids/Vgs curve is divided into normal and sub threshold regions, where boundary is Vgs= Vth.
- Vth determines max Ids and leakage current: faster but leakier.
- Substrate node acts as 4^{th} terminal, and affects Vth.
- Scaling has been success story of semiconductor with reduction of power supply voltage.
- But now, more Moore.

3.4 Basic CMOS Logic Circuits

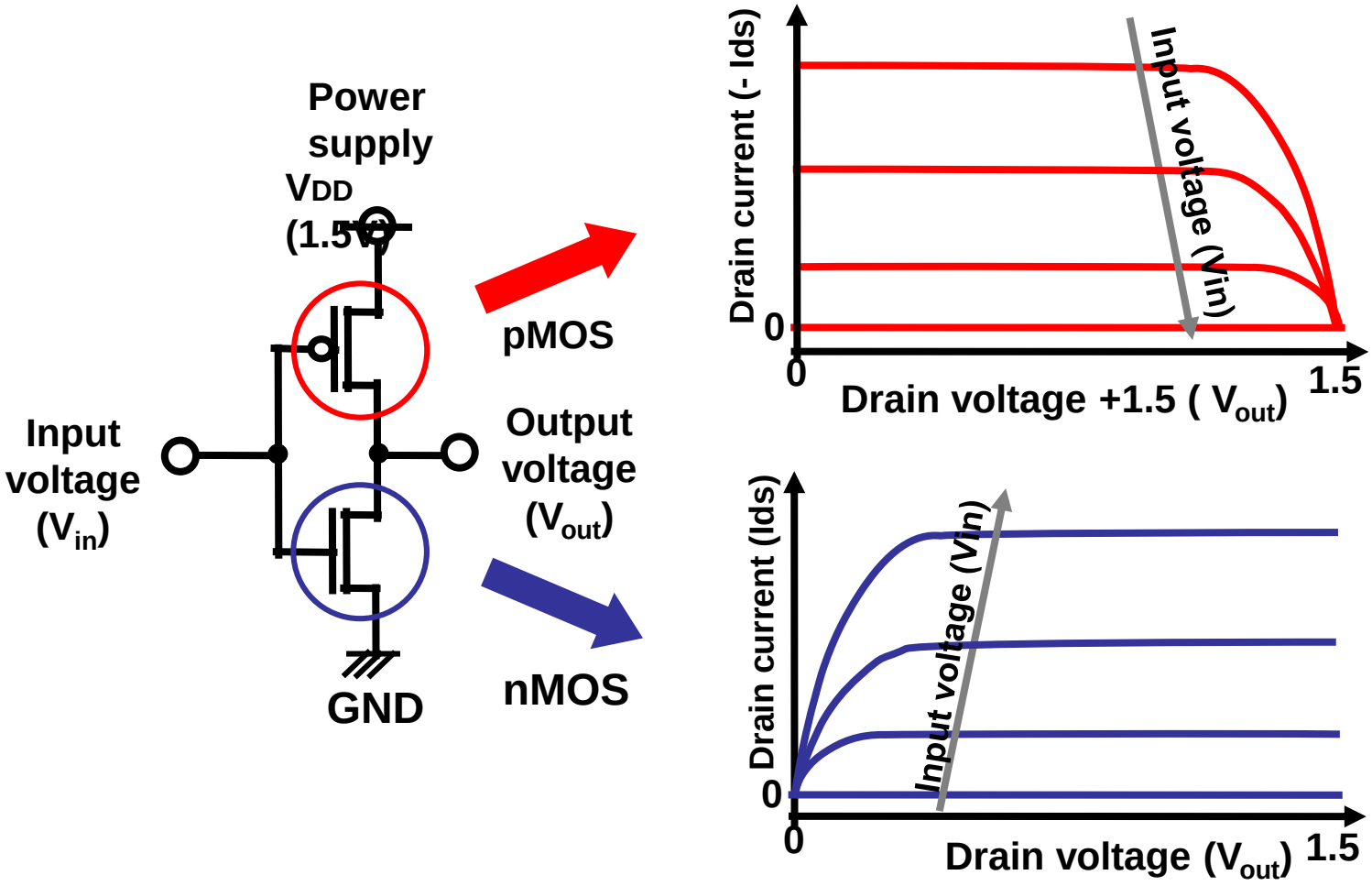
- **Inverter**
  - **Delay time**
  - **Power consumption**
- **Logic gate**
- **Logic Block**

Inverter



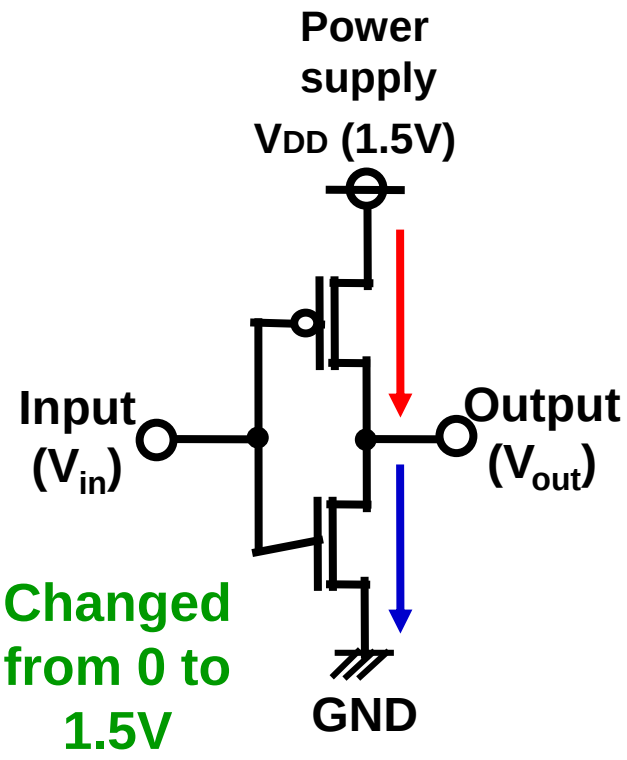
Simplest logic circuit with a pair of pMOS and nMOS transistors

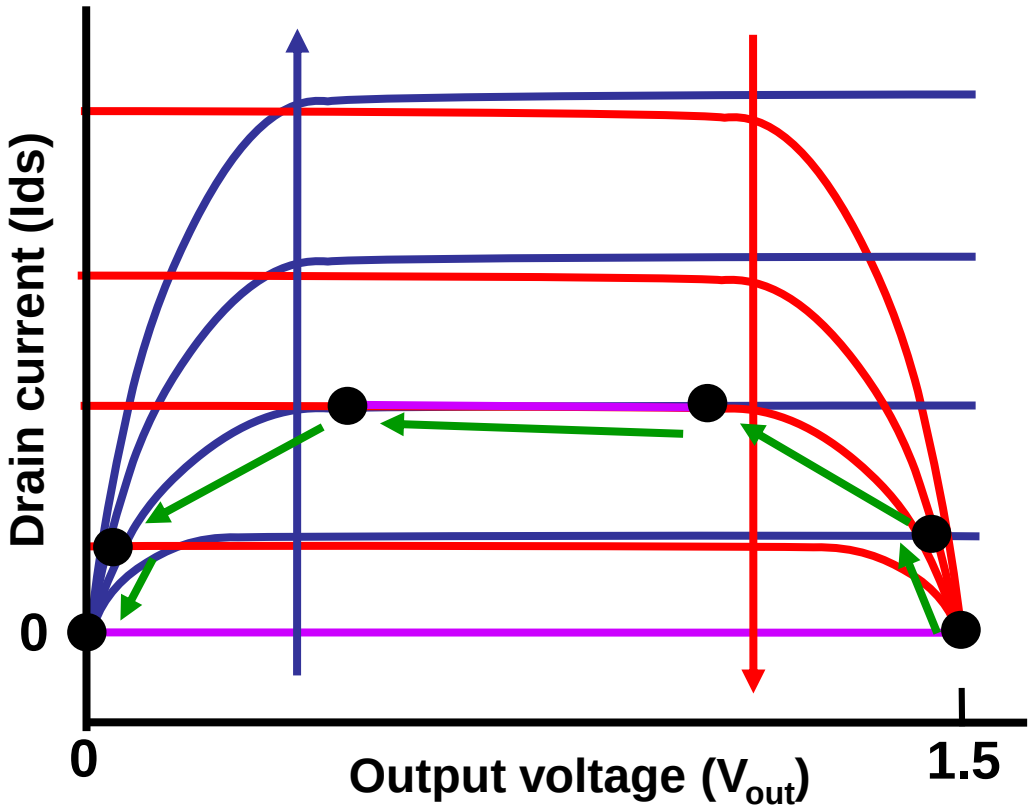
Current Characteristics



Inverter characteristics are defined by current characteristics of both transistors.

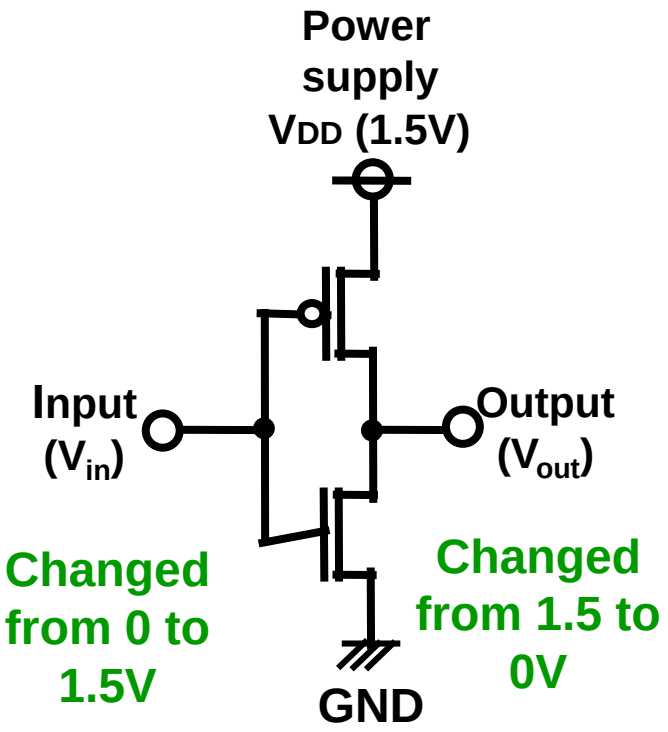
Behavior

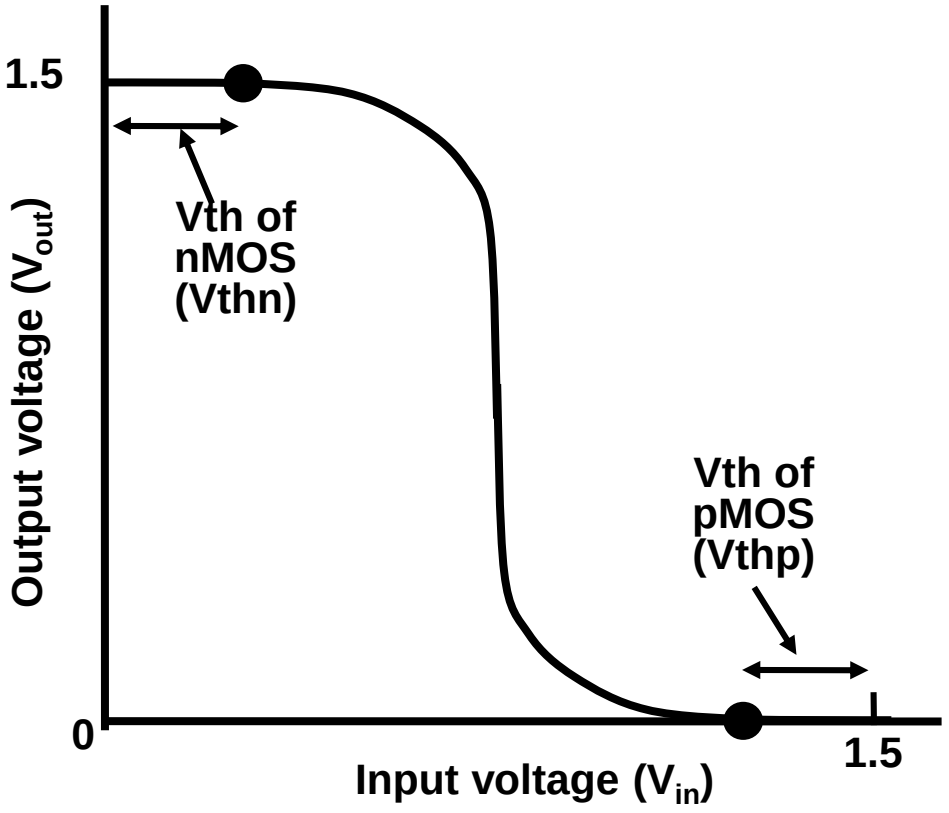




Output voltages (V_{out}) are determined by intersection points (● mark) of pMOS and nMOS current curves.

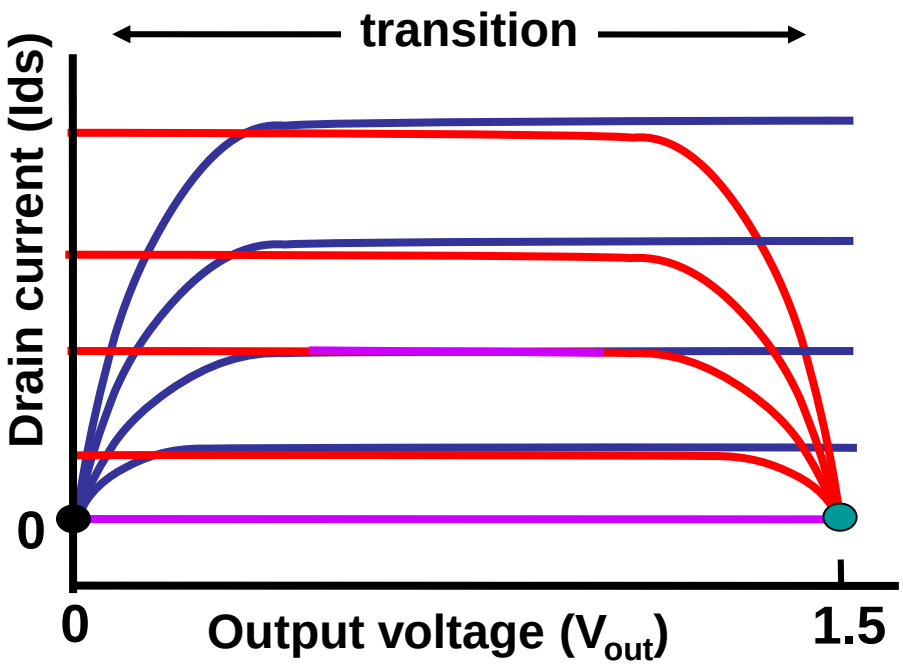
I/O Characteristics

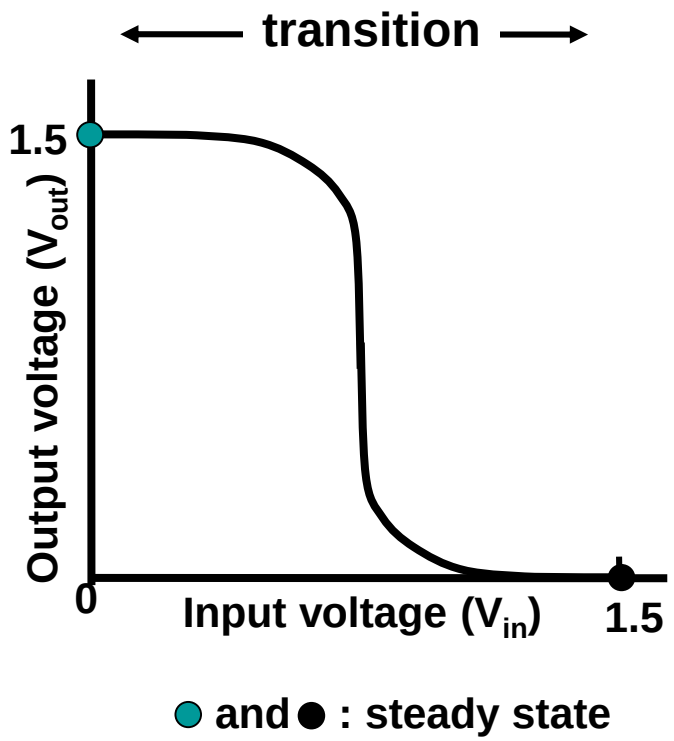




Signal logically inverted from input appears at output: inverter

Merits of CMOS Inverter

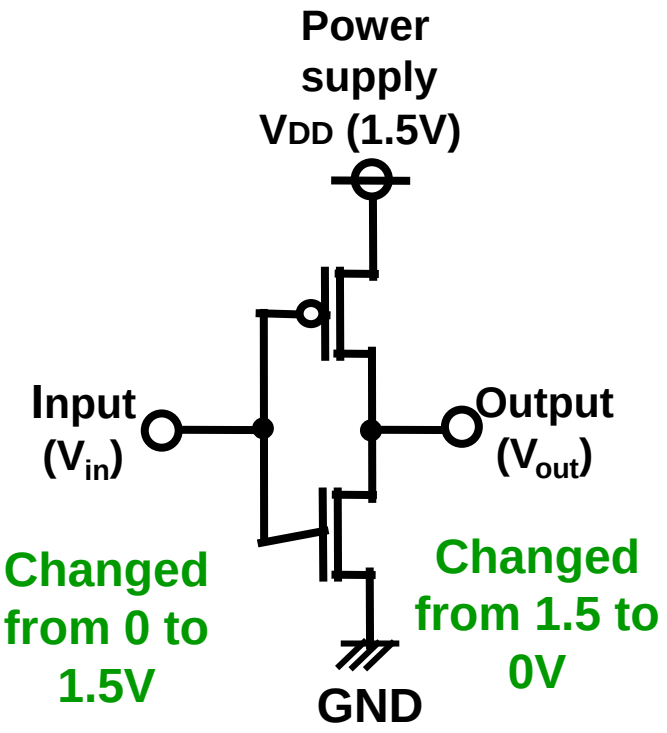


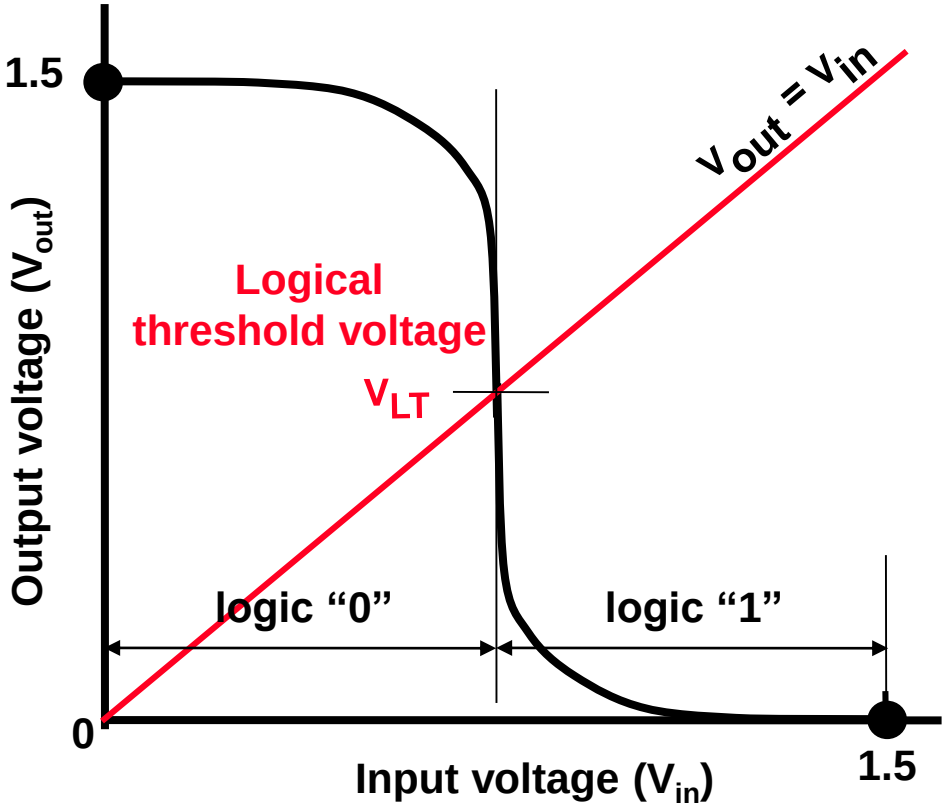


Complementary Operation

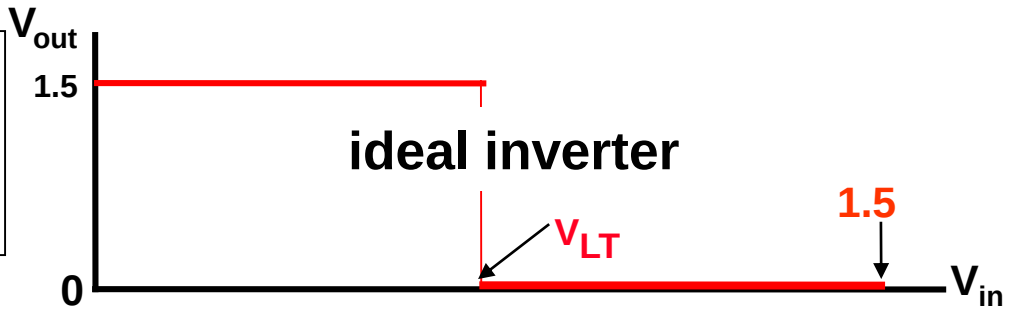
Either nMOS or pMOS is ON in steady state: no direct current flow.
Input and output voltages swing from 0 to 1.5v (V_{DD}).

Logical Threshold Voltage

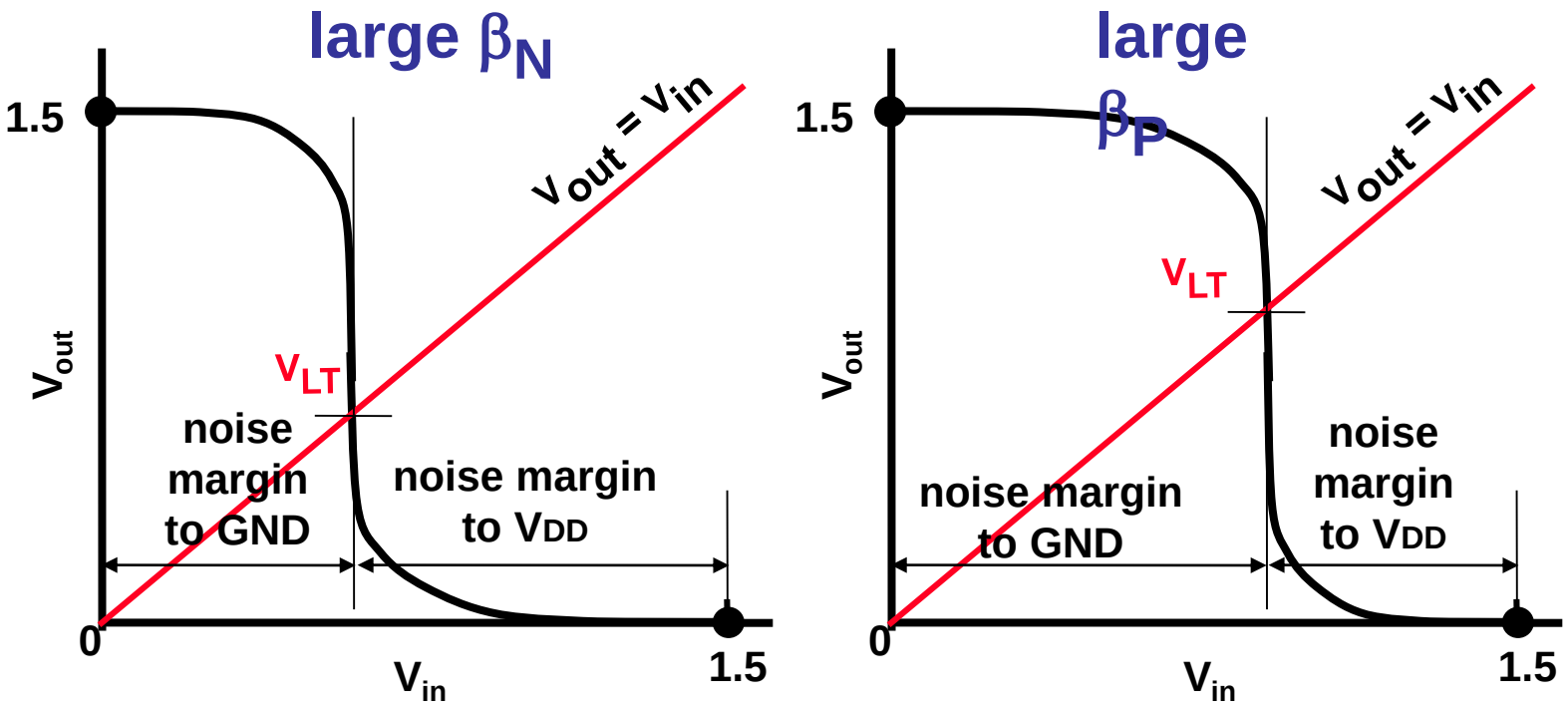




Vin < VLT:
  Inverter acknowledges input=logic0.
Vin > VLT:
  Inverter acknowledges input=logic1.



Noise Margins



To set logical threshold voltage of each gate at the same level is important to secure noise margin: $V_{LT} = V_{DD}/2$

Features of CMOS Circuit

Advantage	Disadvantage
(1) Low power dissipation	(1) Subject to Latch up
(2) Wide operating voltage range	(2) Complicated wafer process
(3) Large noise margin	(3) Large device area
(4) Wide operating temperature	

Let's take a 10-minutes BREAK

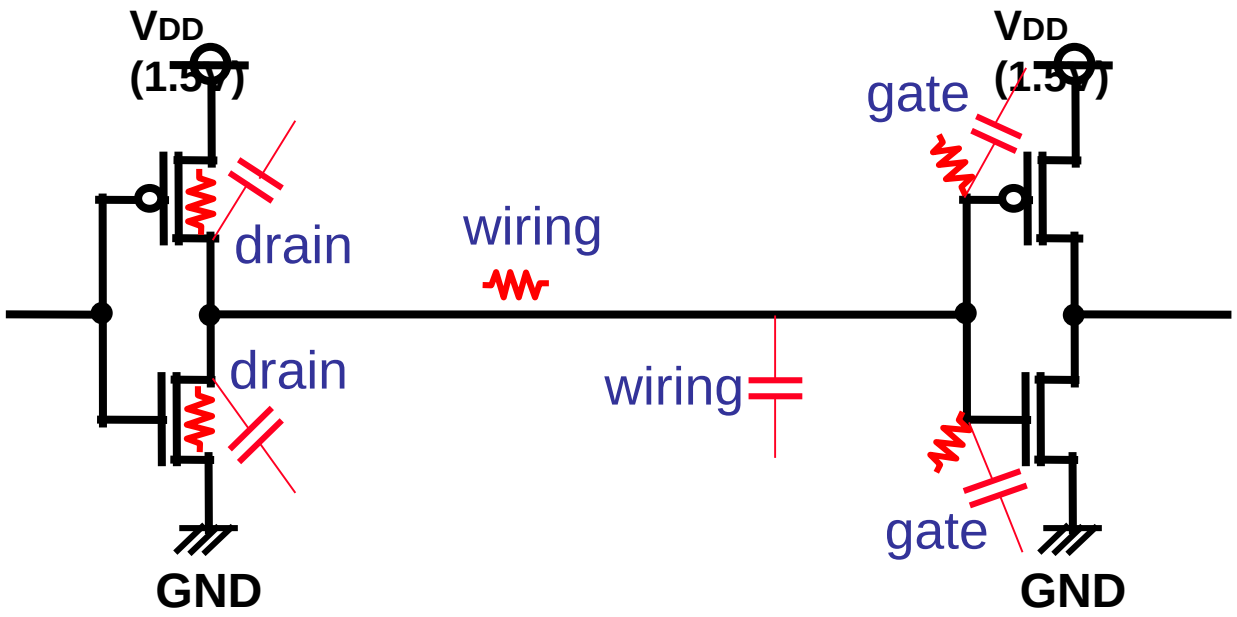
3.4 Basic CMOS Logic Circuits

- Inverter
  - Delay time
  - Power consumption
- Logic gate
- Logic Block

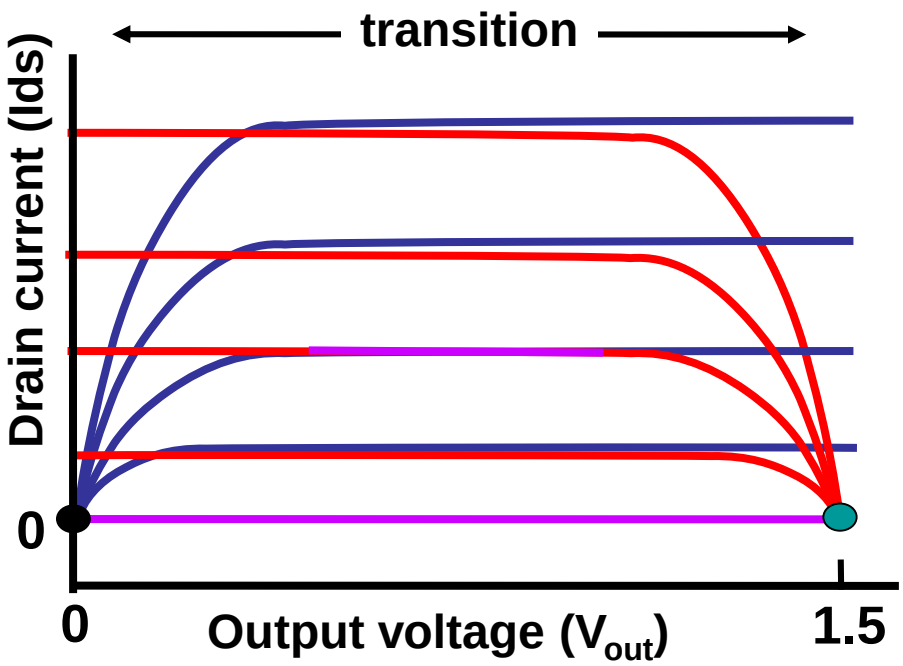
Circuit Model

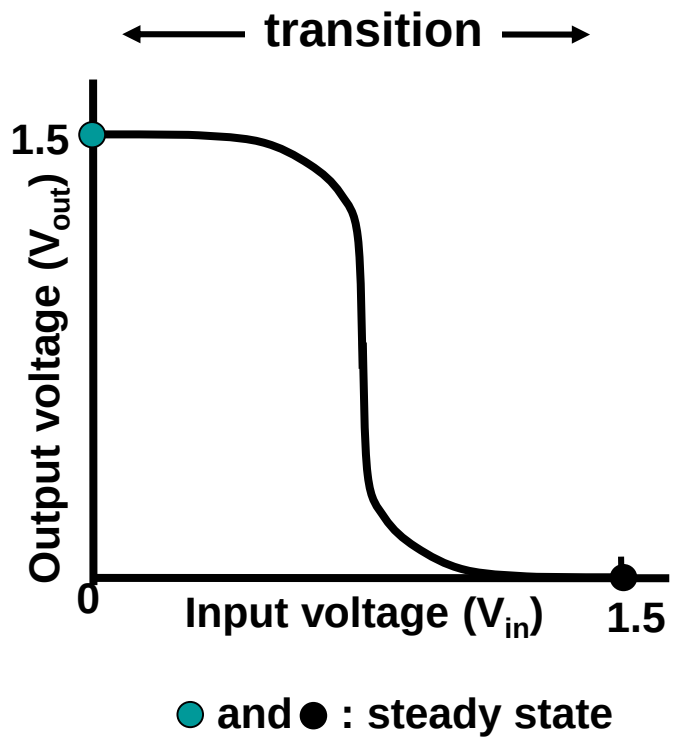
- for estimating delay time and power consumption -

An inverter chain with parasitic devices will be investigated.



Merits of CMOS Inverter



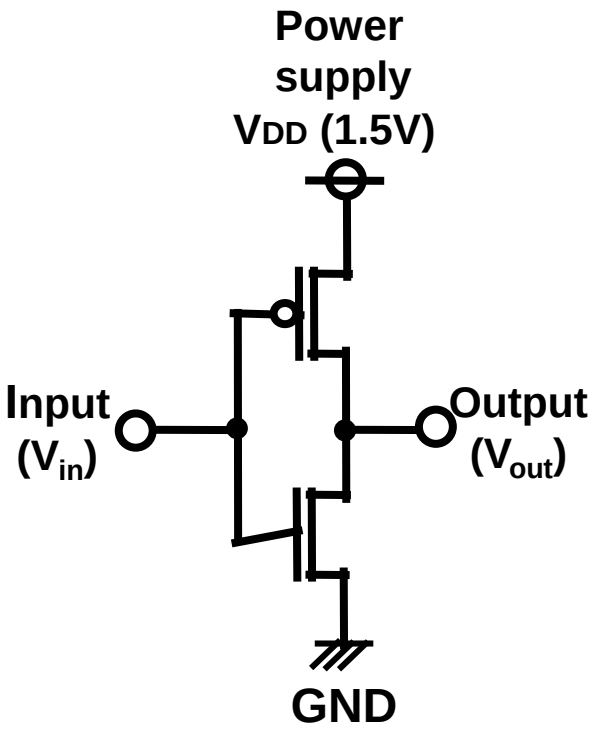


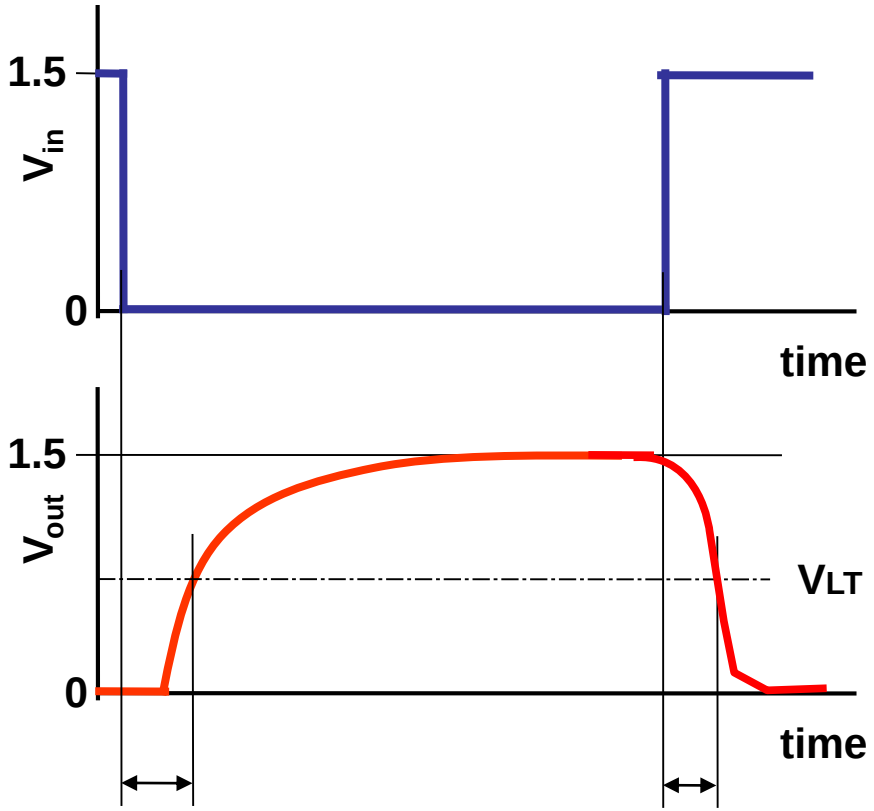
$$Id = \frac{W}{L} \mu Cox \; f(Vd, Vg)$$

for both nMOS and pMOS

- time-varying functions
- multi-dimensional differential equations

Delay Time

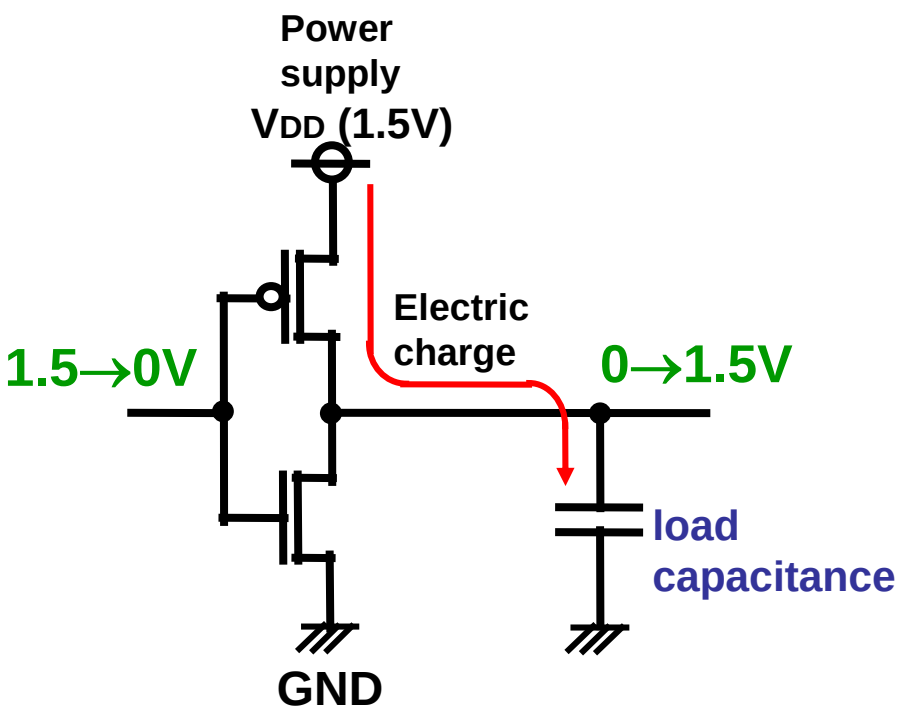




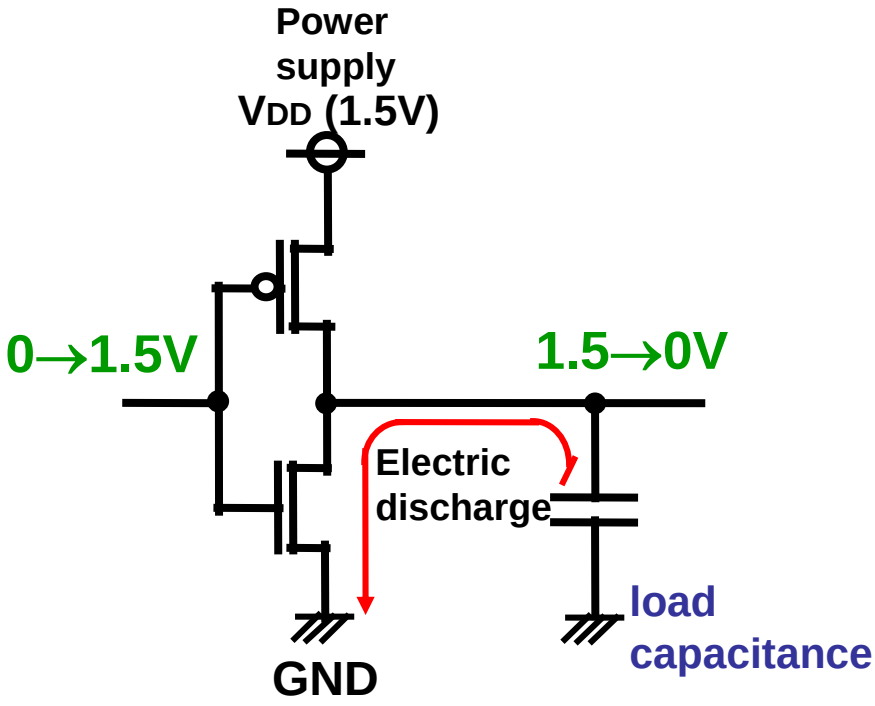
Delay time (rising) Delay time (falling)

Propagation delay time

< Propagation of “1→0” >



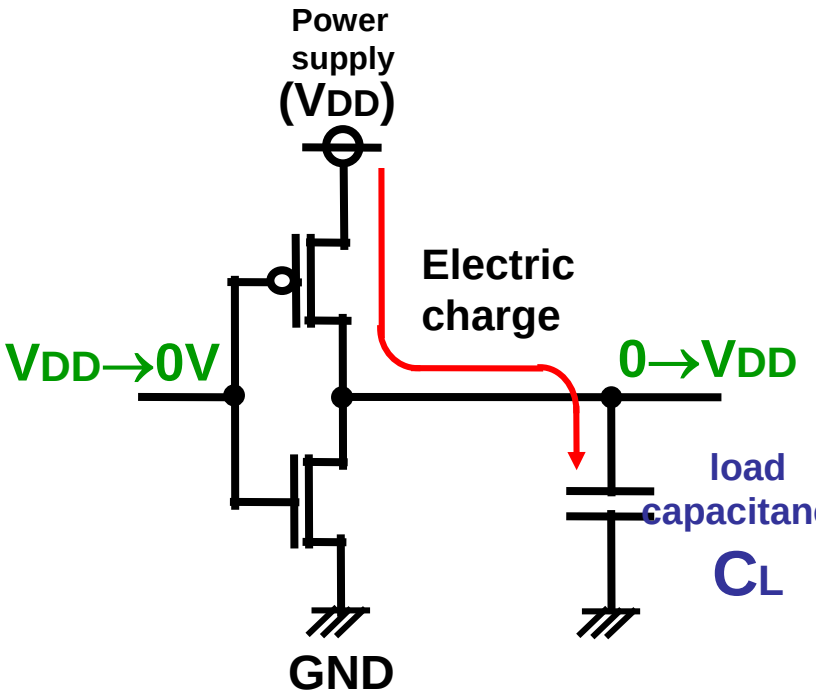
< Propagation of “0→1” >



- ◆Electric charging / discharging at load capacitance take time: delay is caused.
- ◆Load capacitance : stray capacitance of wiring, junction capacitance at drains, gate capacitance of succeeding circuit

Delay Time for Charging

< “1→0” propagation>



◆ Current flows when pMOS is ON,

$$Ids = -\beta p \cdot (-V_{DD}-Vthp)^2$$
$$= -\beta p \cdot (V_{DD}-|Vthp|)^2$$

◆ Electric charge to be charged

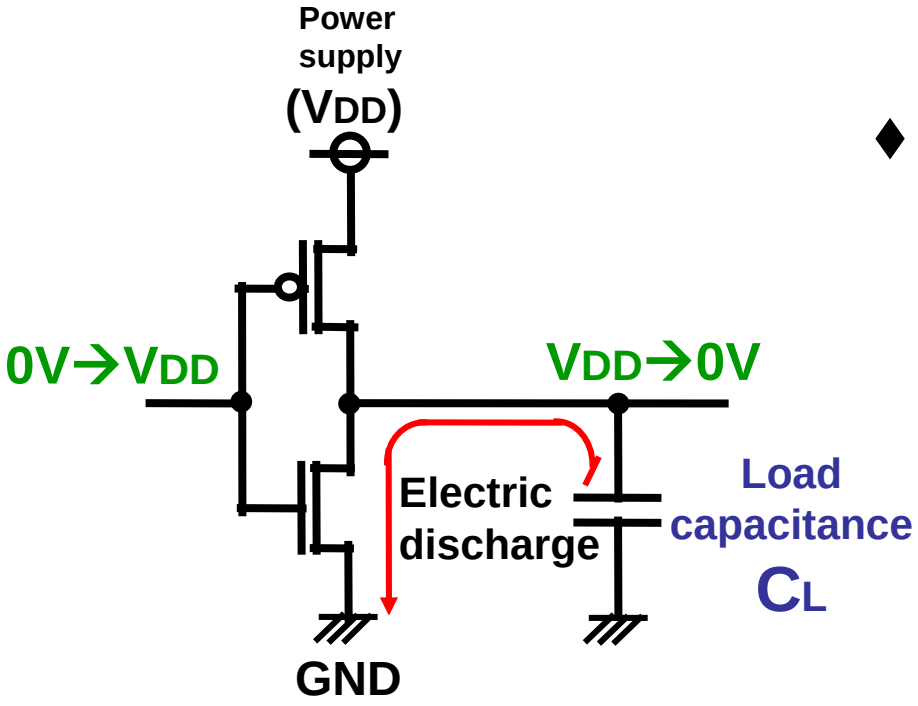
$$Q = C_L \cdot V_{DD}$$

Delay time is

$$Td = Q/|Ids|$$
$$= \frac{C_L \cdot V_{DD}}{\beta p \cdot (V_{DD}-|Vthp|)^2}$$

Delay Time for Discharging

< “0→1” propagation>



♦ Current flows when nMOS is ON,

$$Ids = \beta n \cdot (V_{DD} - Vthn)^2$$

♦ Electric charge to be discharged

$$Q = C_L \cdot V_{DD}$$

Delay Time is,

$$Td = Q/Ids$$

$$= \frac{C_L \cdot V_{DD}}{\beta n \cdot (V_{DD} - Vthn)^2}$$

Summary of Delay Time

$$Td = \begin{cases} \dfrac{C_L \cdot V_{DD}}{\beta p \cdot (V_{DD}-|Vthp|)^2} & : \text{rising} \\ \dfrac{C_L \cdot V_{DD}}{\beta n \cdot (V_{DD}-Vthn)^2} & : \text{falling} \end{cases}$$

- Faster, if load capacitance CL is smaller
- Faster, when power supply voltage, V_{DD} is higher
- Faster, if |Vth| is smaller
- Faster, if β is greater

$$\beta = \mu * Cox * W/2L$$

Mobility

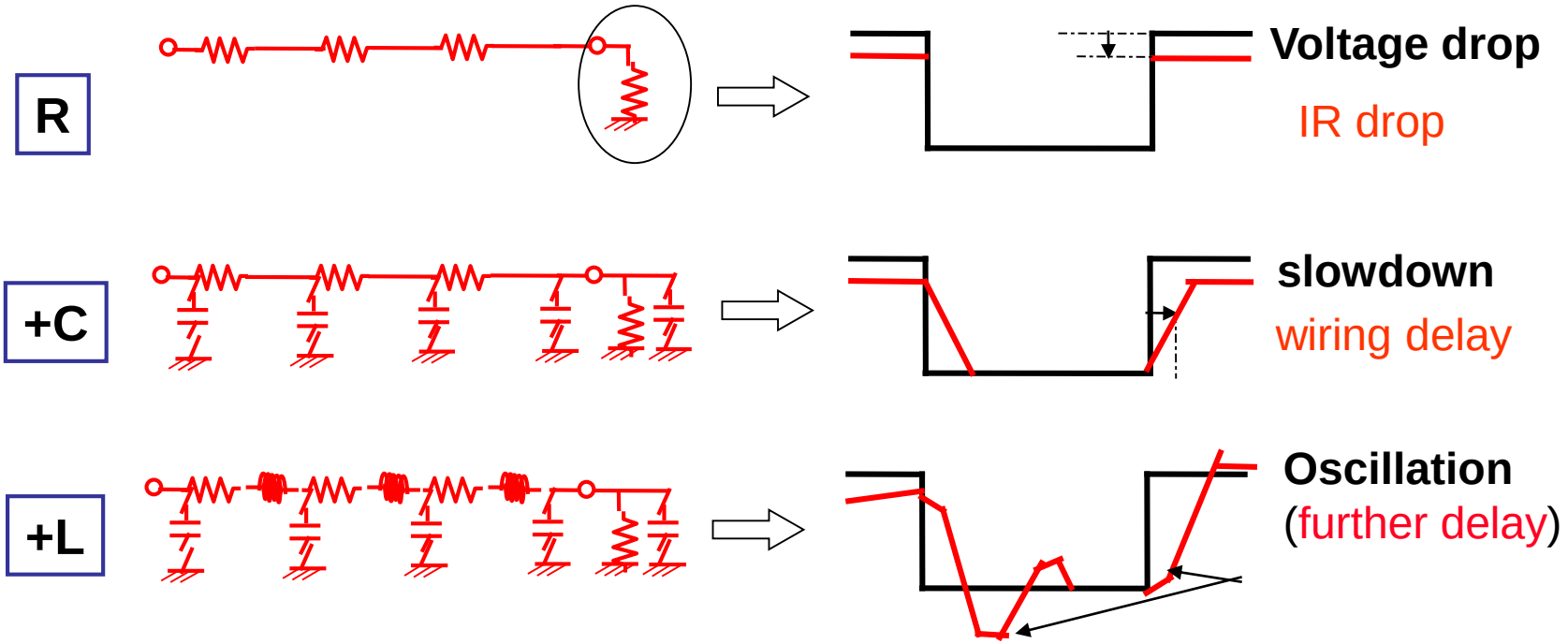
Capacity of gate oxide

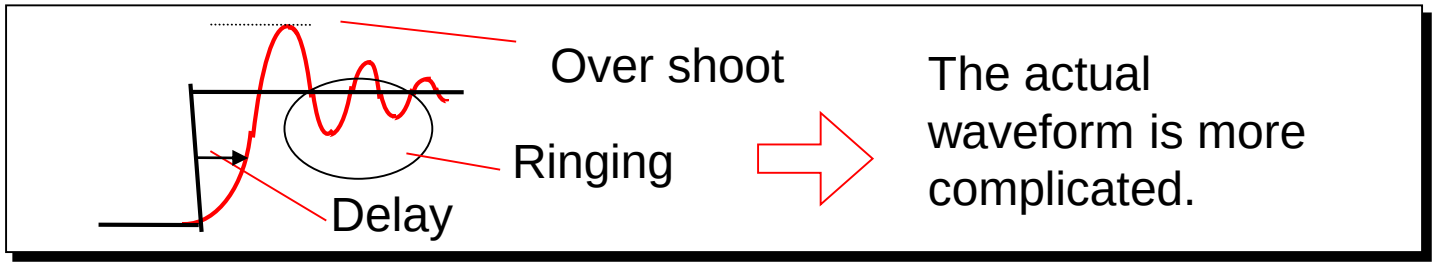
- Faster, if gate length L is shorter
- Faster, if gate width W is wider

But min. L exists!

Further Disturbances

Influence of R, C and L





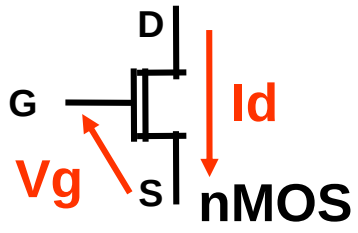
3.4 Basic CMOS Logic Circuits

Afternoon Section

- Review morning Section – Q&A
- Inverter
  - Delay time
  - Power consumption
- Logic gate
- Logic Block

Review Morning Section – Q&A

Exercise 1



Linear region $(0 \leqq Vd \leqq Vg-Vth)$

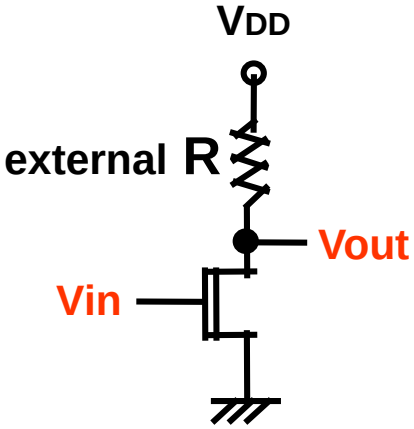
$$Id = \frac{W}{L} \mu Cox \left\{(Vg-Vth)Vd - \frac{1}{2}Vd^2\right\}$$

Saturation region $(Vd > Vg-Vth)$

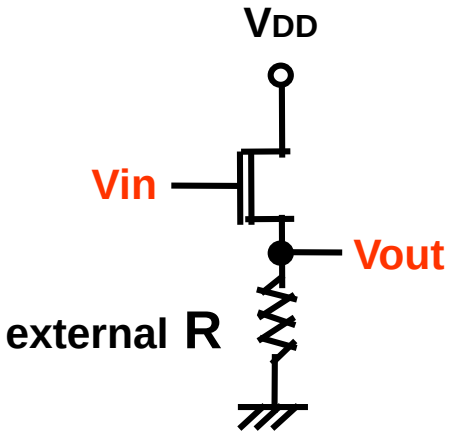
$$Id = \frac{W}{2L} \mu Cox (Vg-Vth)^2$$

$\alpha = \mu CoxW/2L$

Vin is connected to Vdd, and R becomes infinity, then Vout =?



Vout =



Vout =

Power Consumption

- Actual LSI power consumption is time variant, but generally represented by its average value. This is important figure for longer battery shutoff time.

- Breakdown of average power consumption P:

$$P = P_{dynamic} + P_{SC} + P_{leak}$$

$P_{dynamic}$: Dynamic power

P_{SC} : Short Circuit power

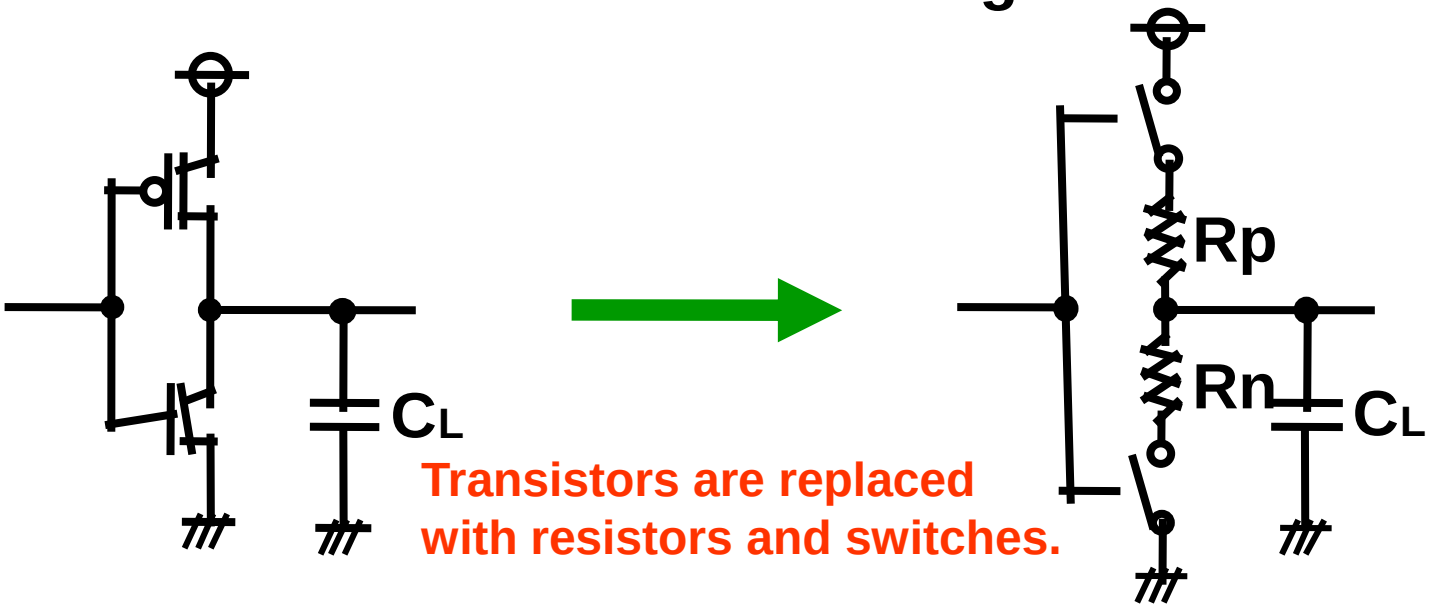
P_{leak} : Leakage power

- Start from simple inverter case

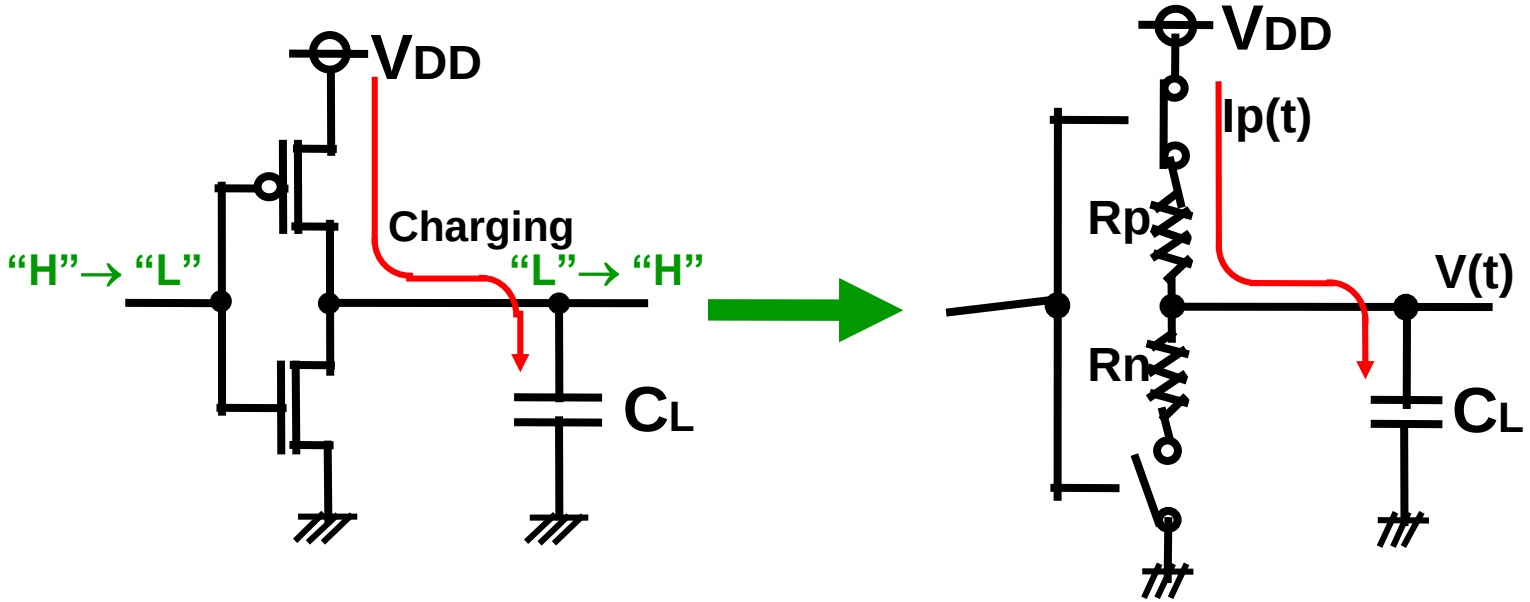
Dynamic power

- Power consumption due to charging and discharging of load capacitance
- Basically IV, I^2R, V^2/R are represented by functions of time.

→ The following simplified, computational model is used to obtain average value of time



Charging



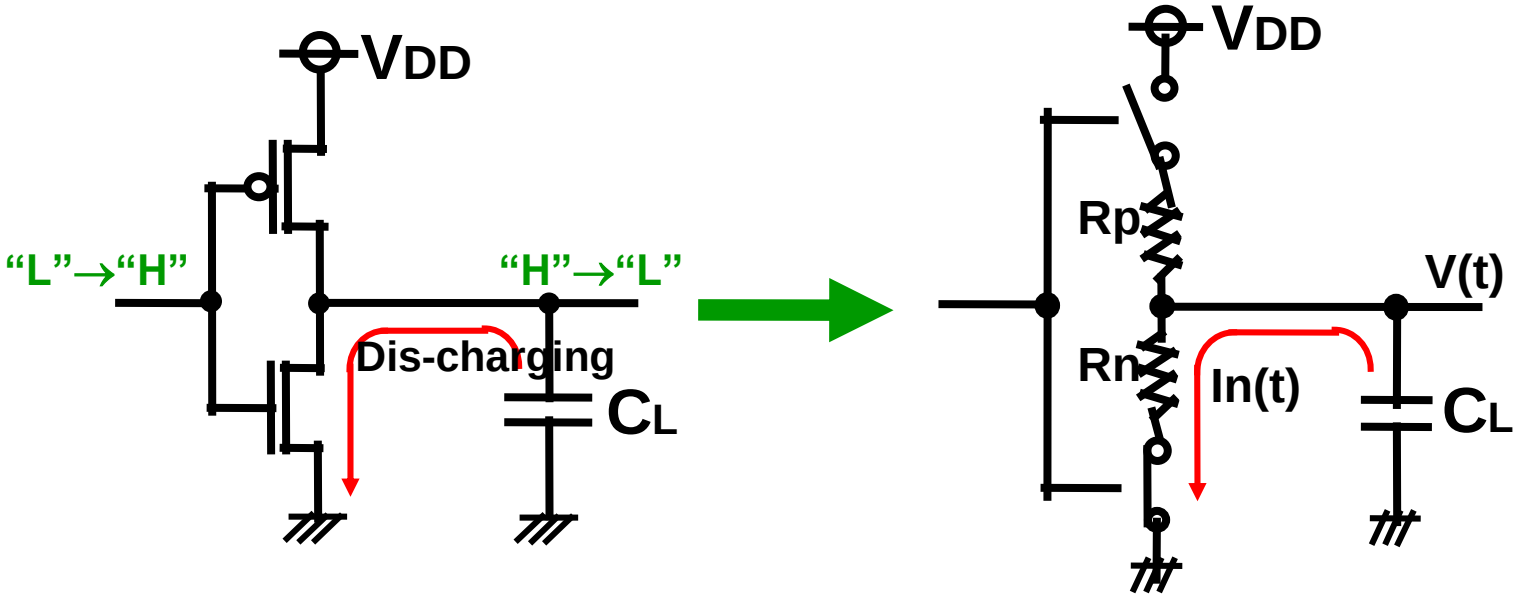
$$C_L \frac{dV}{dt} = I_P$$

Power $= (V_{DD}-V) \cdot I_P$: function of time

$$\text{Energy} = \int_{t=0}^{\infty} (V_{DD}-V) \cdot I_P \, dt = \int_{V=0}^{V_{DD}} C_L \cdot (V_{DD}-V) dV$$

$$= \frac{1}{2} C_L \cdot V_{DD}^2$$ ← Rp independent

Discharging



$$-C_L \frac{dV}{dt} = I_n$$

Power $= V \cdot I_n$: function of time

$$\text{Energy} = \int_{t=0}^{\infty} V \cdot I_n \, dt = \int_{V=V_{DD}}^{0} -C_L \cdot V \, dV$$

$$= \frac{1}{2} C_L \cdot V_{DD}^2$$ ← Rn independent

Dynamic Power of Inverter

◆ **Energy consumed during one cycle of inverter toggle operation**

$$\frac{1}{2}C_L \cdot V_{DD}^2 \quad + \quad \frac{1}{2}C_L \cdot V_{DD}^2 \quad = \boxed{C_L \cdot V_{DD}^2}$$

(Charging energy) (Discharging energy)

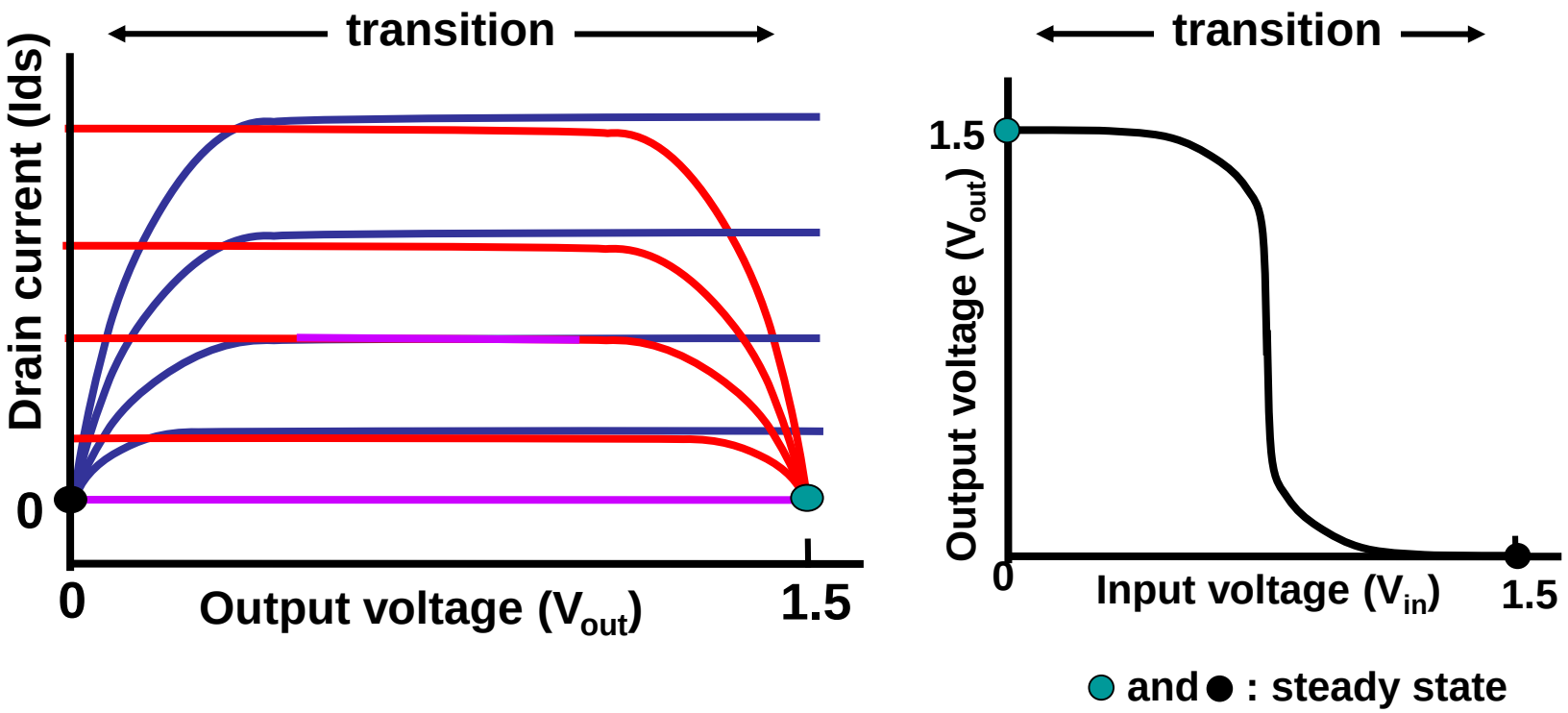
Energy consumption of inverter is defined by power supply voltage and parasitic capacitance, irrespective of Rp and Rn resistors.

◆ **Power consumption (= energy consumed in 1 second)**

Assuming inverter toggles f times in 1 second, thus average dynamic power is represented by $f \cdot C_L \cdot V_{DD}^2$

Although simplified equation, comprehend relation among dimensions.

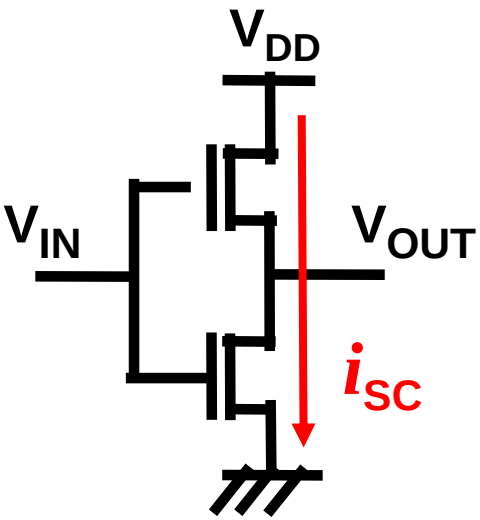
Complementary Operation (restudy)

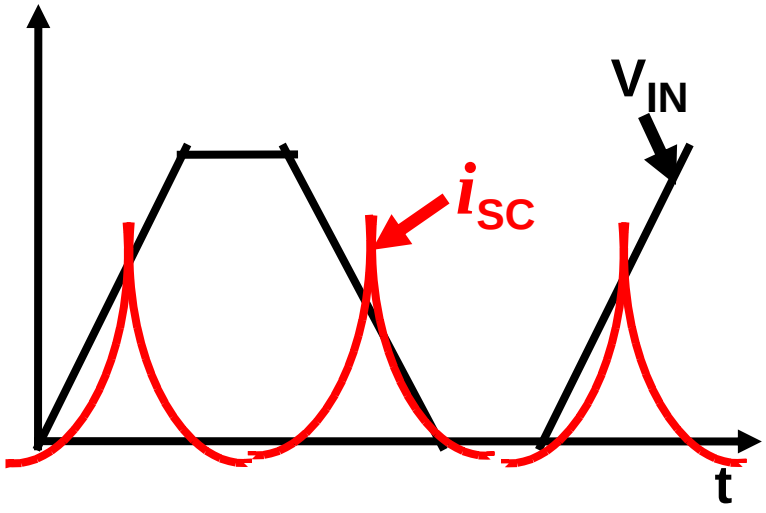


Either nMOS or pMOS is ON in steady state: no direct current flow.
→ Complementary operation, BUT, BUT, BUT!
Input and output voltages swing from 0 to 1.5v (V_{DD}).

Short-Circuit Power

- When inverter switching occurs, inrush, short circuit current i_{SC} flows from V_{DD} to GND during state transition, which actually dissipates power.
- Short-circuit power remains 10~15% of overall power consumption, as long as circuits are designed so that their input transition time and output one are equal.
- Short-circuit power is proportional to operating frequency.



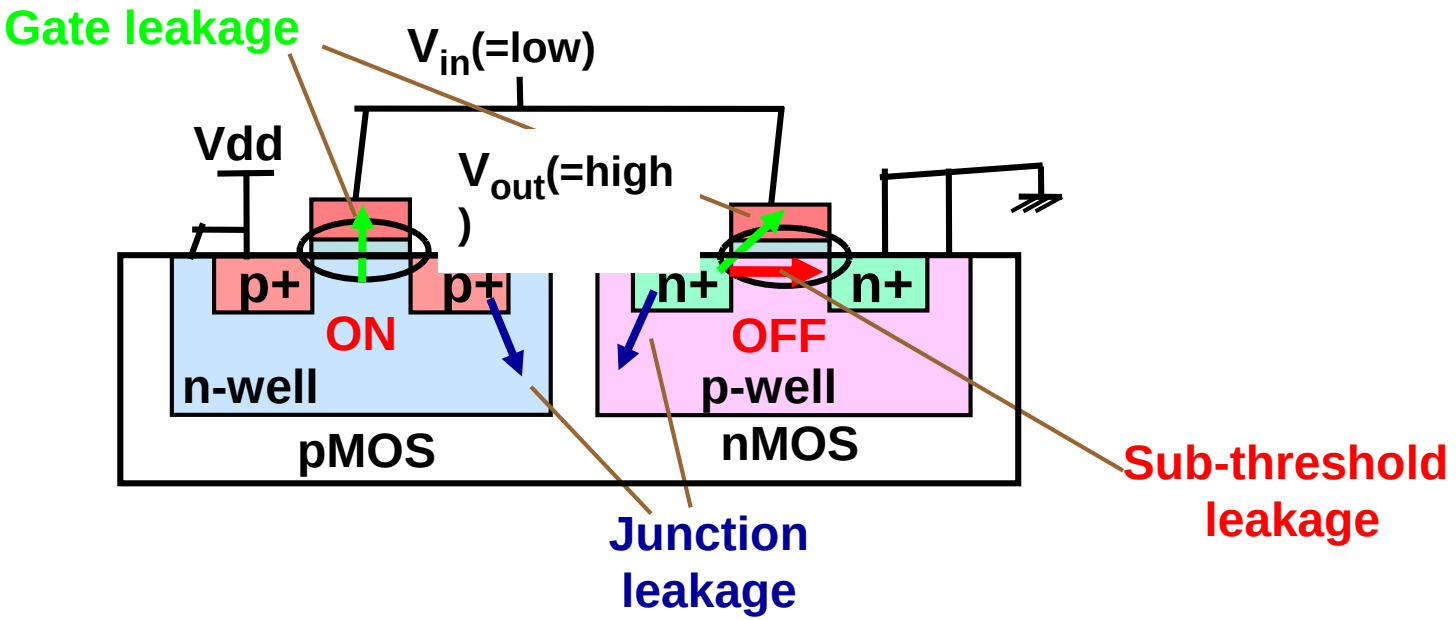


Leakage Power

- Power consumption due to leakage current :

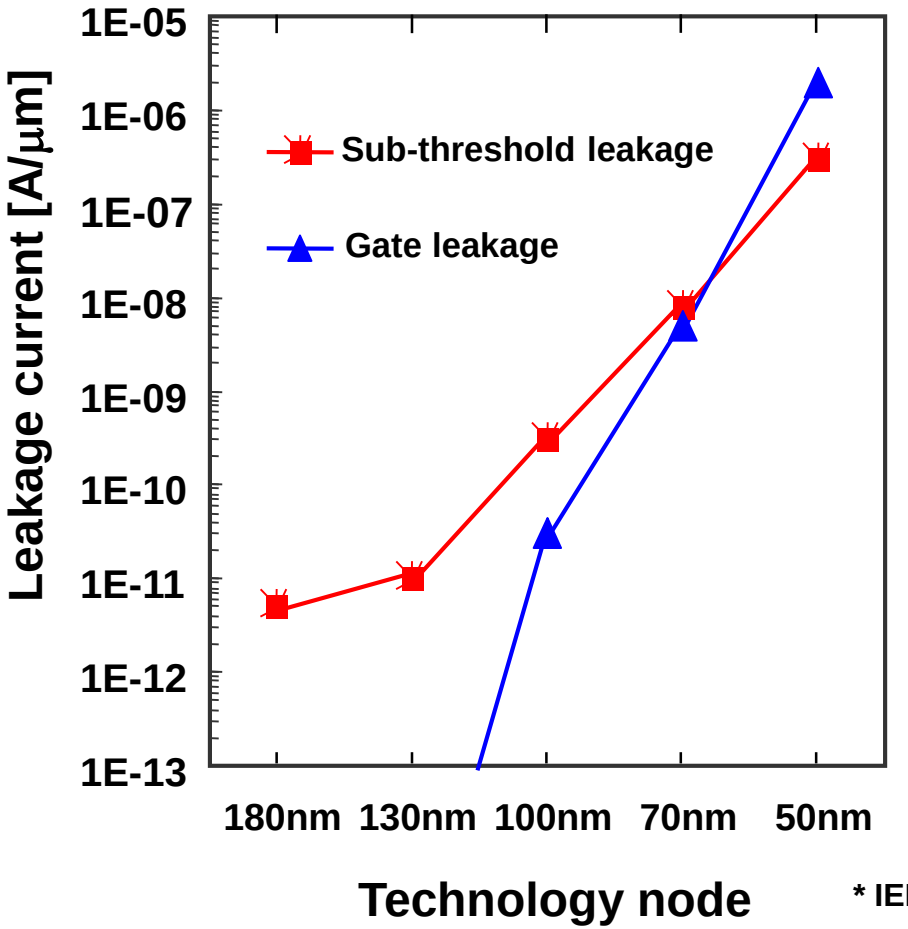
  $I_{leak} \cdot V_{DD}$

- Breakdown of I_{leak} :
  - Reverse-bias current of source and drain junctions: junction leak
  - Sub-threshold leakage at channel
  - Gate leakage at gate oxide



Trend of MOS Leakage Current

(excerpt from CICC-00*, pp.409-412, 2000, T. Inukai et al.)



- Both sub-threshold and gate leakage are increased along with evolution of technology node.
- Gate leakage will become more dominant.

→Serious problem in reducing power consumption

* IEEE 2000 Custom Integrated Circuits Conference

Dynamic Power of CMOS LSI

- Dynamic power of entire LSI is shown in the following expression by using activation rate α, by considering that whole circuits are not actively operating all the time.

$$Pdynamic = \alpha \cdot f \cdot \Sigma C_L \cdot V_{DD}^2$$

α : average activation rate of the circuit (empirical)

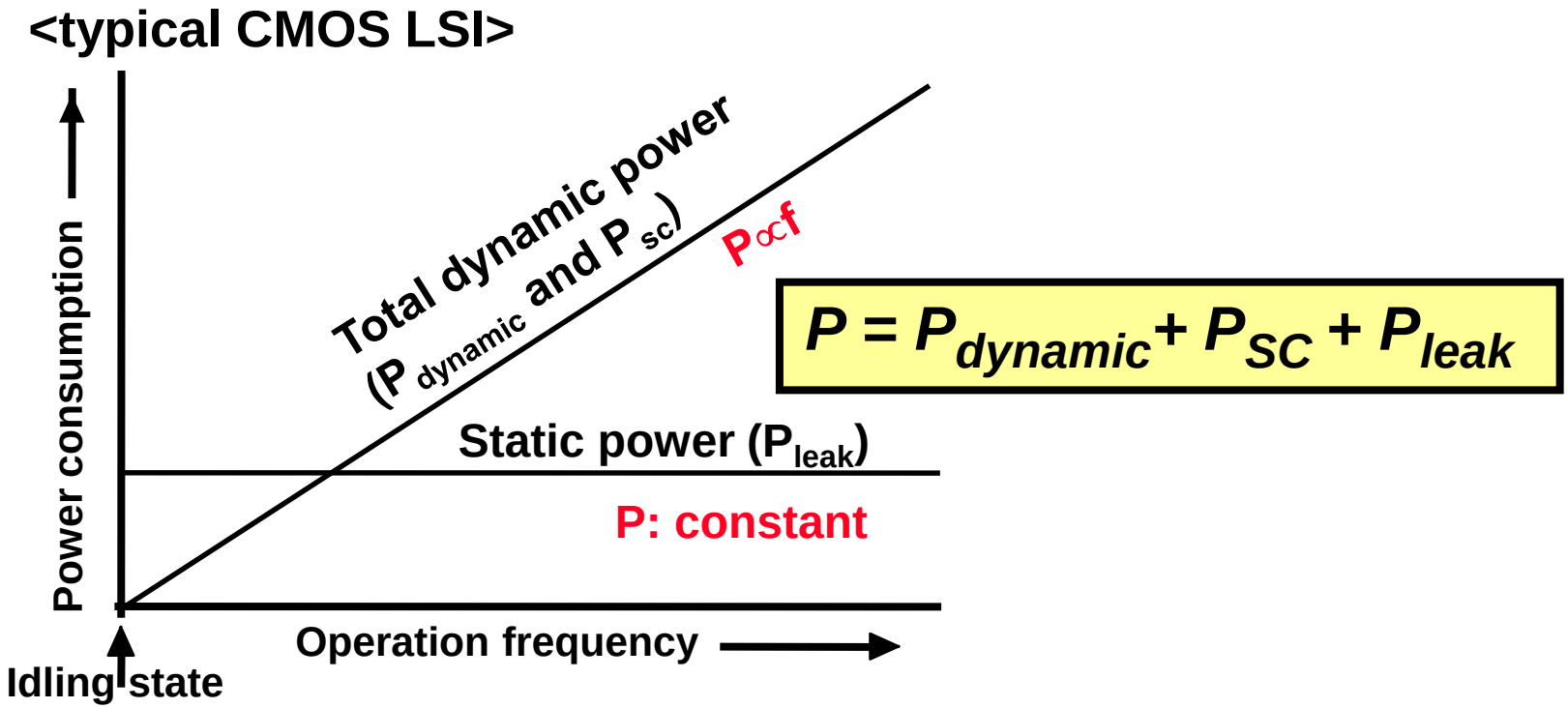
f : operation frequency

ΣC_L : aggregate parasitic capacitance of entire LSI

V_{DD}: power supply voltage

- The equation above is conceptual. In actual designs, design tools are used to tentatively estimate the entire power dissipation during logic synthesis.

Dynamic And Static Power Consumption



- Static power consumption is dominant during low-speed and idle operations.
- Dynamic power consumption is dominant during high-speed operation. However, due to increases in leakage current (sub threshold and gate) and circuit complexity, static power consumption becomes critical even in high-speed operation area.

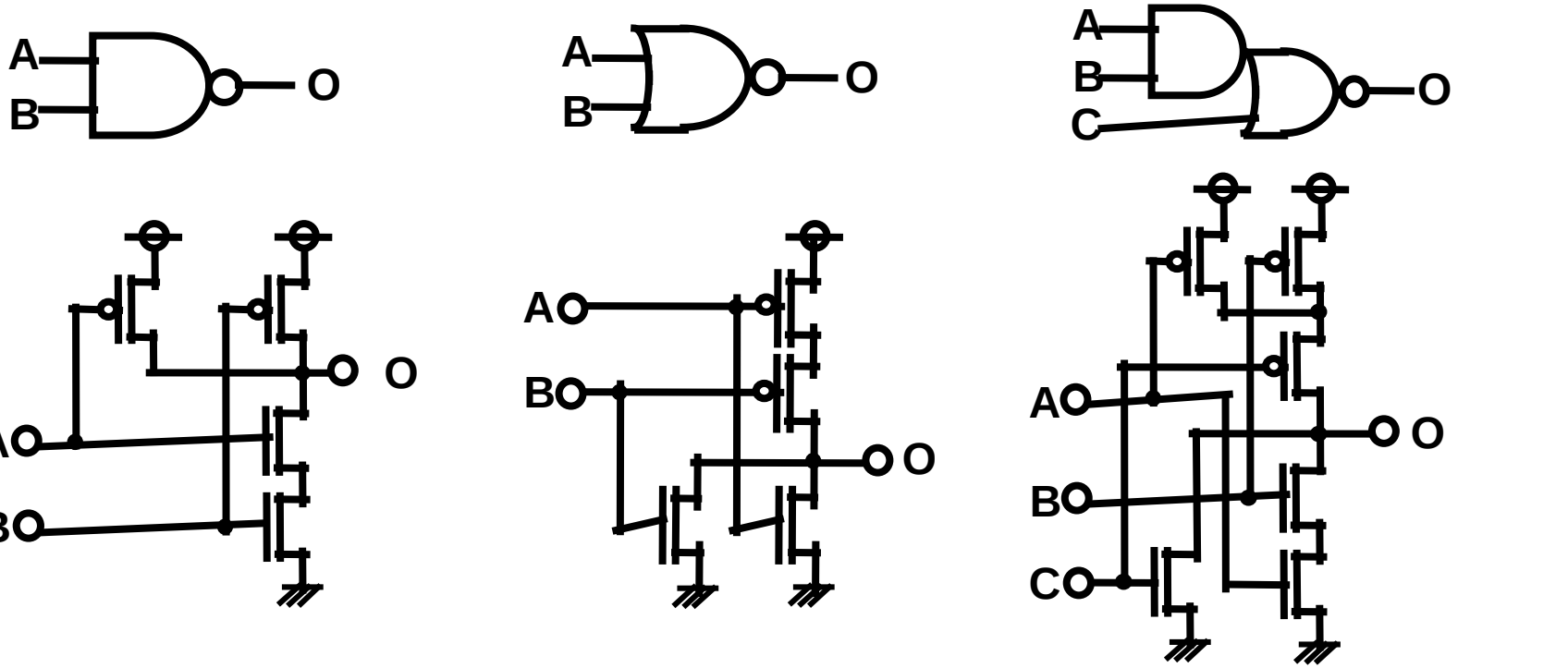
3.4 Basic CMOS Logic Circuits

- Inverter
- Logic gate
- Logic Block

Logic Gate

Examples of logic gates

- 2 input NAND ($O=\overline{A \cdot B}$)
- 2 input NOR ($O=\overline{A+B}$)
- Combinational gate ($O=\overline{A \cdot B+C}$)



- With complementary transistor configurations, all logic circuits can be implemented.
- Basically their complementary operations are similar to those of an inverter.

Basic Rules for Logic Gate Configuration

pMOS:

Logical product in parallel

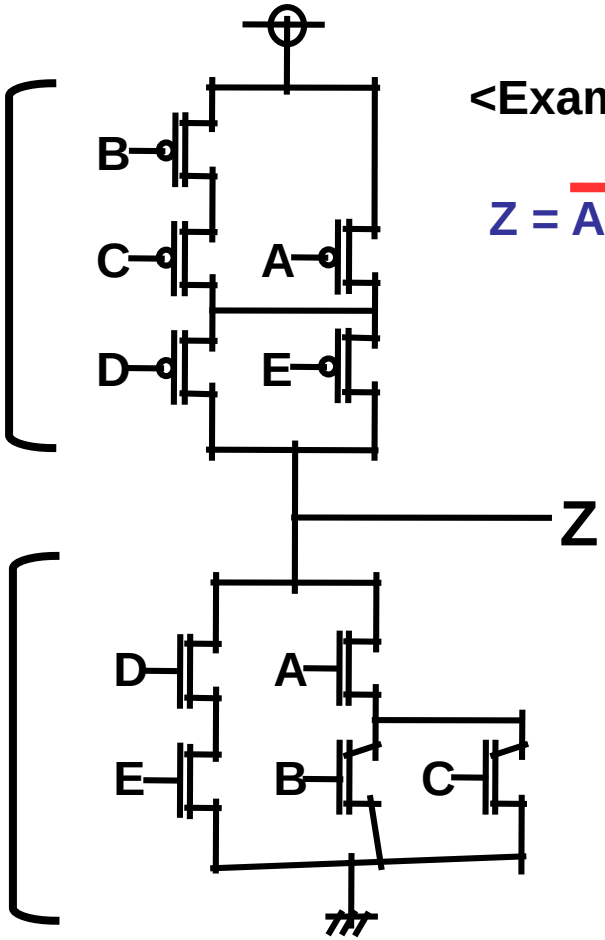
Logical addition in serial

Duality

nMOS:

Logical addition in parallel

Logical product in serial



over-bar

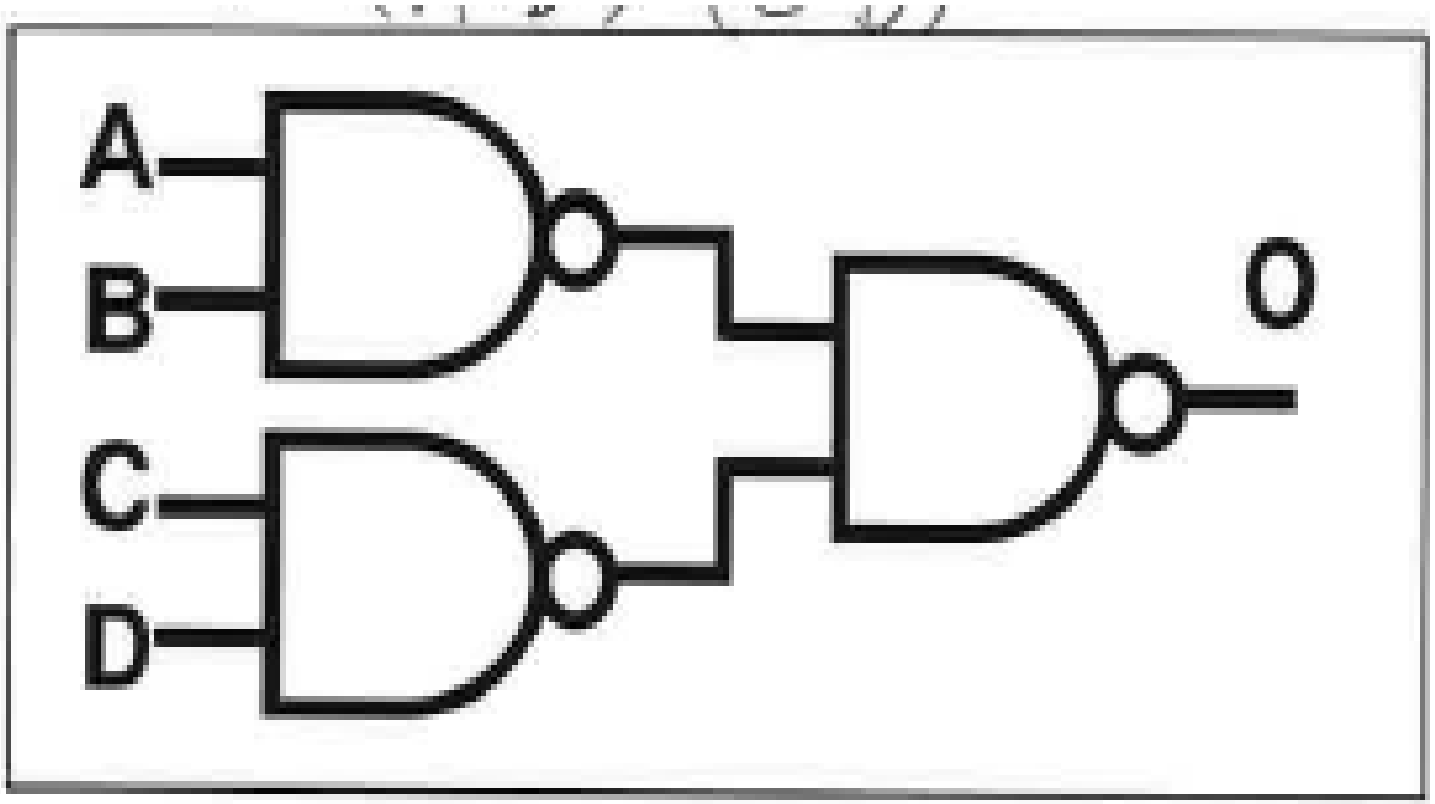
<Example>

$Z = \overline{A \bullet (B+C) + D \bullet E}$

According to these rules, any logic gate can be implemented in a complementary way.

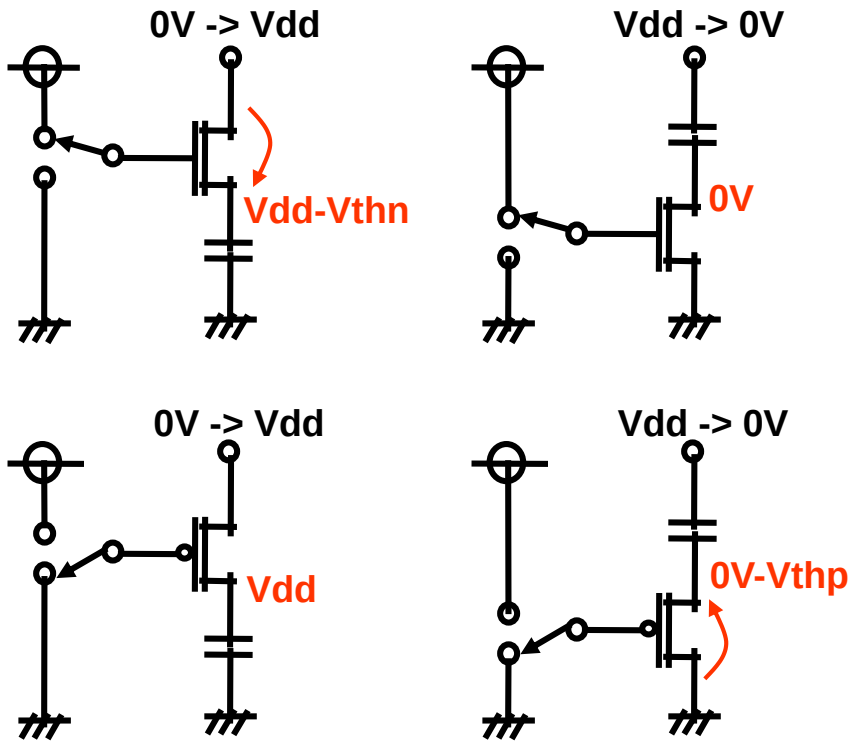
Exercise 2

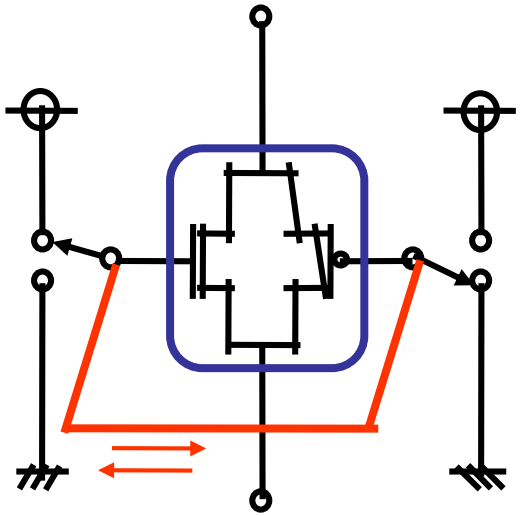
Draw CMOS circuit for below logic gate



Transistor Switches

Voltage reduction by Vth





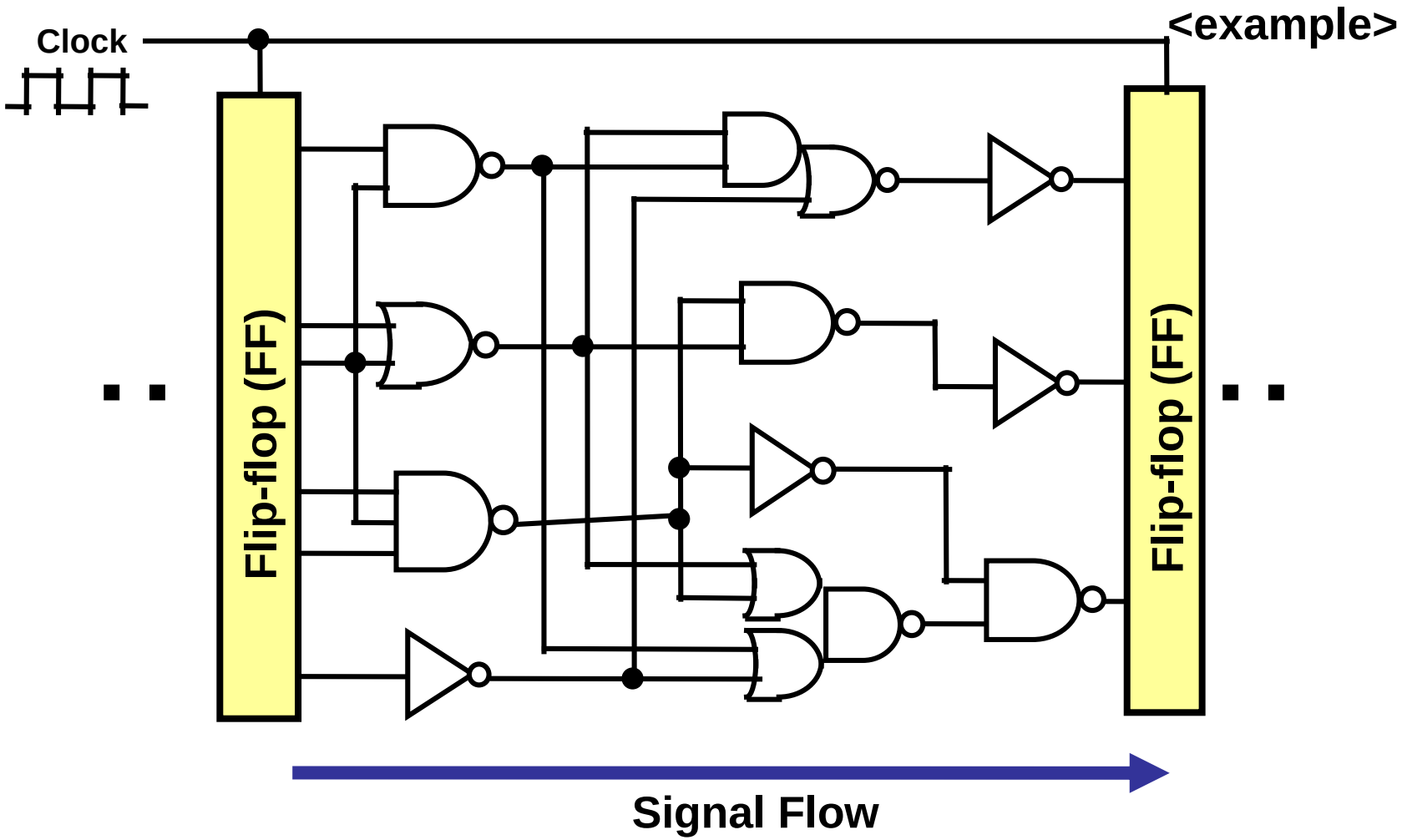
Complementary Switch

Voltage reduction by Vth can be prevented by complementary operations.

3.4 Basic CMOS Logic Circuits

- Inverter
  - Delay time
  - Power consumption
- Logic gate
- Logic Block

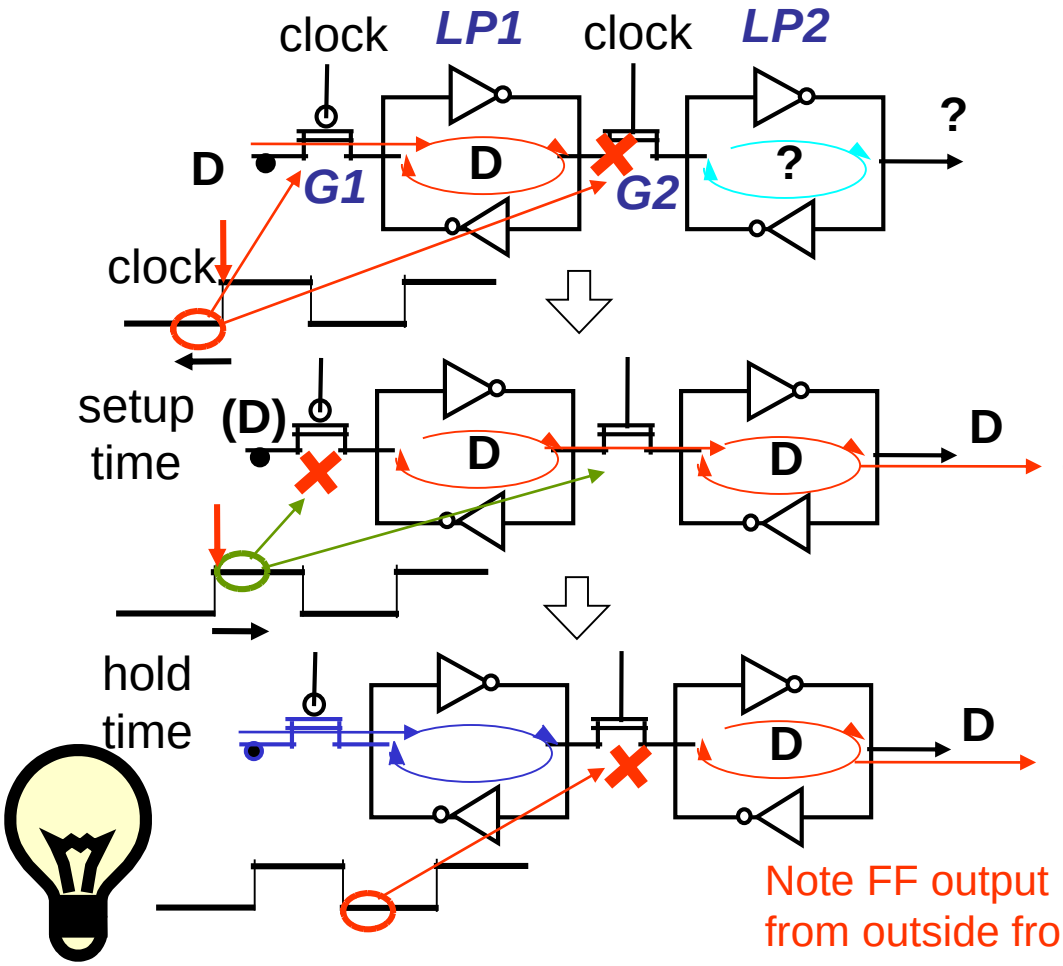
Standard Organization of Logic Block



FF: A circuit that holds the input data and transmits it to the next stage by using a clock signal.

Flip Flops

Principle of operation



The figures shown left are a simplified example.

1. Gate G1 is ON while clock remains low, and data D is taken into loop LP1.

2. When clock rises, G1 is OFF and G2 is ON to pass data D into next loop LP2.

3. When clock goes low, G2 is OFF and LP2 keeps its data D.

Note FF output is not determined until any value is set from outside from logic simulation standpoint. Especially cares should be taken after power on.

Key Components of Logic LSI

<Control Logic Circuit>

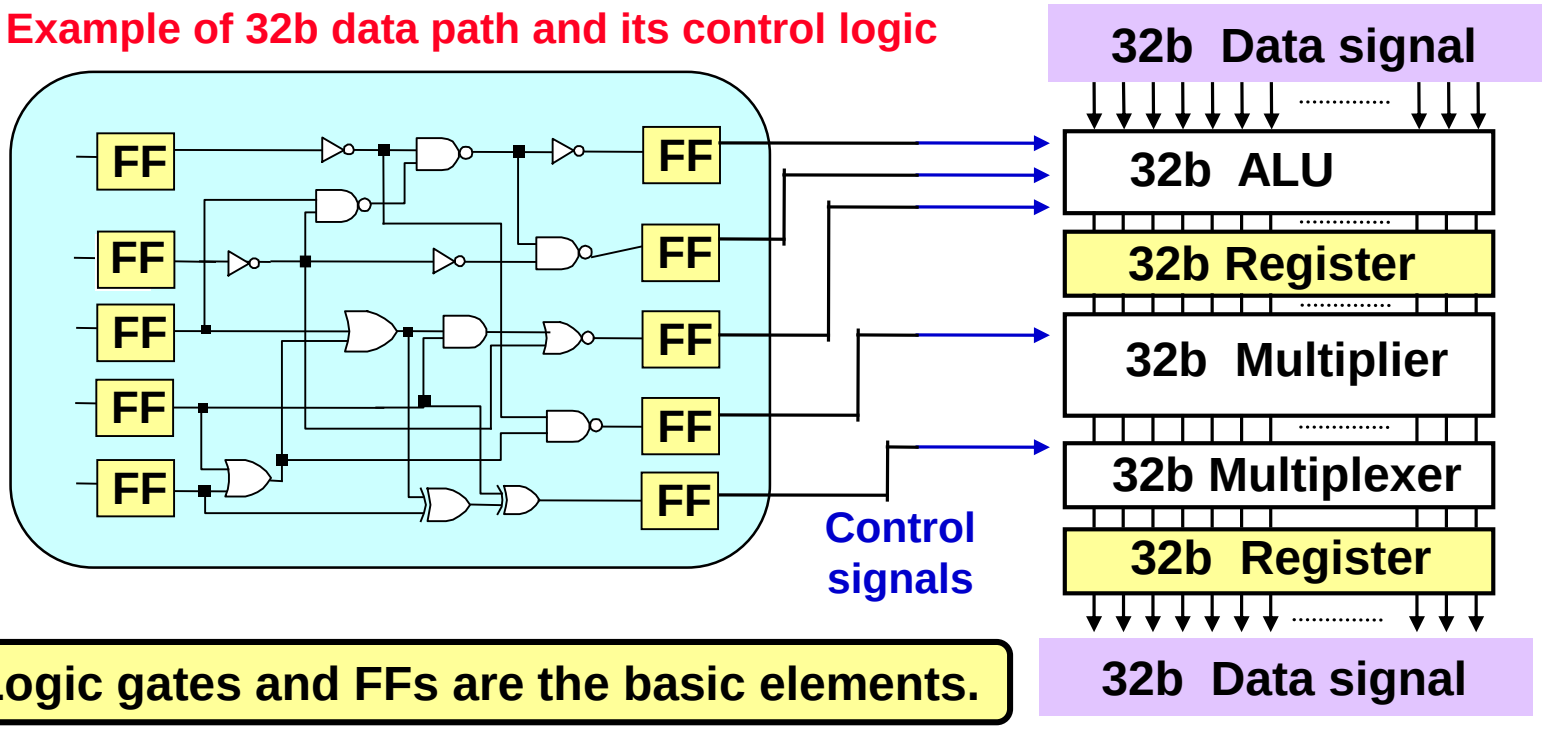
- Control of data path
- Control of whole chip
- Control of interface with external chip

<Data Path>

- Execution units
- Registers, selectors
- multiple-bit width

A register is the data storing circuit.

Example of 32b data path and its control logic

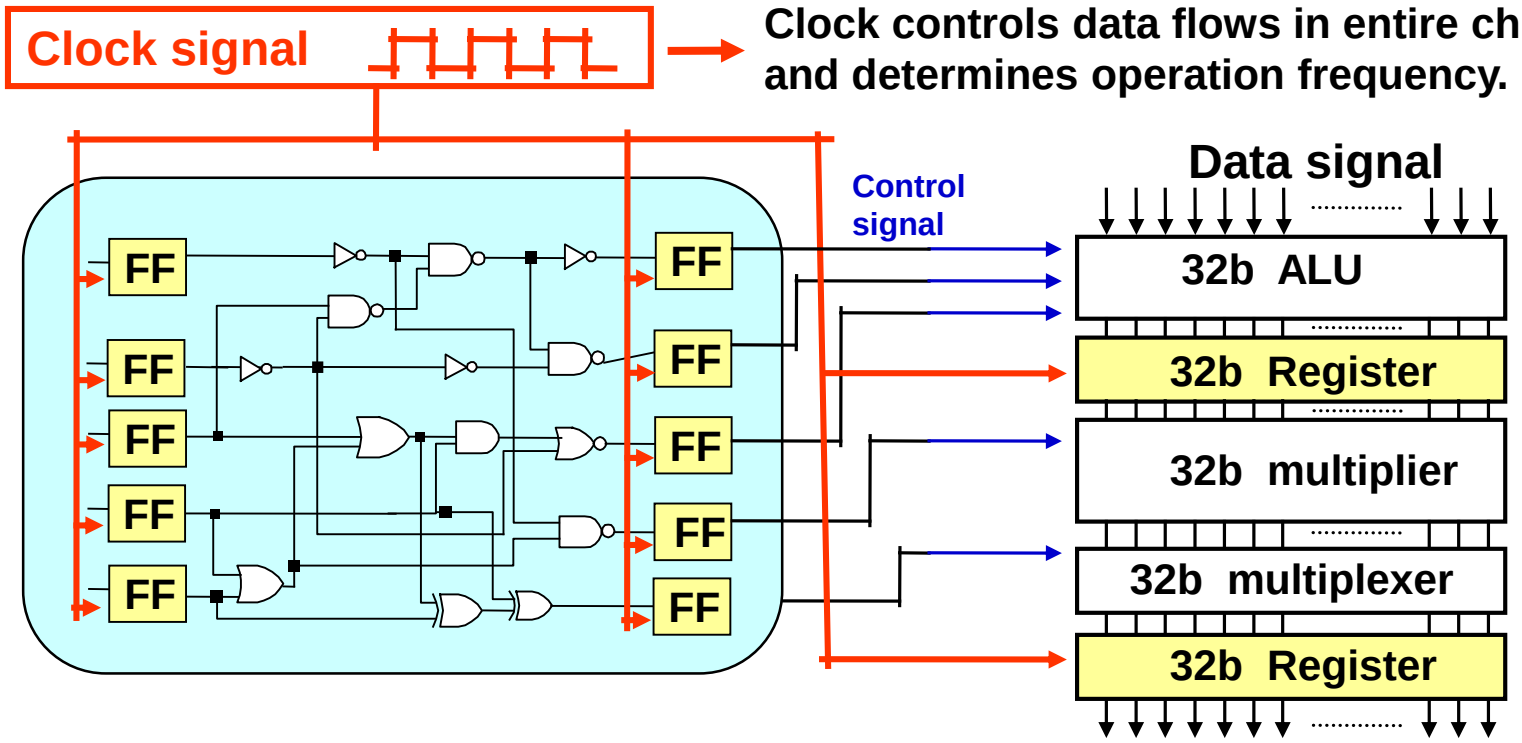


Logic gates and FFs are the basic elements.

Clock Signal

- FFs and registers require clock signal for their operation
- Clock-skew* must be minimized in synchronous design

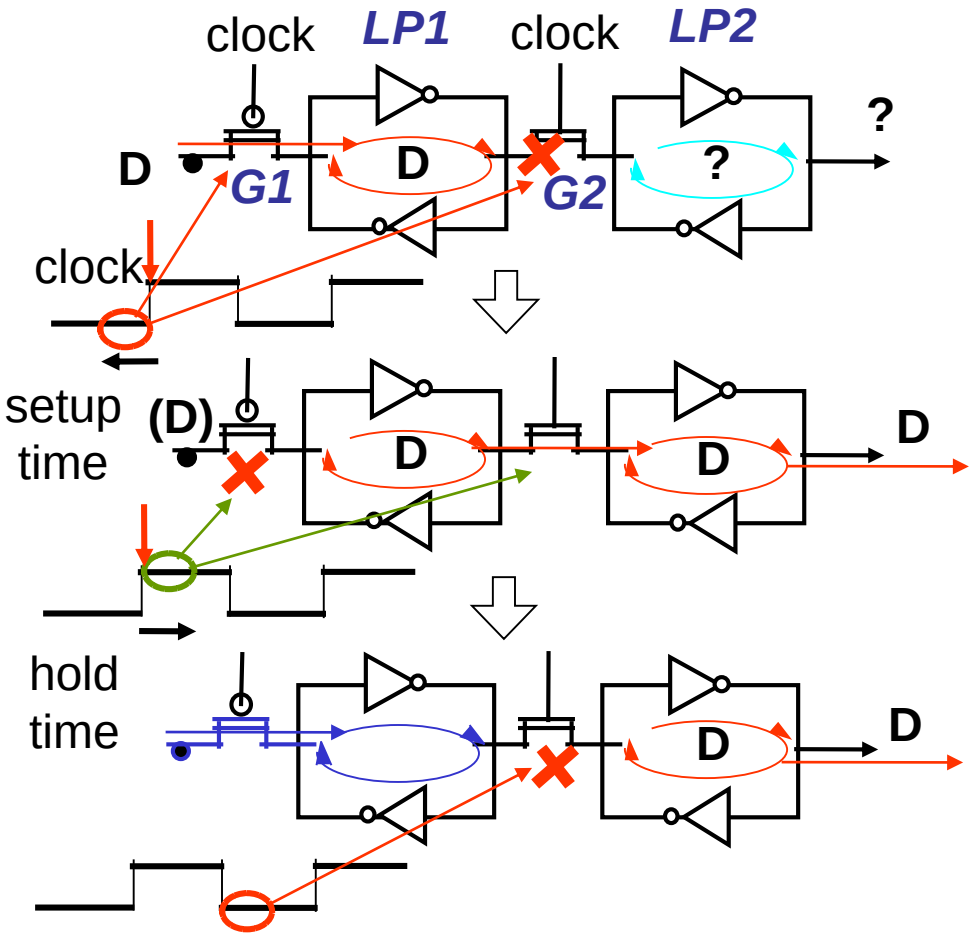
*clock-skew ··· time lag of clock signals among FFs and registers



Routed over entire chip, clock signal is the key factor in determining speed and power consumption

Flip Flops, Again

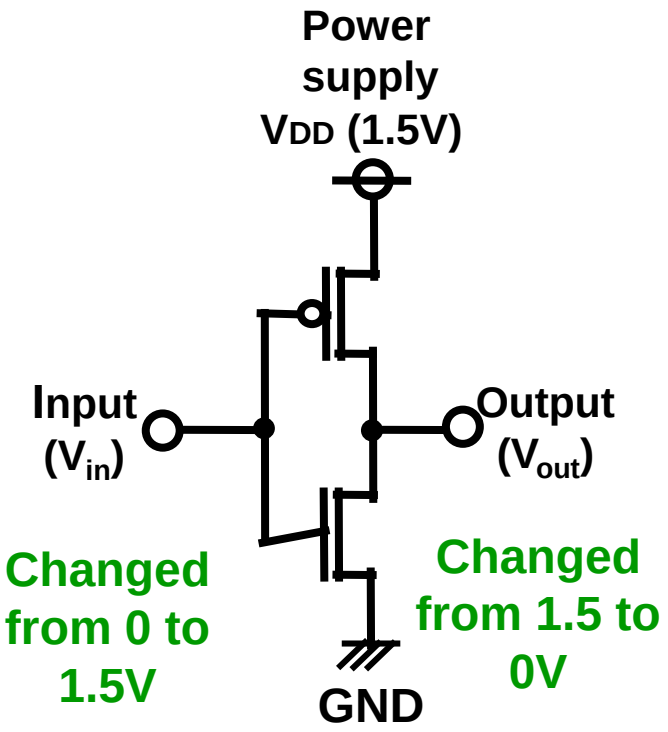
Principle of operation

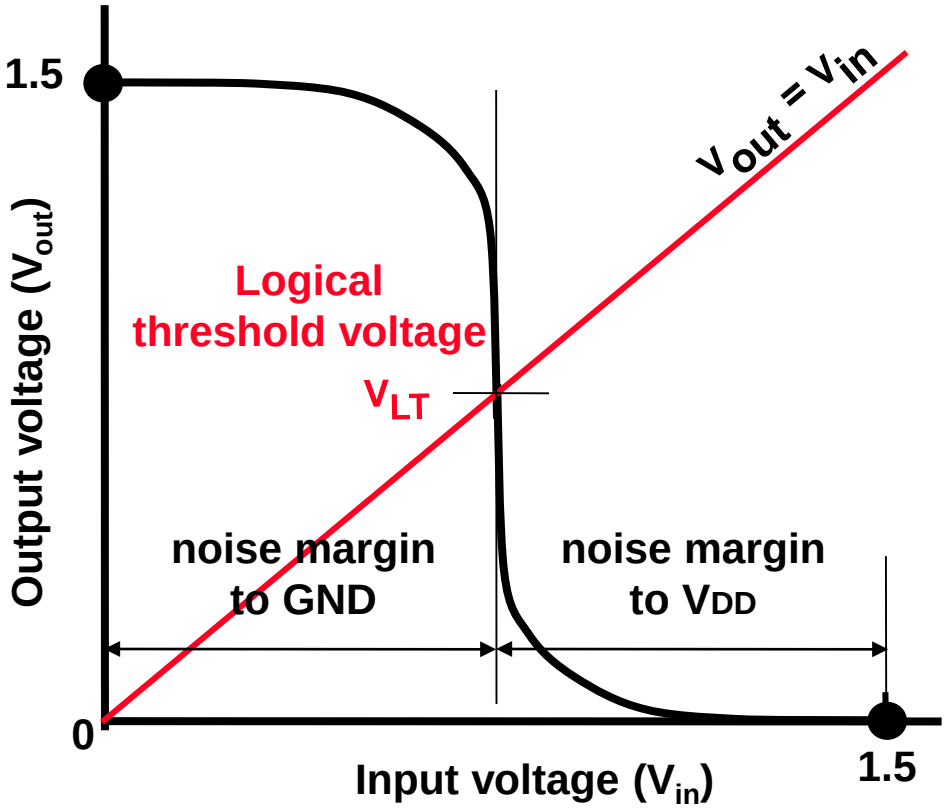


Unavoidable Problem of flip flop

Synchronous design must be adopted.

Logical Threshold Voltage (restudy)



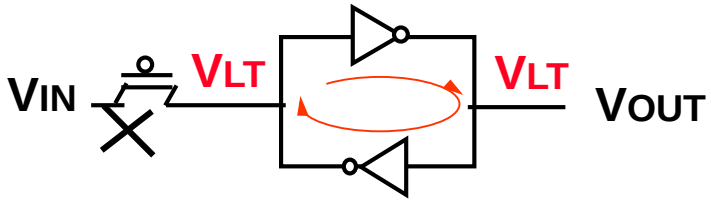


To set logical threshold voltage of each gate at the same level is important to secure noise margin: $V_{LT} = V_{DD}/2$

Metastable State (1)

- To set logical threshold voltage of each GATE at the same level is important to secure noise margin: V_{LT} = 1/2 V_{DD}.

- But big problem in FLIP FLOPs.



- When input V_{IN} is held at V_{LT} and then gate becomes OFF, the flip flop MIGHT may keep this level for unpredictable period.

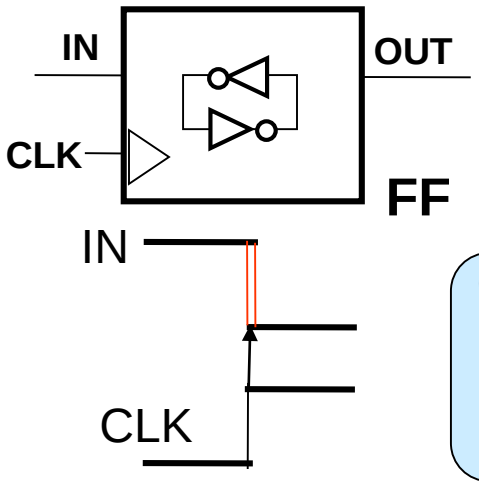
- But actually when small plus noise is applied to left node of loop, V_{OUT} accordingly becomes 0. In minus case, Vout goes to 1.

- Behavior of V_{OUT} is not predictable depending upon noise level: metastable.

< hypothetical case >

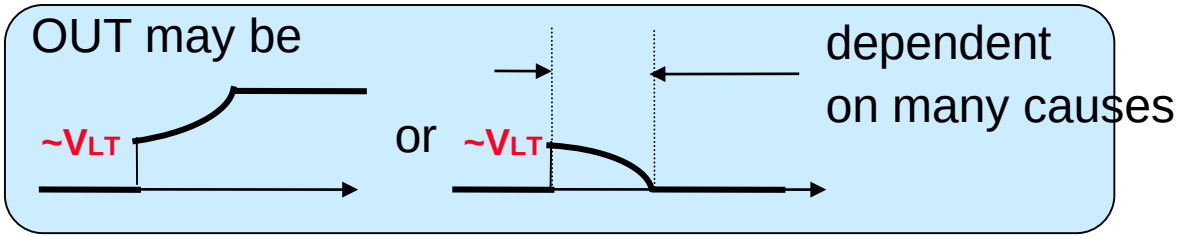
Metastable State (2)

< actual case >



When falling edge of IN and rising edge of CLK are very close, voltages at inverter loop within FF become close to V_{LT} depending on timing of IN.

Succeeding behavior is unpredictable.

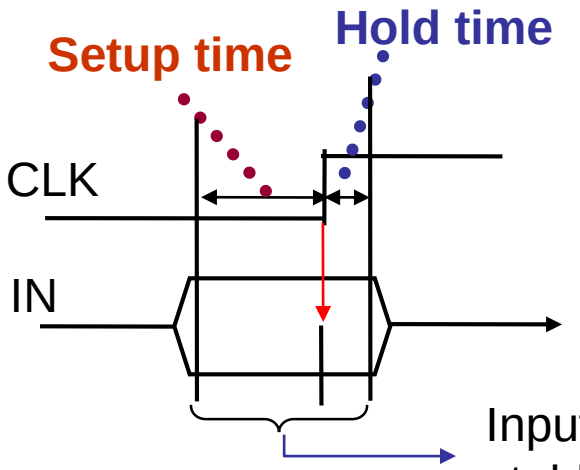


This phenomenon surely happens when IN is asynchronous with CLK. OUT must be sensed at least one clock cycle after CLK rising edge under focusing.

Asynchronous input must be clocked twice to wait for settlement of metastable behavior.

Asynchronous data transfer may cause one of the most serious logic design bugs that need long time to be fixed because failure is intermittent.

Synchronous Design

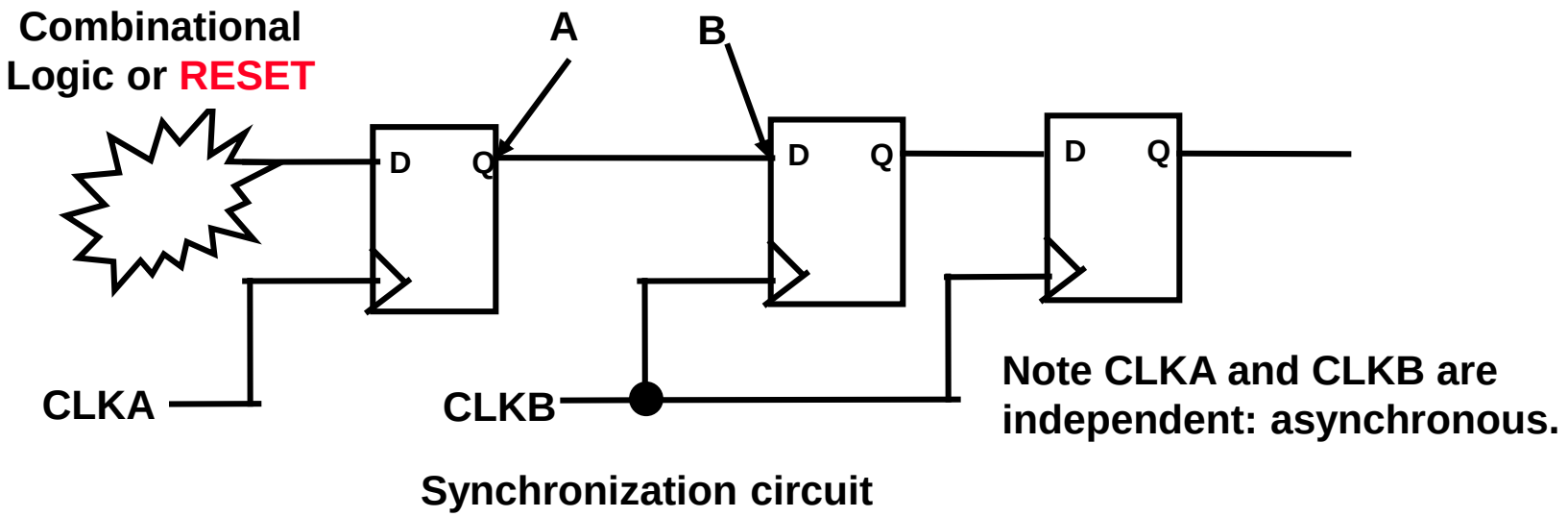


Input stable during setup/hold time can prevent metastable behavior.

To observe setup/hold time is the key in synchronous design.

Note : setup/hold time is different from “delay”. Be sure to thoroughly verify it with STA.

Asynchronous Input



Synchronization circuit

Designers common knowledge : asynchronous input must be clocked twice to wait for settlement of metastable state

Pitfalls = Error :

- **overlook that CLKA and CLKB are independent**
- **nodes A and B are not 1-to-1 connection**
- **$f_{CLKA} > f_{CLKB}$**

Summary for Logic Circuits (1)

- Inverter, a fundamental logic circuit, is comprised of a pair of nMOS and pMOS transistors, where both gates are commonly connected to input, and both drains to output.
- Output voltage swings from GND to V_{DD}, and no direct current flows from V_{DD} to GND.
- Logical threshold voltage: $V_{LT}=V_{IN}=V_{OUT}$ ➔ $V_{DD}/2$
- Delay time: $$Td = \frac{CL \cdot V_{DD}}{\beta \cdot (V_{DD}-Vth)^2}$$
- Power consumption :P = Pdynamic + Psc + Pleak,
  $$Pdynamic = \alpha * f * \Sigma C_L * V_{DD}^2$$
- Based on inverter structure, any functional gate can be configured in complementary way by applying duality rules.
- Standard logic block is composed of combinational logic sandwitched by 2 rows of FFs.

Summary for Logic Circuits (2)

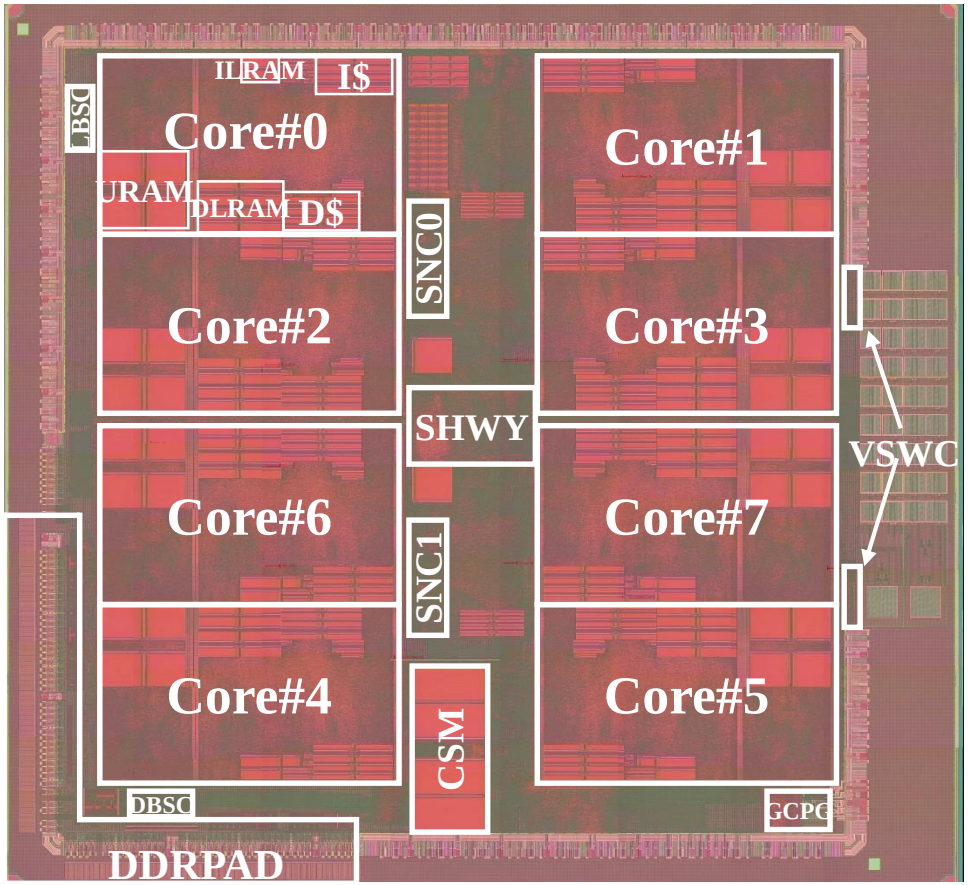
- Typical logic LSI designs include logic blocks, and datapath controlled by some of logic blocks.
- Clock signal must be carefully considered in terms of timing designs and routing because it is routed to every flip flop and register.
- Metastable behavior is inherent in FF. To avoid this, synchronous design is straightforward as far as setup/hold time is appropriately observed.
- Asynchronous data transfer must be carefully designed.

References

- Circuit Design for CMOS VLSI by John P. Uyemura,1992
- Application-Specific Integrated Circuits
  by Michael John Sebastian Smith, 1997
- Digital Integrated Circuits A Design Perspective by Jan M. Rabaey,1996

Appendix

LSI Example 1 (processor chip)

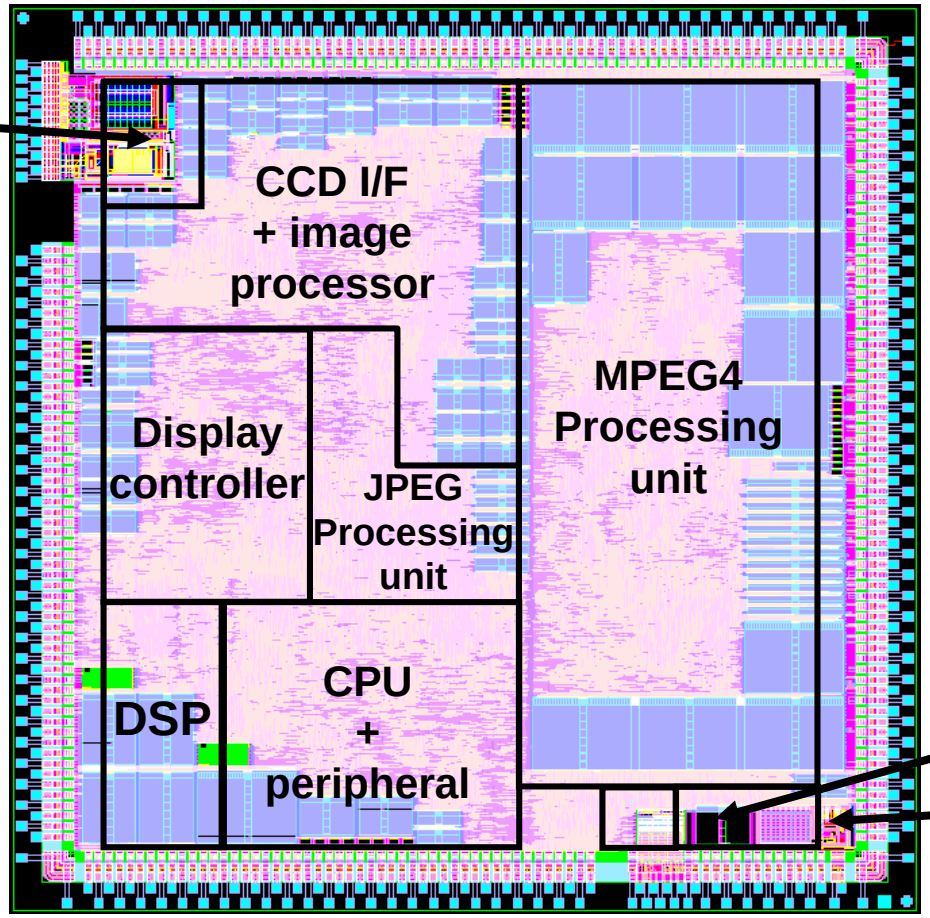


Process Technology	90nm, 8-layer, triple-Vth, CMOS
Chip Size	104.8mm^2 (10.61mm x 9.88mm)
CPU Core Size	6.6mm^2 (3.36mm x 1.96mm)
Supply Voltage	1.0V–1.4V (internal), 1.8/3.3V (I/O)
Power Domains	17 (8 CPUs, 8 URAMs, common)

LSI: Large Scale Integration

LSI Example 2 (SoC)

< Layout plot of SoC chip for Digital Still Camera (DSC)>



SoC: System on Chip

CCD: Charge Coupled Device

DSP: Digital Signal Processor

JPEG: Joint Photographic Experts Group

MPEG: Moving Picture Experts Group

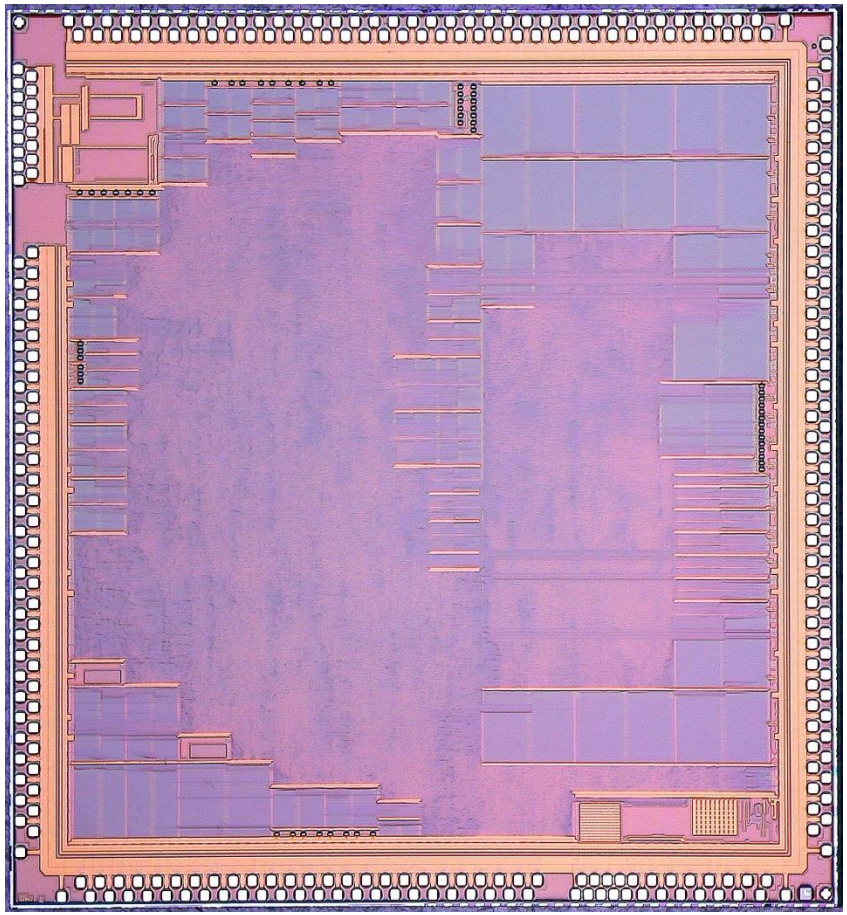
USB: Universal Serial Bus

PLL: Phase Locked Loop

Wide variety of functional units are integrated on a single chip to configure an SoC

Die Photo and Outline of SoC for DSC

<Die photo>



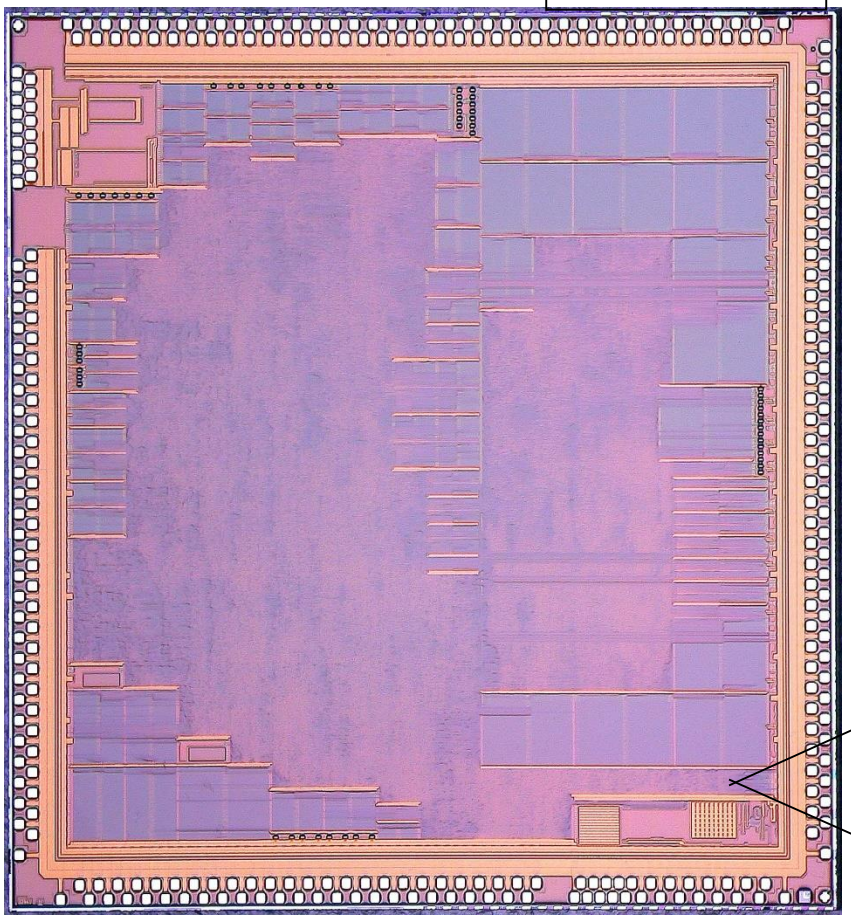
<Chip summary>

Number of logic gates	2.5M gates (1 gate =4 trs.)
SRAM	equipped with 90 pcs, totally 3M bits
ROM	equipped with 3 pcs of 64K- bit block
Analog	PLL, ADC, DAC, USB
Process	0.15μm, 5-layer metal
Chip size	7.85 x 7.85 mm^2

Physical Dimensions

um: 10^{-6} m
nm: 10^{-9} m

<Die photo>

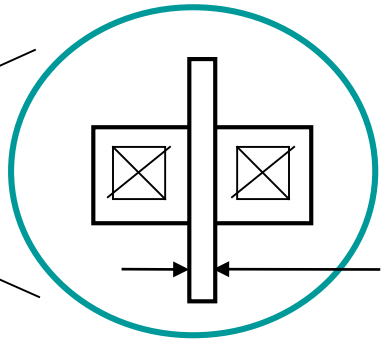


~11 um — **fine silk**

2,000~100,000 nm (naked eye) — **mold** **(spore)**

500~3,000 nm (microscope) — **bacteria**

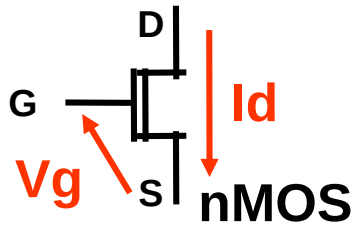
10~400 nm (elec. microscope) — **virus**



MOS transistor

channel length:
100~150 nm

Exercise 1



Linear region $(0 \leqq Vd \leqq Vg-Vth)$

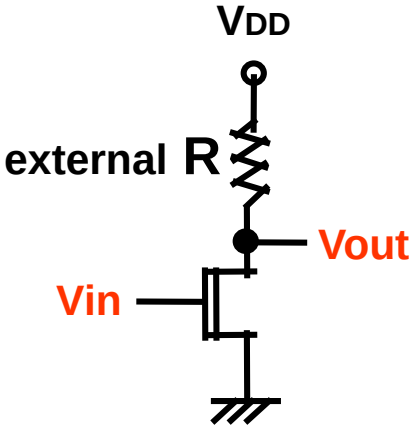
$$Id = \frac{W}{L} \mu Cox \left\{(Vg-Vth)Vd - \frac{1}{2}Vd^2\right\}$$

Saturation region $(Vd > Vg-Vth)$

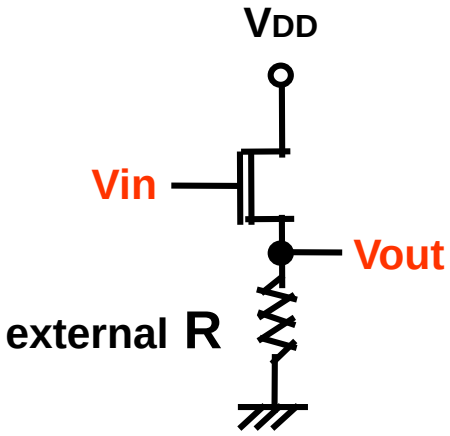
$$Id = \frac{W}{2L} \mu Cox (Vg-Vth)^2$$

$\alpha = \mu CoxW/2L$

Vin is connected to Vdd, and R becomes infinity, then Vout =?

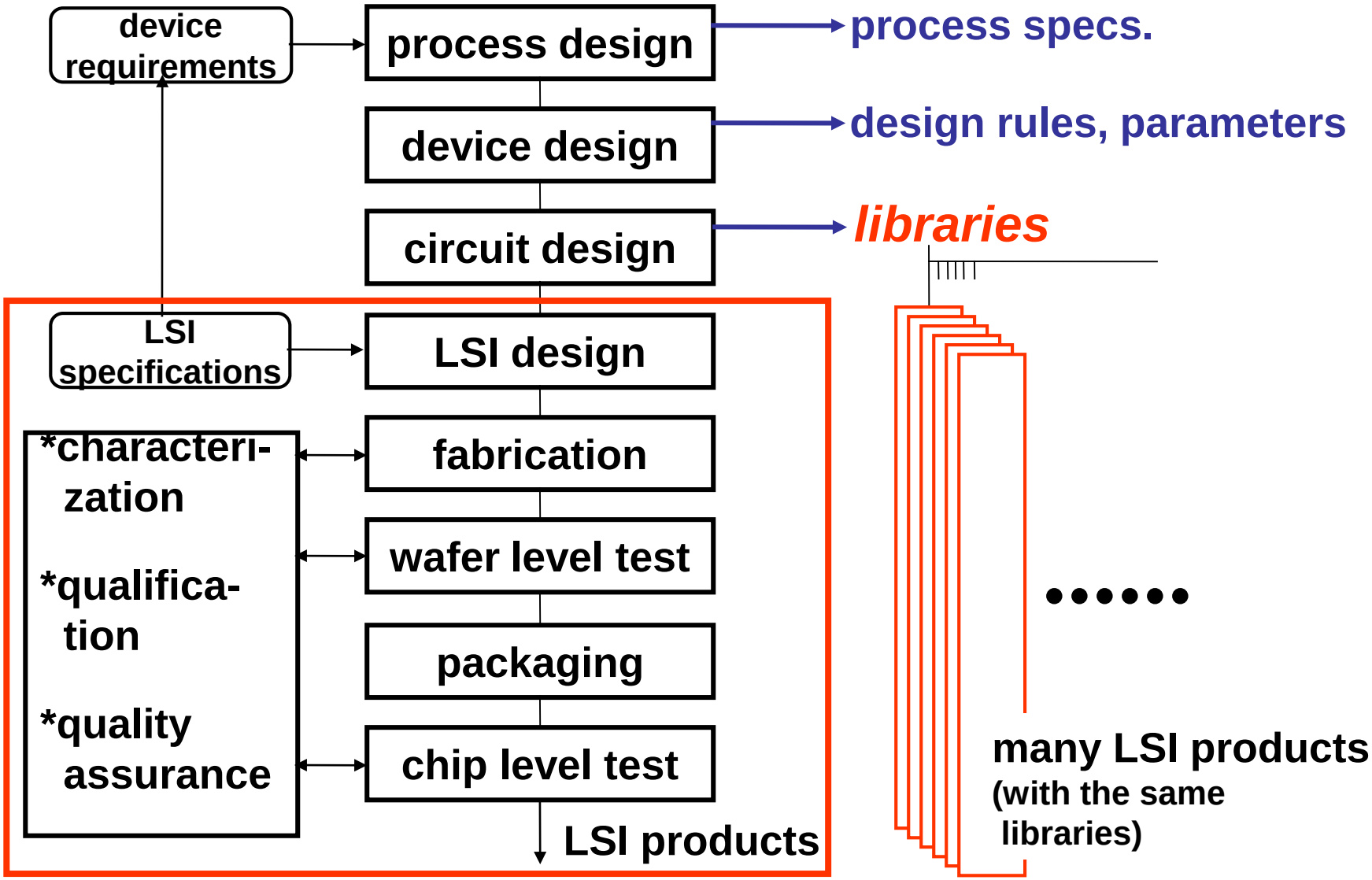


Vout =

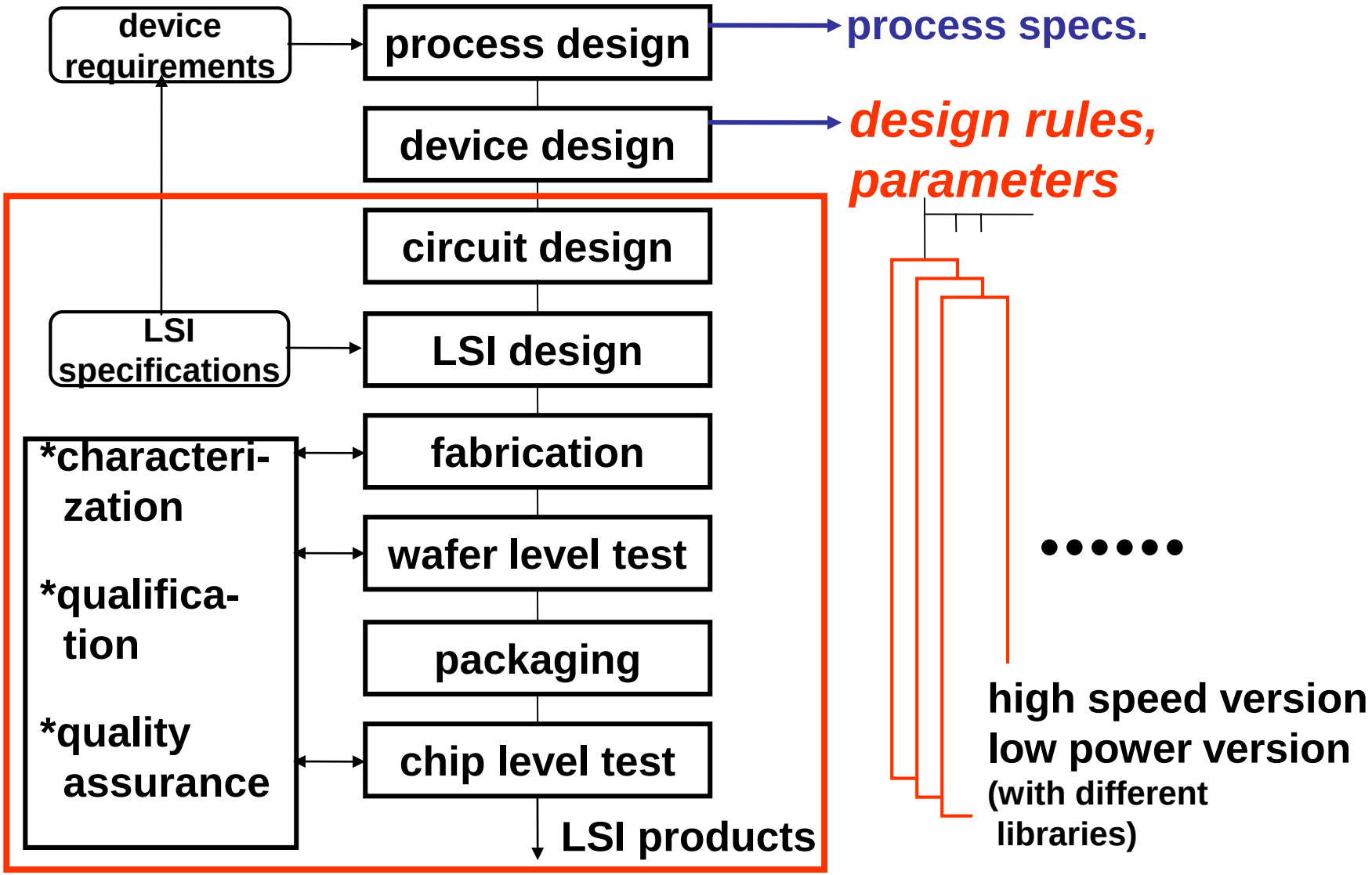


Vout =

Diversifications (1)



Diversifications (2)



Calculation of MOS capacitance

Capacitance C is a capability to store charges.

$$C = \varepsilon \times \varepsilon_0 \times S / t$$

C : Capacitance (Cox)
S : Area of capacitor
t : Thickness of insulator
ε : Relative permittivity of insulator(3.9 for SiO_2)
ε_0 : Permittivity of vacuum (8.84×10^{-14} F/cm)

The amount of charge to be stored is determined by the product of C and Voltage.

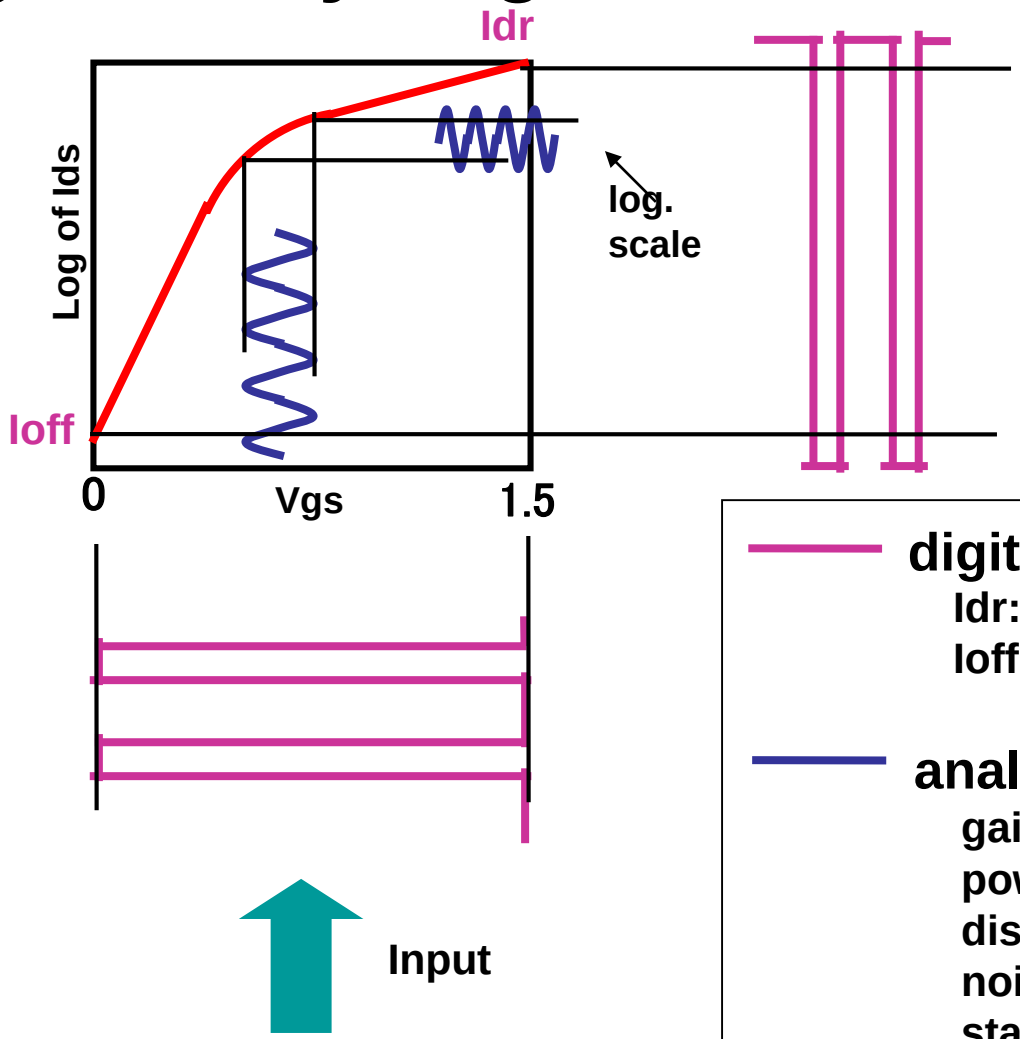
$$Q = C \times V$$

Q : Stored charge
V : Applied voltage

Example The capacitance of MOS capacitor(P-substrate) whose area is 2.5×10^{-3} (cm^2) with applying voltage of - 3.0V is 884 (pF). Calculate the gate thickness.

$$Tox = \frac{8.84\times10^{-14} \times 3.9 \times 2.5\times10^{-3}}{884\times10^{-12}} = 9.75\times10^{-7}\ cm = 9.75nm$$

By the way, Digital vs. Analog



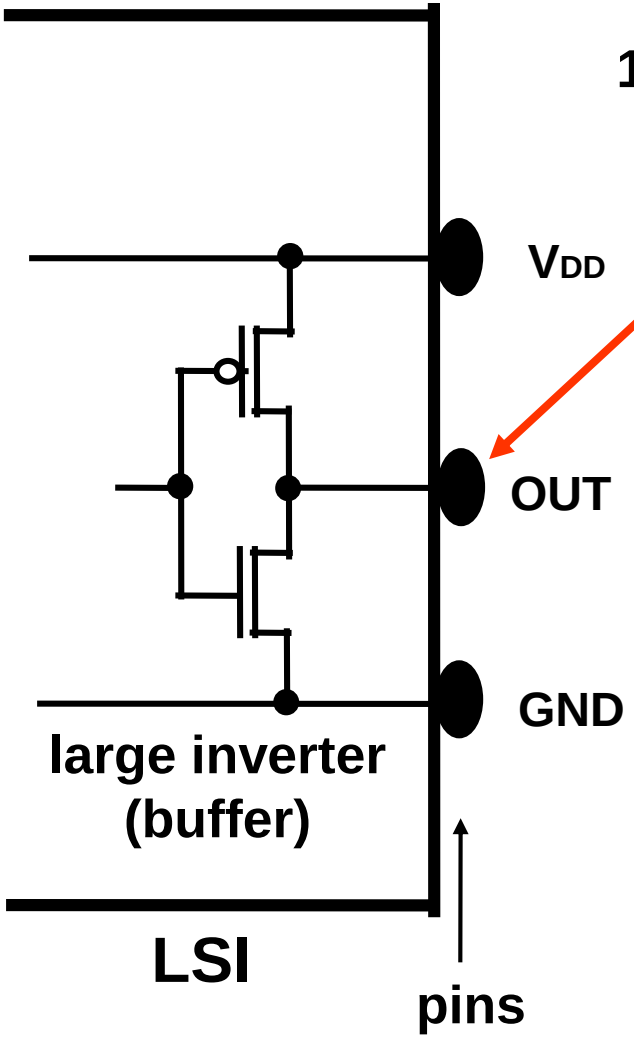
digital

- Idr: speed and power
- Ioff: standby power

analog

- gain
- power dissipation
- distortion, linearity
- noise immunity
- stability
- pair matching

What is Latch Up



1. Large noise (>VDD) or negative noise (<0)

2. Then, large current keeps flowing from VDD to GND due to parasitic bipolar transistors

3. Malfunction will occur.

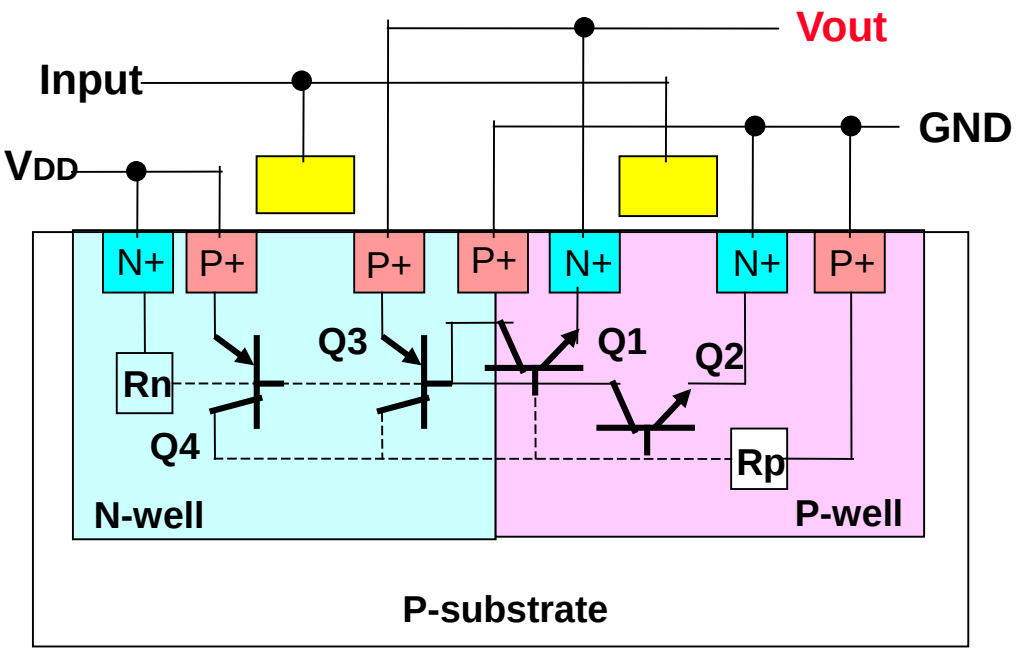
4. Finally, power lines in LSI may melt down due to high current.

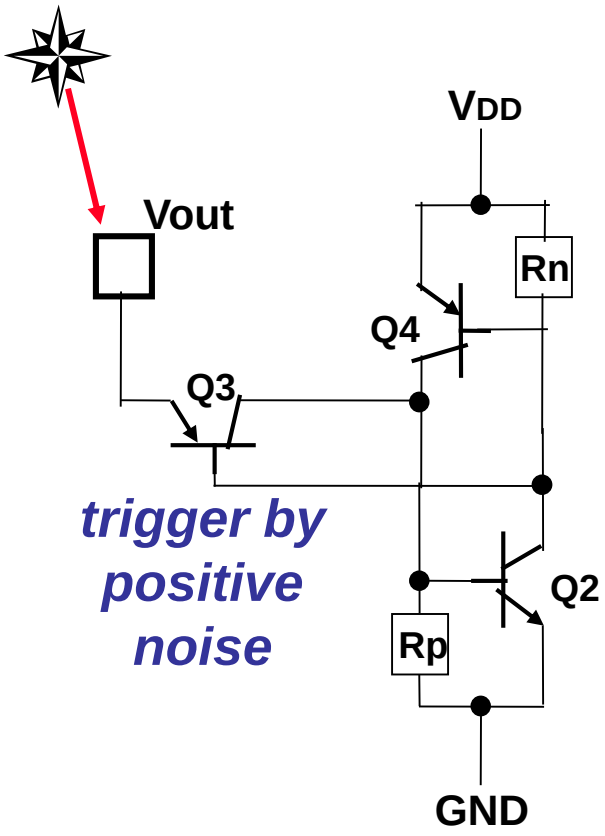
BD002

Latch up, a worrying problem

- Reason: positive feedback loop including parasitic bipolar transistors in CMOS
- Cause: noise spike or improper circuit hookup.
- Conditions: depending on bipolar transistors gain and resistivity of n-wells and p-wells (dimension dependent).
- Once the latch up occurs, the only way to stop it is to reduce the current below a critical level, or usually to shut down the power source.
- With process advancement (finer, thinner, closer), the latch up becomes serious.

What is Latch Up





trigger by positive noise

pMOS FET transistors

lateral bipolar transistors (pnp)

nMOS FET transistors

lateral bipolar transistors (npn)

positive feedback loop

Latchup Sequence

- Excessive surge voltage is applied to Vout.
- Base and Emitter of Q3 is forward biased ($|V_{BE}|$>0.6V), and surge current flows to V_{DD} through Rn.
- Q3 becomes ON, and collector current flows to GND through Rp.
- Voltage across Rp exceeds 0.6V, and emitter and base of Q2 is forward biased ($|V_{BE}|$ >0.6V).
- Q2 becomes ON, and collector current flows from V_{DD} through Rn.
- Voltage across Rn exceeds 0.6V, and emitter and base of Q4 is forward biased ($|V_{BE}|$ >0.6V).
- Q4 becomes ON, and collector current flows to GND through Rp.

- Go to (4), where V_{BE} >>0.6V. Then, (5), (6), (7), (8), (5), (6)…..

➔ melt down

Characteristics of leakage currents

(supplement)

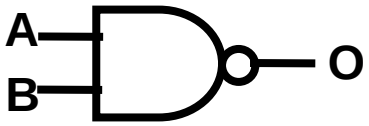
	Voltage dependency	Temperature dependency	Application of substrate bias(Reverse)
Sub-threshold leak	small	large	decrease
Gate leak	large	small	non
Junction leak	large	small	increase

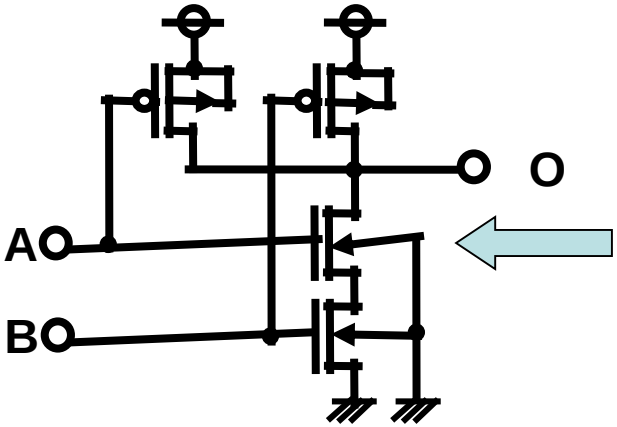
- The component of leakage varies depending on junction temperature.
- Can be reduced by controlling power supply voltage and substrate bias.

Substrate Node of Logic Gate

Examples of logic gates

- 2 input NAND ($O=\overline{A \cdot B}$)

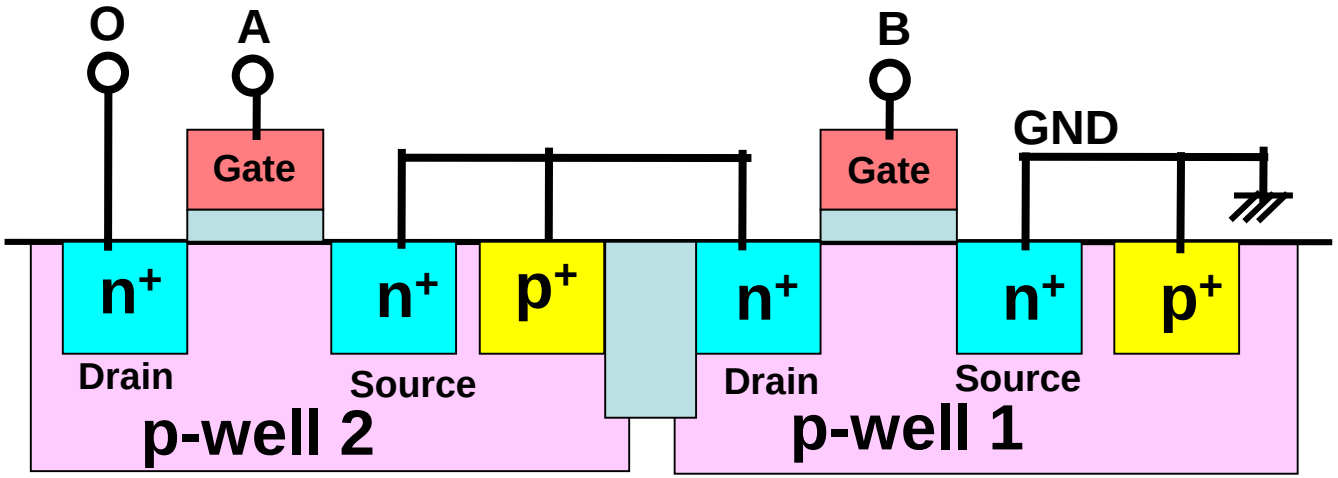




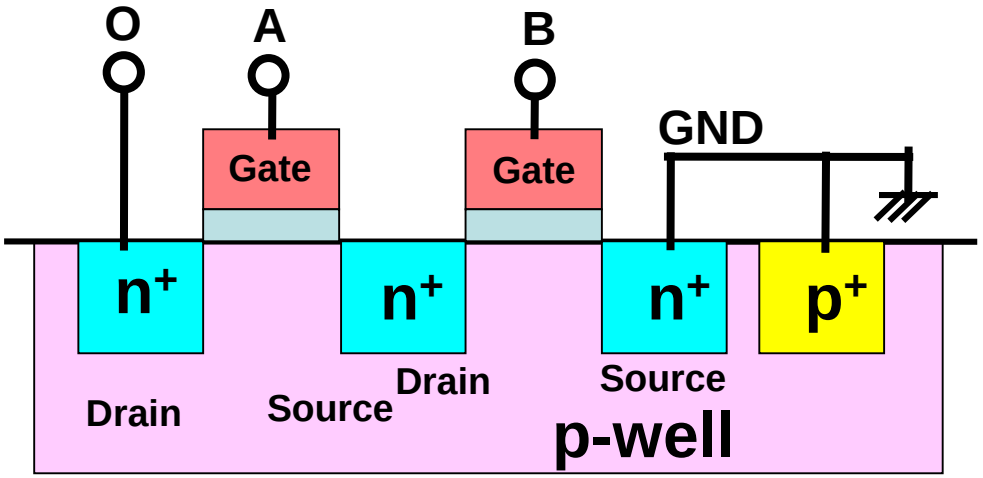
Vthn of this transistor is increased because Vbs becomes negative in some cases: **body effect**.
To prevent body effect of this transistor, its WELL might be isolated from that of lower transistor, which makes cell layout area irresistibly larger.
➔ **WELL is commonly formed in typical designs**.

Device Isolation

<Isolated Well>



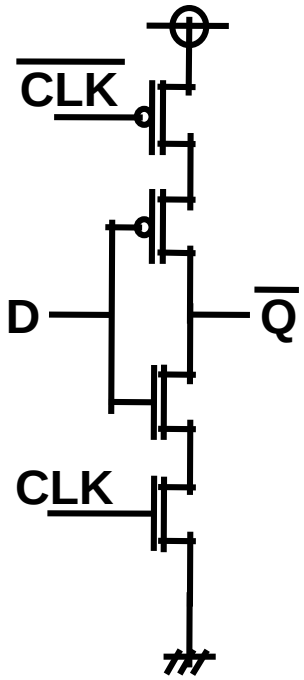
<Common Well>



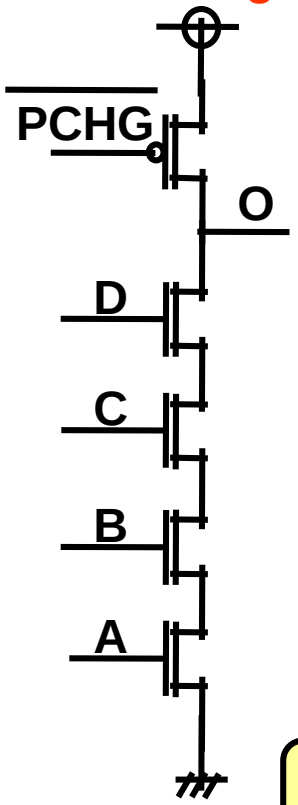
Tricky Circuits

Less transistor counts, but more traps

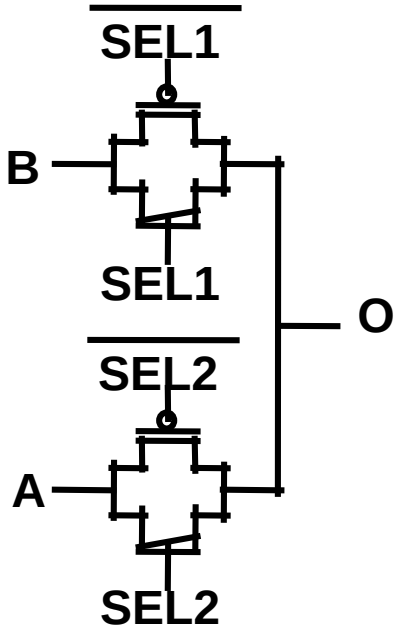
clocked gate (dynamic latch)



dynamic 4-NAND gate



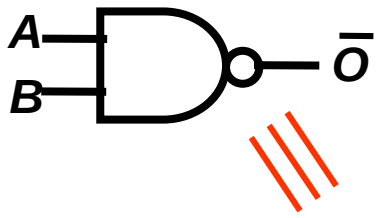
multiplexer (selector)



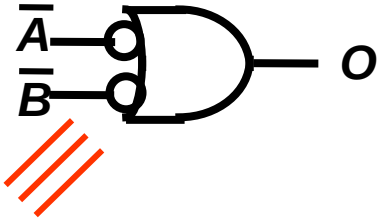
Extensive review is a MUST!

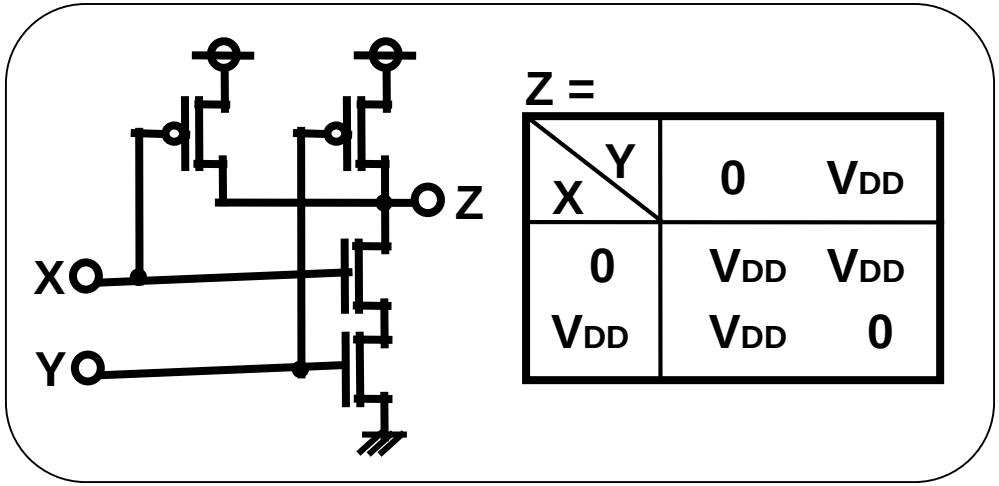
Polarity

○ 2 input NAND ($\overline{O}$=A･B)



○ 2 input OR (O=$\overline{A}$+$\overline{B}$)



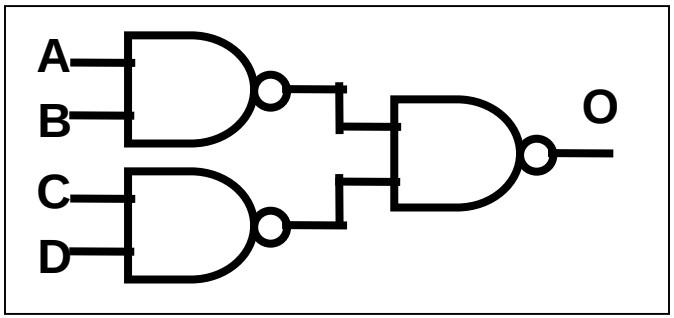


Z =

X \ Y	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	V_{DD}	0

◆ NAND gate acts as NAND or OR depending upon input polarity.
- positive logic: “0” = 0V, “1” = V_{DD}
- negative logic: “0” = V_{DD}, “1” = 0V

Exercise 3



Rewrite symbols

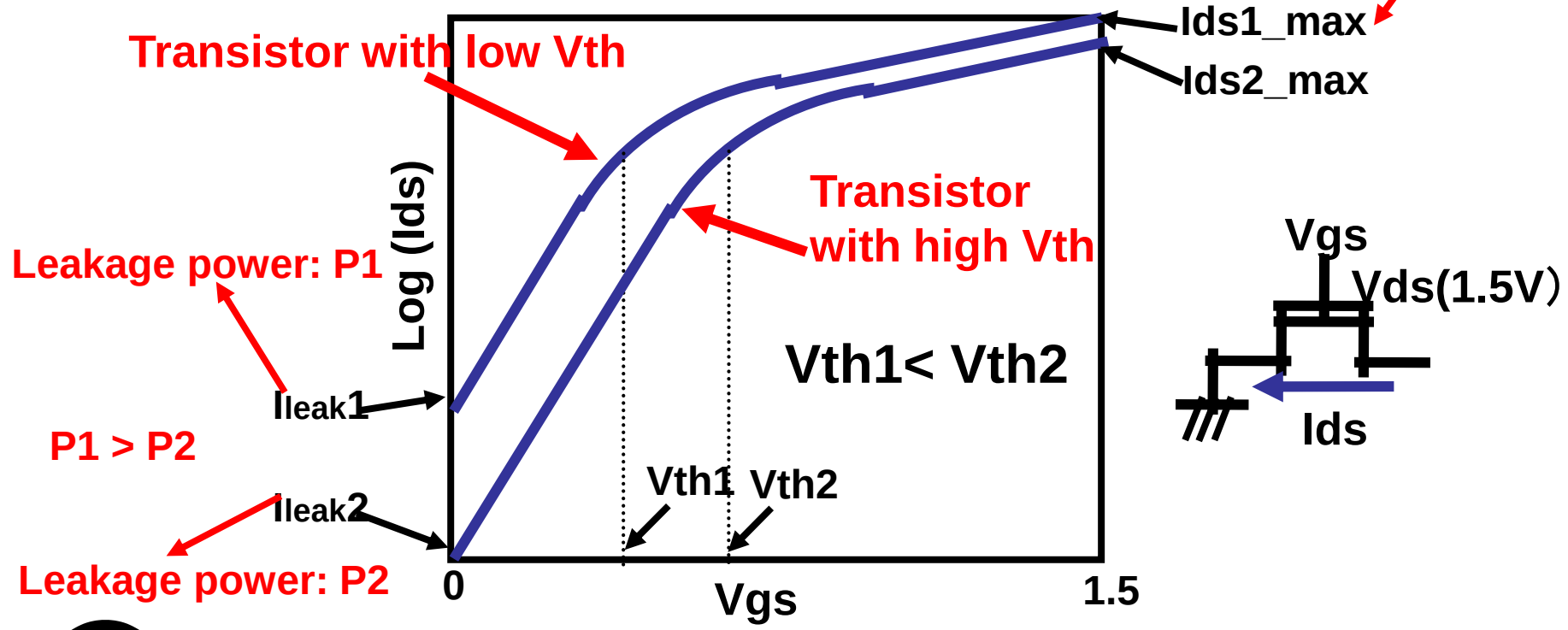
Simplify symbols

Actual simplified circuit

Relationship between threshold voltage and drain current (2)

Transistor Speed

< Different transistor characteristics according to different Vth>



- Vth can be tuned during fabrication by ion implantation.
- Transistor with lower Vth is ….?

What is the relation between Ids and speed of CMOS ?

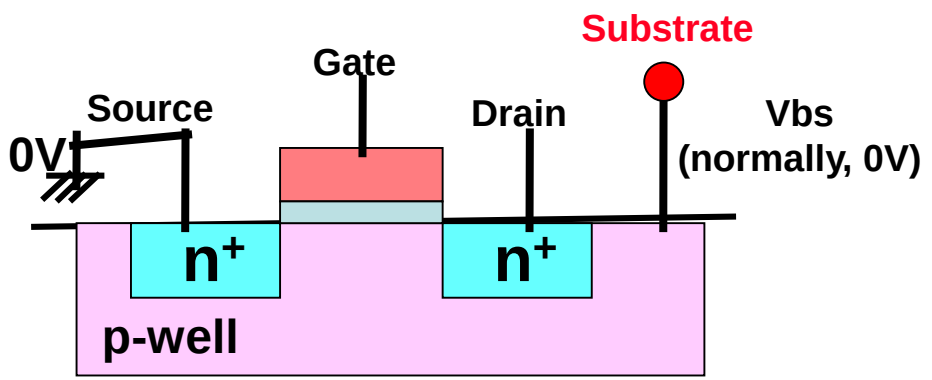
Please refer to slide: Propagation delay time
-The Load Capacitance at the output of CMOS Inverter always exists.
This capacitance consists of stray capacitance of wiring, junction
capacitance at drains, gate capacitance of succeeding circuit.
-Due to Load Capacitance, output of CMOS Inverter can NOT change immediately whenever input changes. It make a delay time at the output (as you saw in slide : Delay time)
=> This delay time = time for charging/discharging the load capacitors, and it depends on charged/discharged current Ids.

If Ids is large,charging/discharging time is small=>delay time is small.
If Ids is small,charging/discharging time is large=>delay time is large.

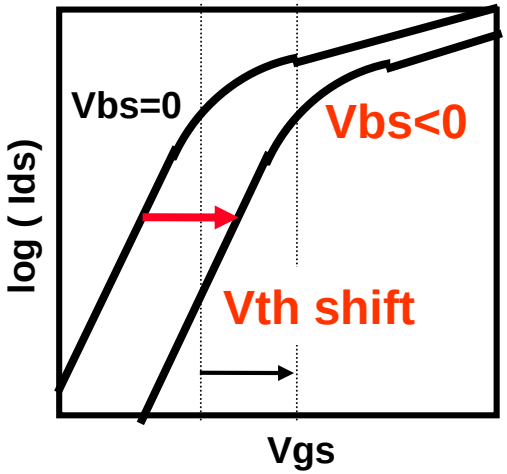
"Speed of a circuit" is related to response time of circuit.
If delay time is smaller, the circuit is faster
If delay time is larger, the circuit is slower

Substrate Node Potential

○Electrical potential of substrate (formed by WELL structure) as 4th electrode also affects transistor characteristics.



<nMOS transistor>



< threshold voltage dependency on substrate voltage >

$$Vth = Vt0 + k(\sqrt{-Vbs + 2\phi} - \sqrt{2\phi})$$

Vt0, k, ϕ: constants

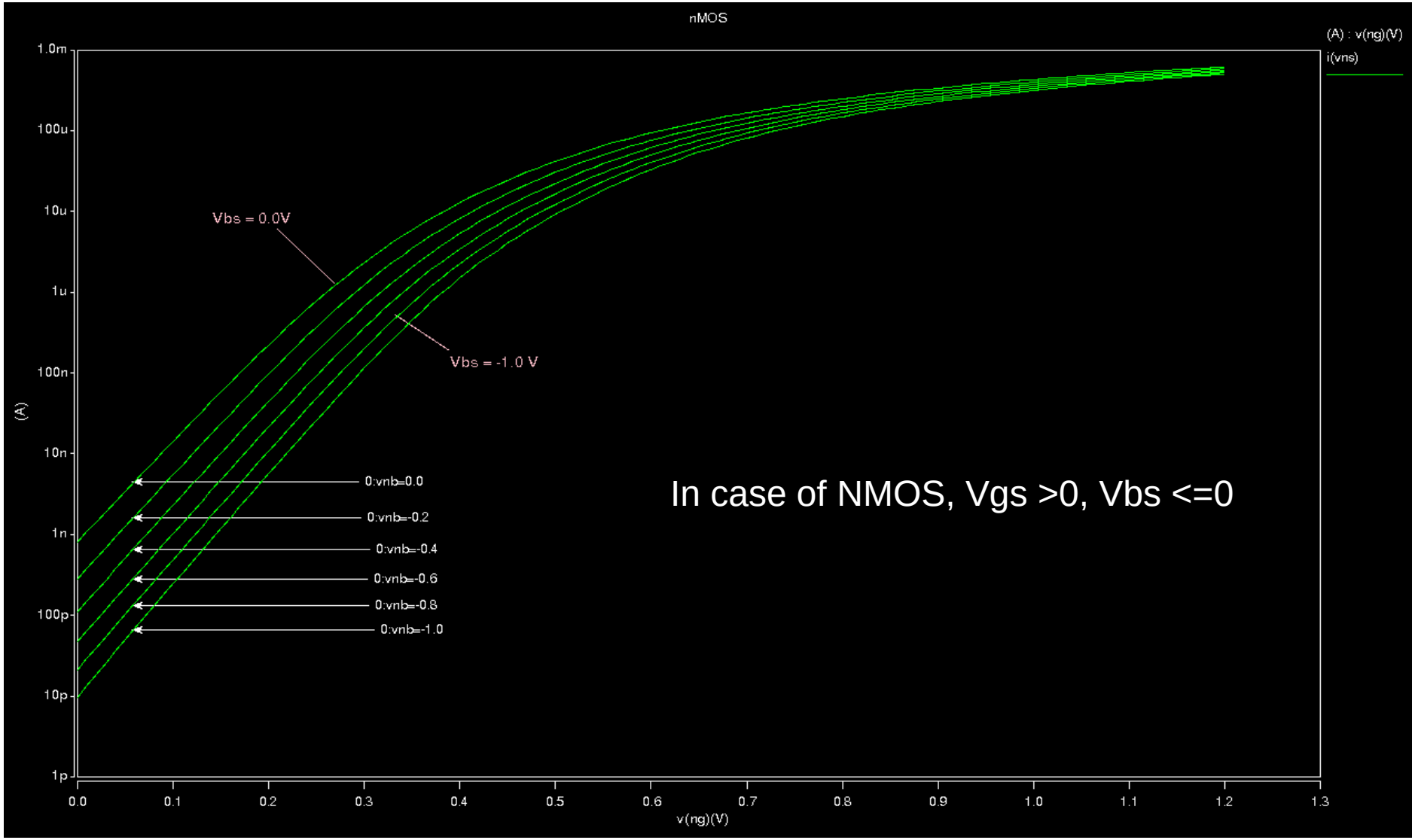
BD002

Body Effect

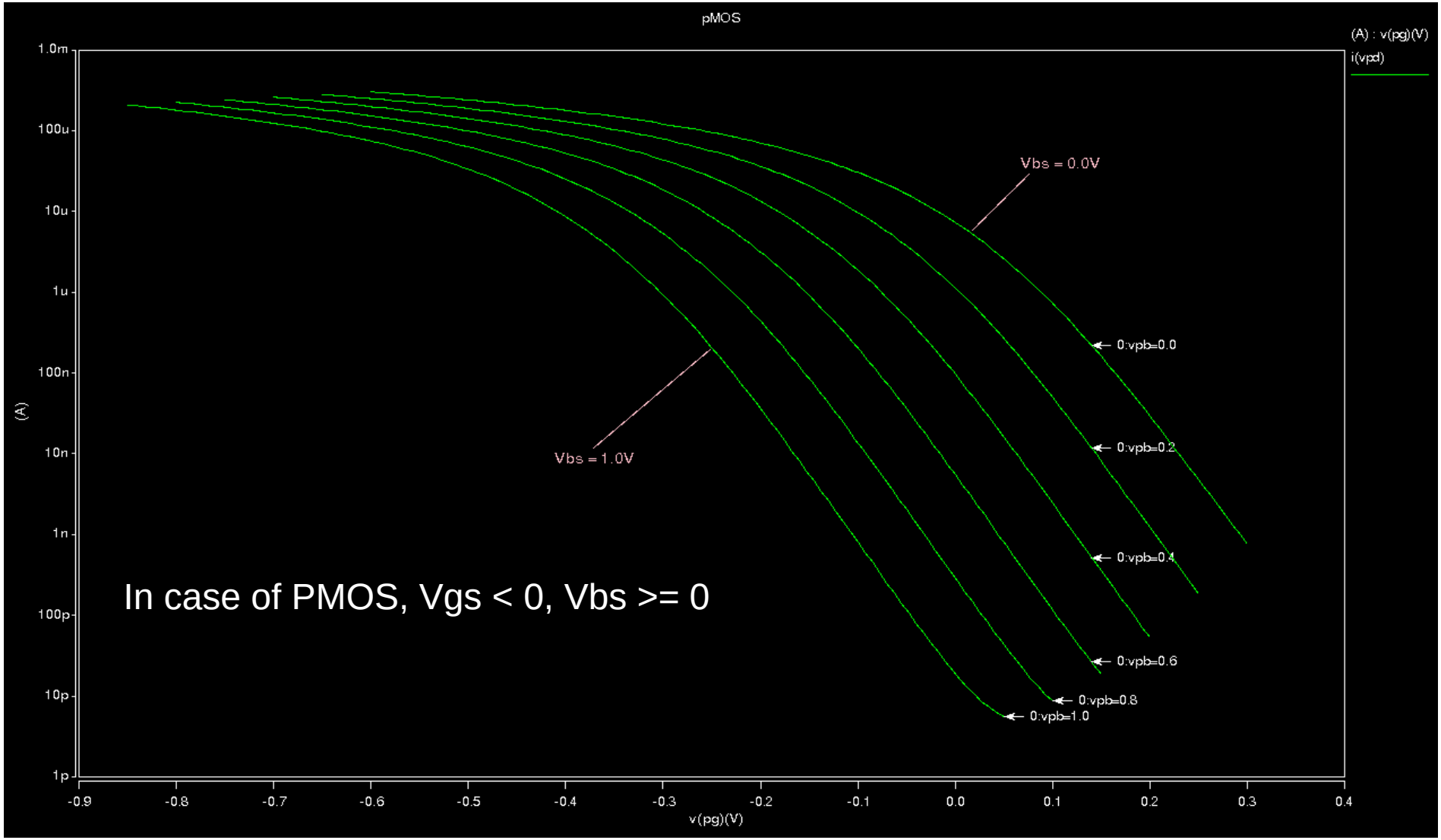
<nMOS>
* Vbs <<0, then …?
* speed, leakage…?

<pMOS>
* Vbs >>0, then …?
* speed, leakage…?

Substrate Node Potential - NMOS



Substrate Node Potential - PMOS



Renesas Electronics Corporation