Teo **Tsiakiris**

Physicist | Engineer

About me

FPGA engineer with passion for developing hardware solutions for real-world applications. My professional experience includes impactful collaborations with prestigious institutions as well as the private sector. I have had the honor of learning from professionals with diverse backgrounds (Software, Firmware, Physics) and ethnicities. Electronics and embedded systems enthusiast. Eager to work and learn from the best.

Contact

Born on 22/12/1993, Age 30

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theodoros-tsiakiris

Soft Skills and Strengths

Conflict resolution | Resourceful | Communication | Organizational | Curiosity | Patience | Team Working | Persistence | Problem Solving | Empathy | Attention to Detail | Self-motivation | Brainstorming | Active Listener | Out of the box thinking

Professional Skills

VHDL | Vunit | Modelsim | Vivado | Active HDL | Analog Circuit design | CI/CD | Git | Docker | JIRA | Cadence Virtuoso

Languages

English - Professional working Proficiency

German - Elementary Proficiency

French - Elementary Proficiency

Greek - Native Proficiency

WORK EXPERIENCE

2023-Today — **Digital Design Engineer** — Dresden, Germany
Last Mile Semiconductors
- Working from the ground up on the state-of-the-art NR+ communications protocol for IoT.
- Study of specifications of the protocol, design (SystemVerilog) and Verification (cocotb) of hdl modules designed for the Physical layer. Writing documentation (Confluence) and contributing to the in-house library (python and hdl modules)
- Working with icglue, an open source tool for register and hdl code generation.
- Writing documentation for the designed IPs

2022-2023 — **CERN Technical student** — Geneva, Switzerland
CERN
- Porting various of the section's IPs from Wishbone to AXI-Lite interface using Cheby register generation tool and testing the VHDL code with VHDL testbenches (Vunit framework).
- Implementation of these IPs in hardware and testing their functionality with Vivado on an AC701 evaluation board.
- Open sourcing IPs of the section and packaging them for a wider audience. Contributing to CERN's general cores, part of open hardware .
- Experience with git CI/CD, Docker images, JIRA project tracking and Git versioning tools

2021-2022 — **Hipeac Intern** — Livorno, Italy
Campera-ES
- Designing and simulation of a system for DFT processing of real-time images for space applications. Conferring regularly with project coordinators and third-party individuals (Xilinx ZCU106 evaluation board).
- Designing a waveform generator for RADAR applications (AMD Kintex Ultrascale).

2021-2021 — **Student - FPGA Designer** — Thessaloniki, Greece
CERN ATLAS-Aristotle University
- Design of I2C, SMbus and PMbus for temperature, voltage, and current regulation with an LT3884 DC-DC converter.

EDUCATION

2019-2023 — **Master Degree** — Thessaloniki, Greece
Aristotle University of Thessaloniki
Electronic circuit technology
A two-year intensive curriculum in the country's second-oldest Masters program.

Embedded Systems: - Server-client configuration for temperature and humidity measurement. (TCP, python, C, Rasberry Pi, atmega2560, atmega328p)

Digital Systems: - UART and I2C on a Zybo Z7-Z10 board.

Integrated circuit design
Degree: 9.60/10

2019 — **Bachelor of Science** — Thessaloniki, Greece
Aristotle University of Thessaloniki
Physics
A 4-year studies program with one year study direction in electronics
Degree: 7.33/10

PUBLICATIONS

Journal Article — **Intel Stratix 10 FPGA design for track reconstruction for the ATLAS experiment at the HL-LHC**, A. Camplani et. al., *Journal of Instrumentation*, doi 10.48550/arXiv.2302.13609

Other Interests

- Bass
- Chess
- Climbing
- Travels
- Movies
- Books

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References

References available after request

SOFTWARE

FPGA	**Aldec ActiveHDL / RivieraPro** **GHDL** **Vunit framework** **Modelsim/Questasim** **Vivado/Quartus**
Microprocessors	**Atmel Studio**
Embedded Systems	**Rasbian**
Analog design	**Cadence Virtuoso**

</> PROGRAMMING LANGUAGES

- **Python**: Intermediate
- **Embedded C**: Intermediate
- **Java**: Basic
- **C/C++**: Basic

CONFERENCES AND WORKSHOPS

IELTS

- IELTS Language Certificate, band 7.0/9.0 (*British Council, 2019*)

XILINX

- Professional Zynq Ultrascale+ MPSoC (*PLC2, 2023*)