

Tung Thanh Le

710 W 148th St, Gardena, CA 90247, USA

<http://ttungl.github.io/>

Work Phone: 323-416-9214

Email: ttungl@gmail.com

Research Interests

- Computer architecture for many-core systems. Scalable, interconnect networks in distributed systems.
- Optimization. Machine learning. Cloud computing.

Education

University of Louisiana at Lafayette

September 2013 – Present

Ph.D. candidate, **Computer Science** (expected: Dec 2017)

Advisors: Prof. Danella Zhao, Prof. Magdy A. Bayoumi

Dissertation: **Optimizing Network-On-Chip designs for Heterogeneous Many-core Architectures**

M.S., **Computer Science**, Dec 2016

M.E., IT Convergence Engineering

School of **Electronic Engineering**

Kumoh National Institute of Technology

September 2011 – June 2013

B.E., with graduation thesis distinction, Automatic Control

School of **Electrical Engineering**

Danang University of Technology

September 2002 – June 2007

Professional Work Experience

University of Louisiana at Lafayette, LA, Graduate Assistantship, August 2013 - present

Hanwha Thales (former: Samsung Thales), South Korea, **Research Intern**, August 2013 – December 2013

Orion Technologies Co., South Korea, **Summer Intern**, June 2012 – August 2012

Unilab, Danang Univ. of Tech., Vietnam, **Software Engineer**, May 2008 – August 2011

Acronics Systems Inc., CA, USA, **PCB Engineer**, June 2007 – April 2008

Honors & Awards

- Graduate Teaching Assistantship, Fall 2015 - Present
- NSF Graduate Research Fellowship, August 2013 – August 2015
- Best Paper Award – 14th Conference on Electronics & Information Communications, 2012
- NIPA scholarship and NRF scholarship, South Korea, September 2011 – June 2013
- Samsung Thales scholarship for student travel, December 2012
- Excellent student in Danang University of Technology, January 2004 – June 2007
- One of four honor students achieving highest score on graduation thesis (4/500), June 2007

Selected publications

- Efficient Reconfigurable Global Network-on-chip Designs towards Heterogeneous CPU-GPU Systems: An Application-Aware Approach – *ISVLSI* 2017
- An Efficient Throughput Improvement through Bandwidth Awareness in Cognitive Radio Networks – *Journal of Comm. Networks*, 2014

Projects

- **HeteroArchGen4M2S**: An automatic software for configuring and running heterogeneous CPU-GPU architectures (HSA) on Multi2Sim simulator. This tool is built on top of M2S simulator, it allows us to configure different HSA (e.g., #CPUs, #GPUs, L1\$, L2\$, memory, network topologies, etc). The output files include the results of network throughput and latency, and dynamic power of the cores.

- **Pingo'in** – *Android Application*

This android app is created by using a Google maps API. You can build your list of points of interest (POI) on the Google's map, then the application will scan your map within the preset radius, if your POIs are within this radius, they will be displayed on your screen. Used Java, Eclipse for building the app, and used SVN for merging the code project.

- **New Cinema Booking System** – *Database Systems*

Designed the database system using ER-diagram. Used MySQL and PHP to build the online booking system. Two modes for admin and users.

- **Price Dropping Looker**: A tool for looking into the price dropped of the Amazon's items. Your wish-list items on Amazon will be alerted via your email if those prices are dropped below your expected price, the ratings and number of reviews also are taken into account.

- **Multi-class inheritance** – *Scheme Language*

Used Scheme language to modify the interpreter for creating new functions of the language. In this work, multi-class inheritance function is created. New instance generated is inherited to all the methods from joined classes. Used Scheme language for implementation.

- **802.11 DCF MAC Protocol simulation** – *Wireless Networking*

Implemented a 802.11 DCF MAC Protocol operation with Gilbert-Elliott channel model, RTS/CTS exchange, in different network topologies. Used C++ for implementation.

- **FPGA, ALU-16bits design** – *Computer Architecture*

Designed an ALU-16bits with basic operations using VHDL, Xilinx ISE and ModelSim. Verified by using Xilinx Spartan 3E FPGA.

- **Online Courses: Machine Learning** (Coursera-License#: 7MMK9BZBASXN); **Java Multithreading** (Udemy-License#: UC-TBSY47EV);

Deep Learning by Google Brain (Udacity)

Computer skills

Expertise with **Java**, **Python**, **Tensorflow**, **C/C++**, **MATLAB**, **Assembly**;

Fluency with **PHP**, **MySQL**, **HTML**, **Scheme**, **R**, **CPLX/AMPL**, **Verilog**, **VHDL**, **LaTeX**.