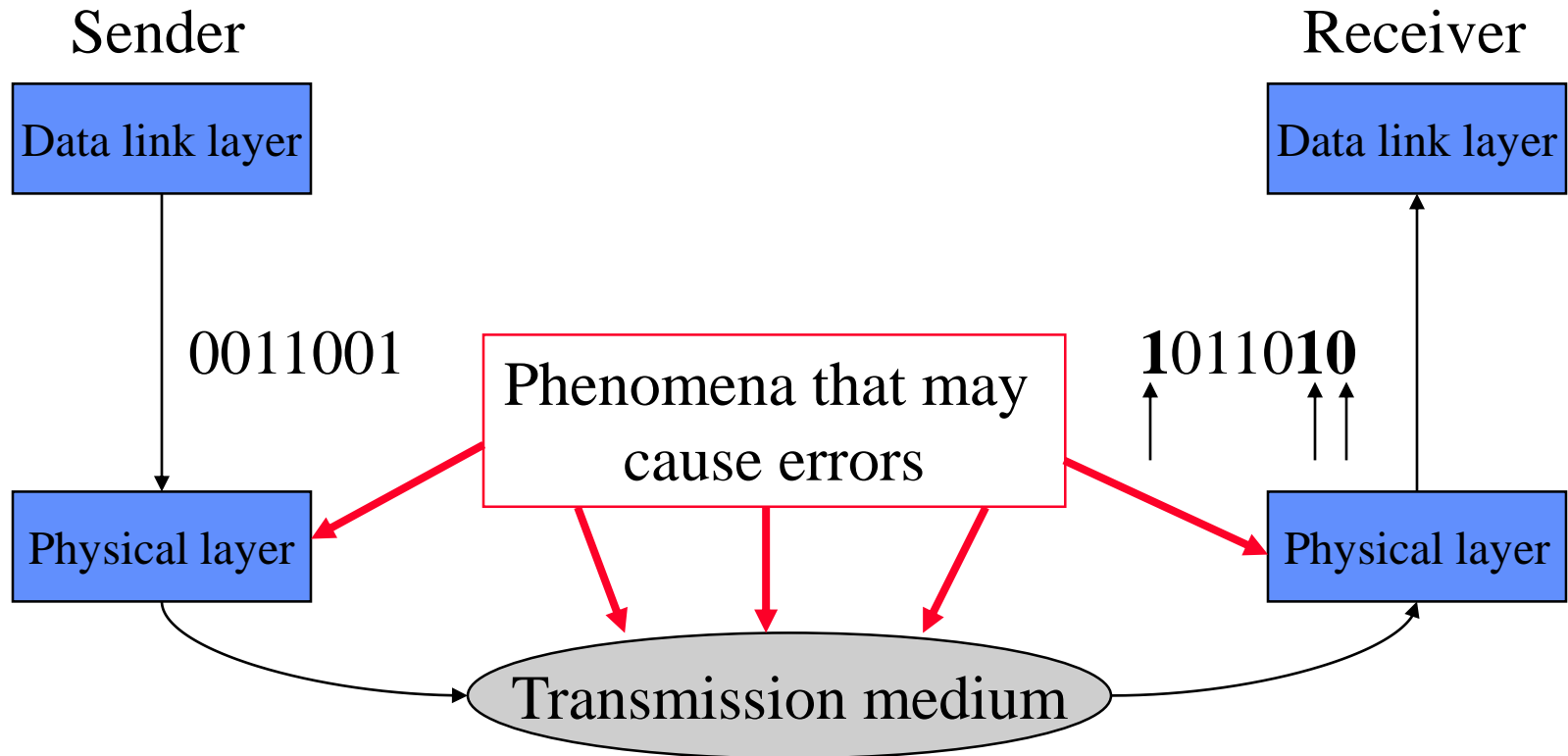


1. Introduction
2. Local Area Networking
- 3. Error Control and Retransmission Protocols**
4. Architectural Principles of the Internet
5. Flow Control in Internet: TCP
6. Routing Algorithms
7. Routing Protocols
8. The principles of ATM
9. Traffic Management in ATM
10. Scheduling
11. Quality of Service
12. Quality of Service routing
13. Peer-to-peer networks



Three ways to deal with errors after detection:

Retransmission

ARQ/TCP

- infrequent errors
- when time permits

Forward Error Correction

real-time services

- frequent errors
- when time does not permit retransmissions

Discard (!)

UDP

- when strict reliability is not required/too expensive

Principle of Error Detection

- message M : k bits
- an operation O on M gives result R ($n-k$ bits)
- sender transmits **codeword** C (n bits) consisting of M and R : $C = (M, R)$
- receiver checks received codeword $C^* = (M^*, R^*)$ by operation O on M^* which gives R^{**}
- if ($R^* = R^{**}$) then
 - receiver assumes that $M^* = M$ and $R^* = R$:
error-free transmission (**not sure!**)
 - else
transmission errors (**sure**)

Fast error detection

- The operation O should be fast to compute:
 - The result R should contain only a small number of bits
 - But, the check should give sufficient guarantee that, if $R^* \neq R$, then it is very likely that $M^* \neq M$

Error Detection: Single Parity Check

- Operation O: addition k message bits mod 2
- Sender:
 - append $R = \text{sum of message bits mod } 2$
 - e.g. [0110100] becomes [0110100 | 1]
 - transmit
- Receiver (single parity check):
 - compute sum R^* of received codeword C^* bits mod 2
 - if $R^* = 0$,
 - no errors
 - else error(s)

0	\oplus	0	=	0
0	\oplus	1	=	1
1	\oplus	0	=	1
1	\oplus	1	=	0

Single bit error is detected

Horizontal & Vertical Parity Checks

1	0	0	1	1	0	0	1
0	1	0	1	0	0	1	1
1	0	0	1	1	1	0	0
0	1	0	0	1	0	0	0
1	0	0	1	0	0	0	0
1	0	0	0	1	1	1	0

Horizontal
checks

Vertical
checks

Parity Check Codes

or “Linear Codes”

s_1	s_2	s_3	c_1	c_2	c_3	c_4
0	0	0	0	0	0	0
1	0	0	1	1	1	0
0	1	0	0	1	1	1
0	0	1	1	1	0	1
1	1	0	1	0	0	1
1	0	1	0	0	1	1
0	1	1	1	0	1	0
1	1	1	0	1	0	0

$$c_1 = s_1 + s_3$$

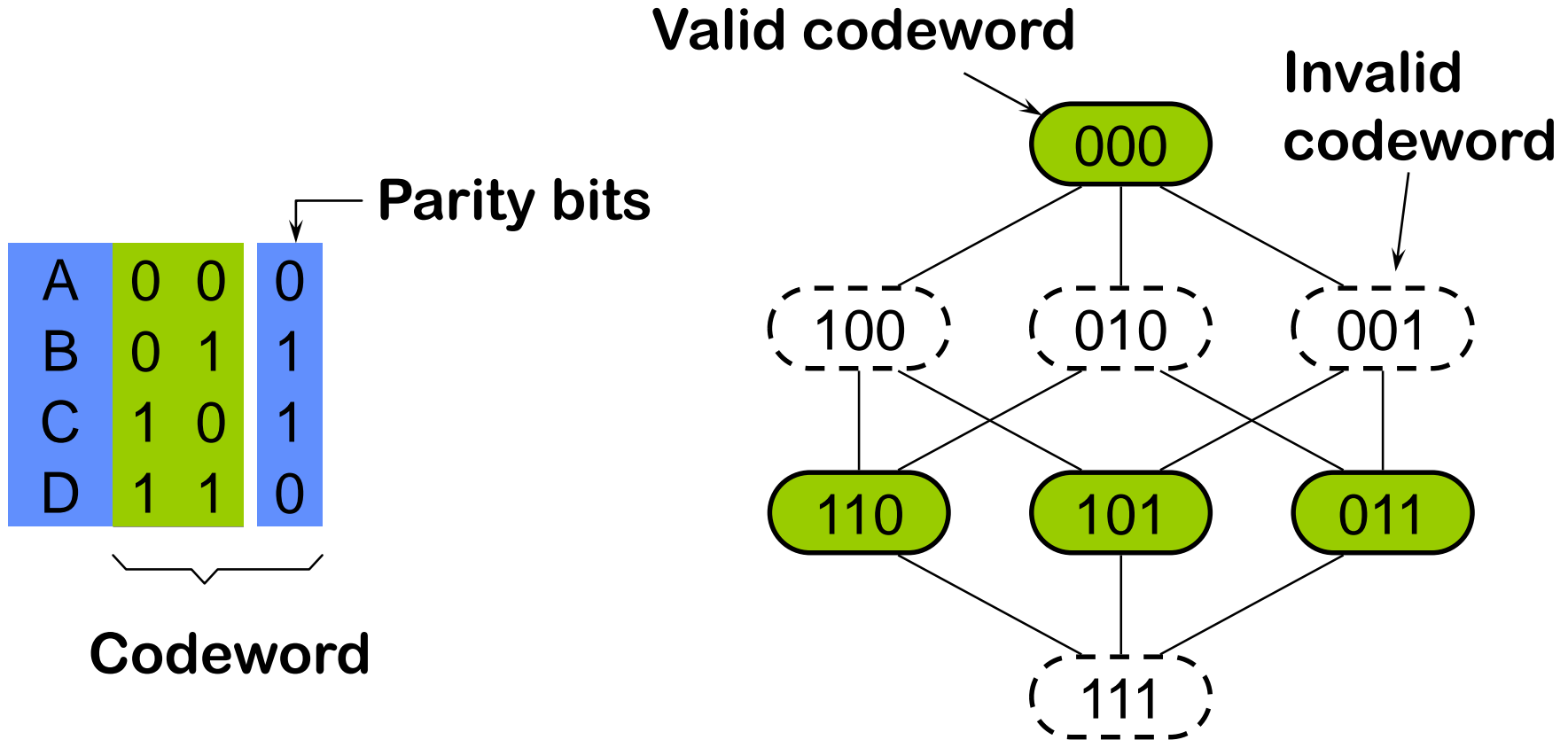
$$c_2 = s_1 + s_2 + s_3$$

$$c_3 = s_1 + s_2$$

$$c_4 = s_2 + s_3$$

$$d=4$$



























Hamming distance



Hamming distance = 2

Error detection and correction

Minimum distance for error-detecting and error-correcting codes

Hamming distance	 valid codeword  invalid codeword	error detection	error correction
1	 — 	0	0
2	 —  — 	1	0
3	 —  —  — 	2	1
4	 —  —  —  — 	3	1
5	 —  —  —  —  — 	4	2
d	 —  — ... —  — 	$d - 1$	$\left\lfloor \frac{d - 1}{2} \right\rfloor$

To detect d errors : distance $\geq d + 1$

To correct d errors: distance $\geq 2d + 1$

Modulo 2 Arithmetic

Modulo 2 arithmetic...

[same as “*exclusive or*” (*XOR*)]

$$0 \oplus 0 = 0$$

$$0 \oplus 1 = 1$$

$$1 \oplus 0 = 1$$

$$1 \oplus 1 = 0$$

Examples:

$$\oplus \begin{array}{r} 10001011 \\ 10100010 \\ \hline 00101001 \end{array}$$

and

$$\oplus \begin{array}{r} 10001011 \\ 10001011 \\ \hline 00000000 \end{array}$$

Is not addition in base 2!

Base 2 : 10 + 11 = 101

Modulo 2 without carry: 10 + 11 = 01

Addition modulo 2 = subtraction modulo 2

Cyclic Redundancy Check (CRC)

Given: M : 1010101010

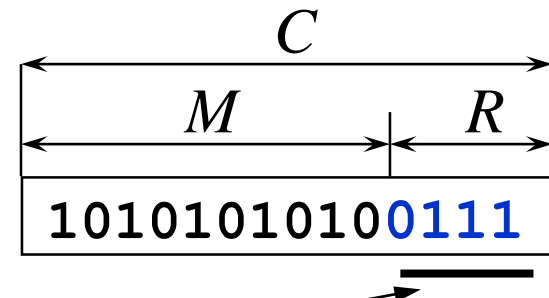
G : 10111

Solution: $r + 1 = 5 \Rightarrow r = 4$

$M \cdot 2^r = 10101010100000$

$$\begin{array}{r}
 10101010100000 \\
 \underline{10111} \\
 10010 \\
 \underline{10111} \\
 10110 \\
 \underline{10111} \\
 10000 \\
 \underline{10111} \\
 111
 \end{array}
 \quad
 \begin{array}{r}
 10111 \\
 \hline
 1001010001 = Q
 \end{array}$$

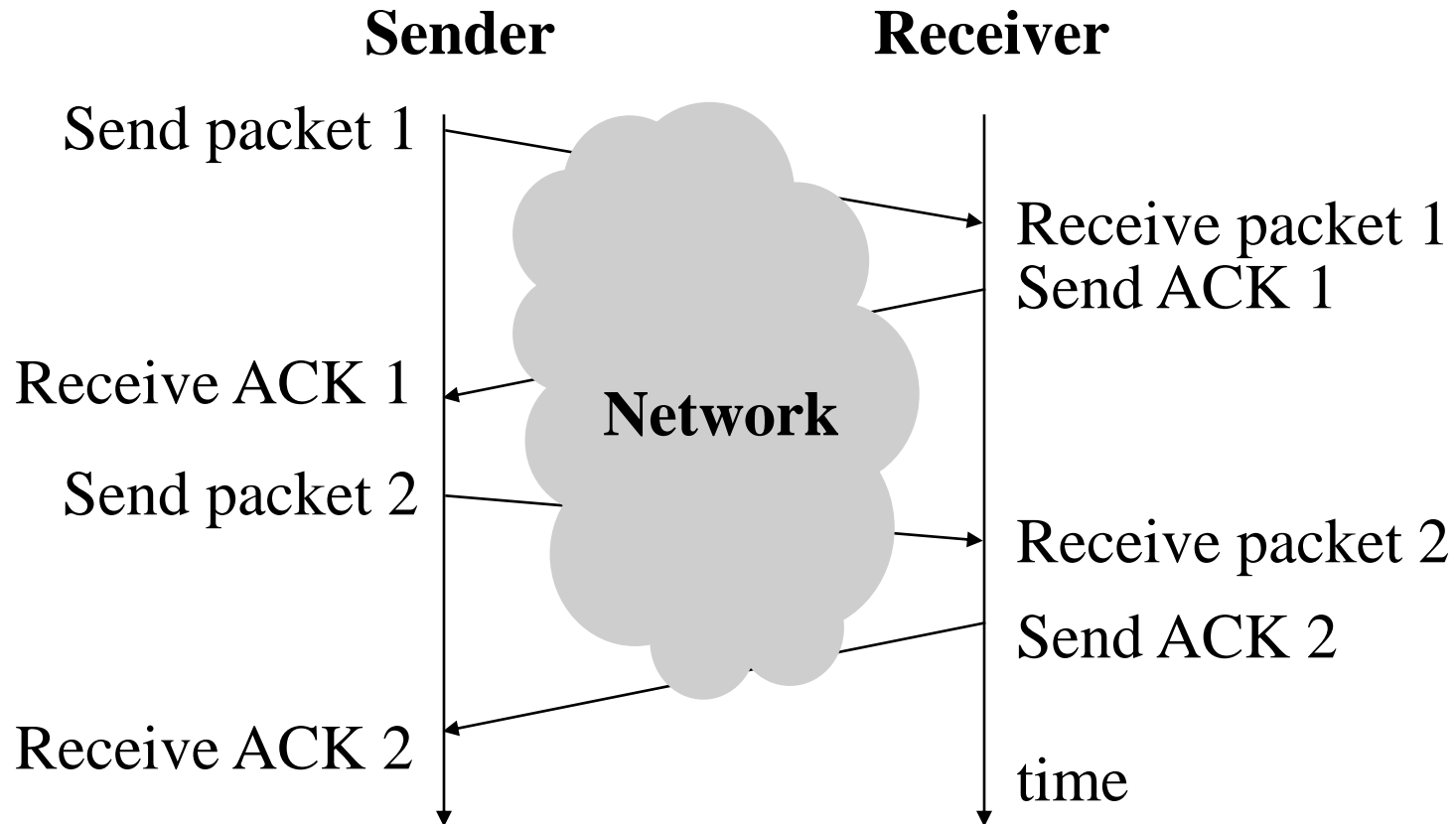
$111 = R \Rightarrow \text{CRC} = 0111$



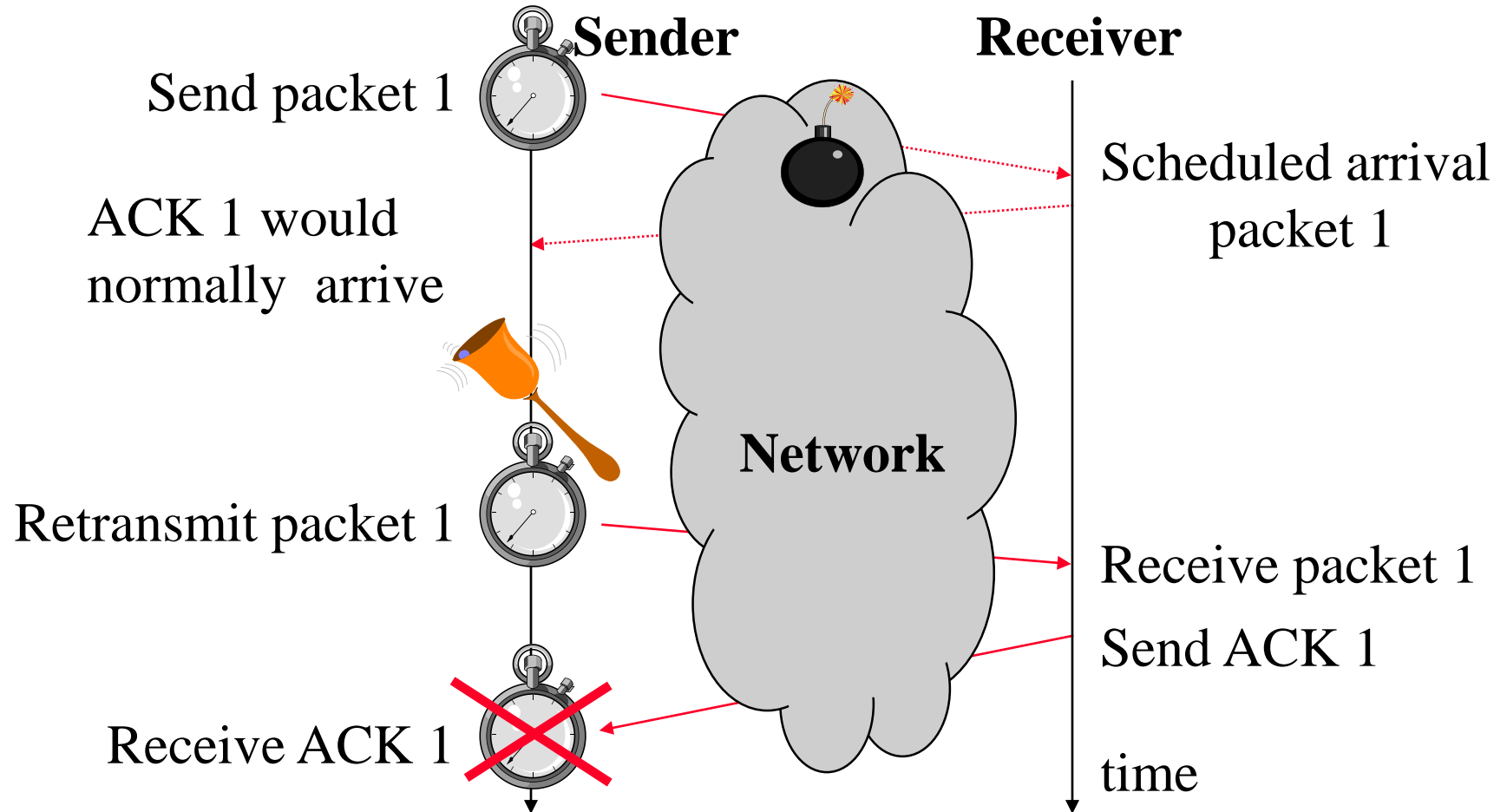
Goal: Implement reliable packet channel
over an unreliable one

Approach: Use timers, acknowledgments &
retransmits

Acknowledgment Scheme

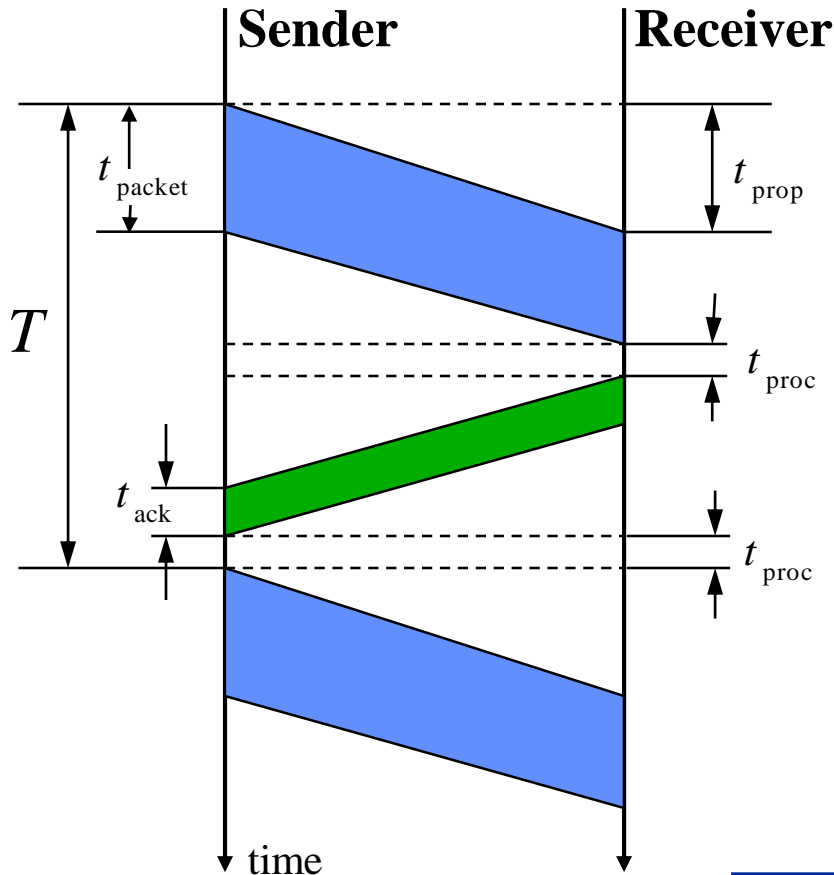


Time-out and Retransmission



- Automatic Repeat Request (ARQ) protocols:
Error detection and retransmission
 - Stop-and-Wait protocol
 - Go Back n protocol
 - Selective Repeat protocol
- Efficiency:
$$\frac{\text{Maximum average rate (throughput)}}{\text{Link rate}}$$

Stop-and-Wait Protocol: Efficiency



No errors: $\eta_{S \& W} = \frac{R_{S \& W}}{C}$

Maximum effective information rate:

$$R_{S \& W} = \frac{l_{\text{packet}} - l_{\text{header}}}{T}$$

$$t_{\text{packet}} = \frac{l_{\text{packet}} \text{ (bits)}}{C \text{ (bits/s)}}, \quad t_{\text{ack}} = \frac{l_{\text{ack}} \text{ (bits)}}{C \text{ (bits/s)}}$$

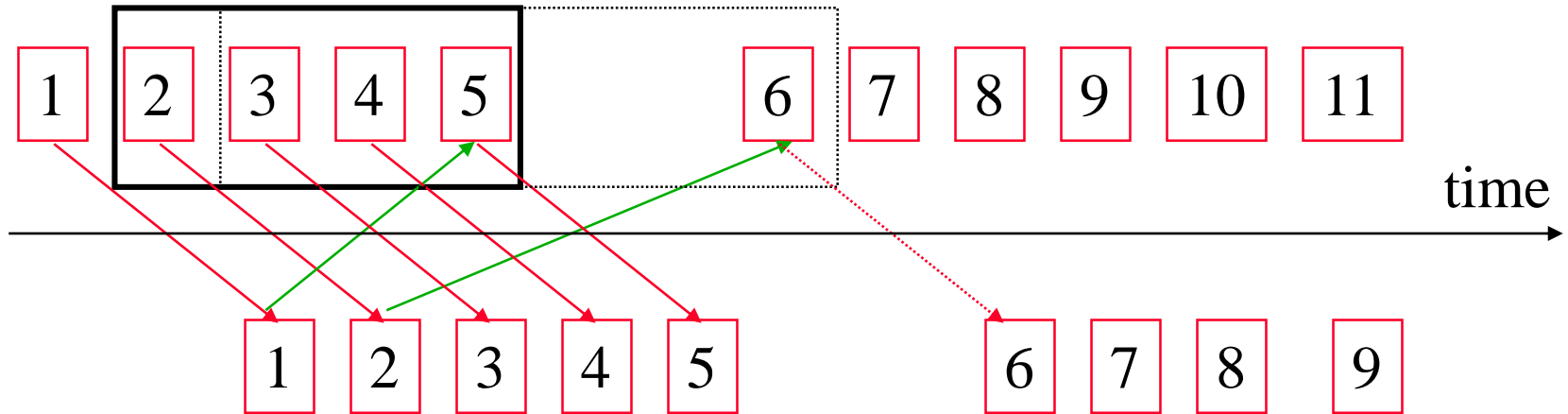
Round-Trip Time T

$$T = 2 \times t_{\text{prop}} + 2 \times t_{\text{proc}} + t_{\text{packet}} + t_{\text{ack}}$$

Combined:

$$\eta_{S \& W} = \frac{1 - \frac{l_{\text{header}}}{l_{\text{packet}}}}{1 + \frac{l_{\text{ack}}}{l_{\text{packet}}} + \frac{2C(t_{\text{prop}} + t_{\text{proc}})}{l_{\text{packet}}}}$$

Sliding Window Size

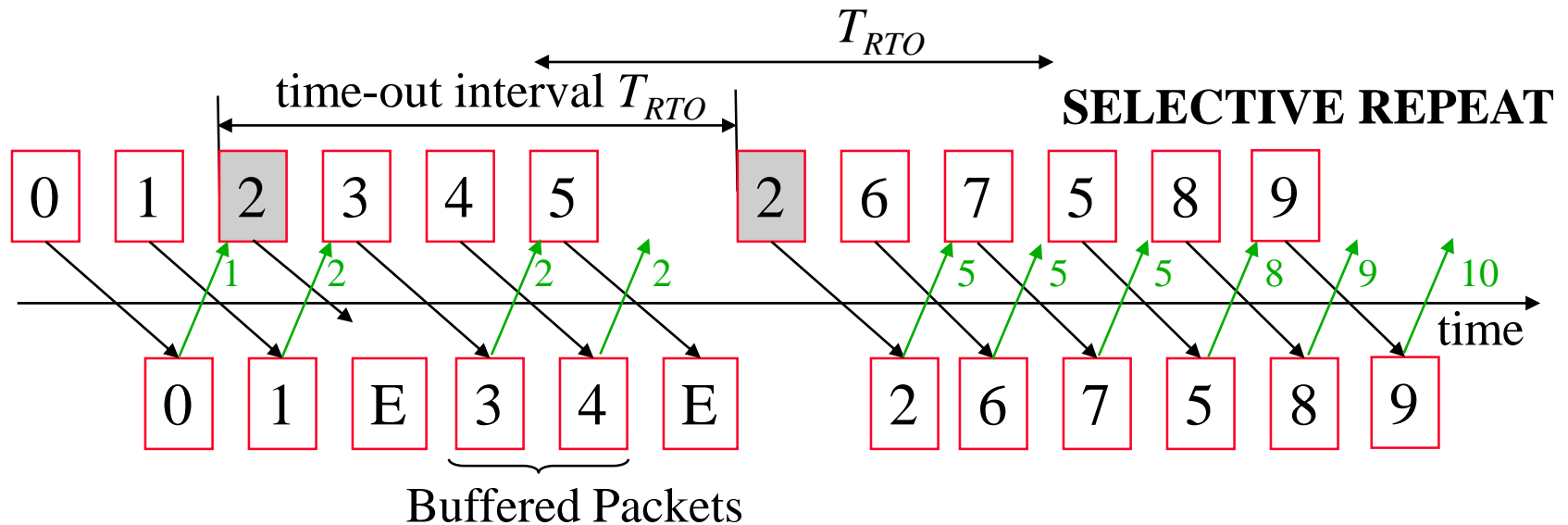
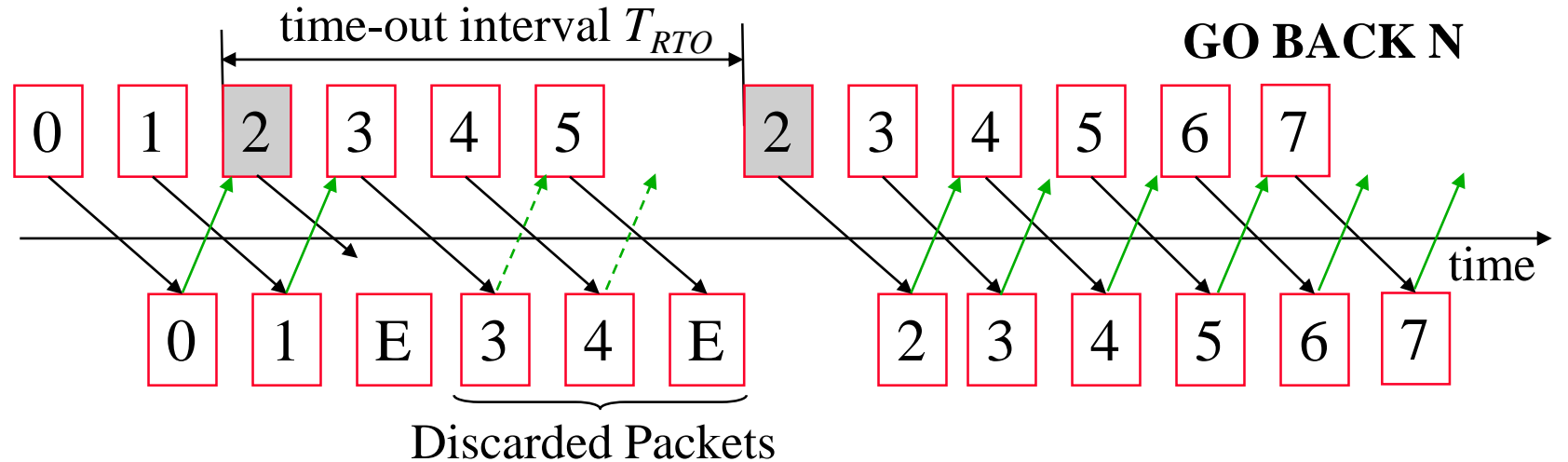


Tuning sliding window impacts number of packets in network



Flow control mechanism: optimal throughput

Sliding Window Strategies



- Explain how to compute a cyclic redundancy check.
- Explain the Selective Repeat ARQ protocol and the purpose of ARQ.