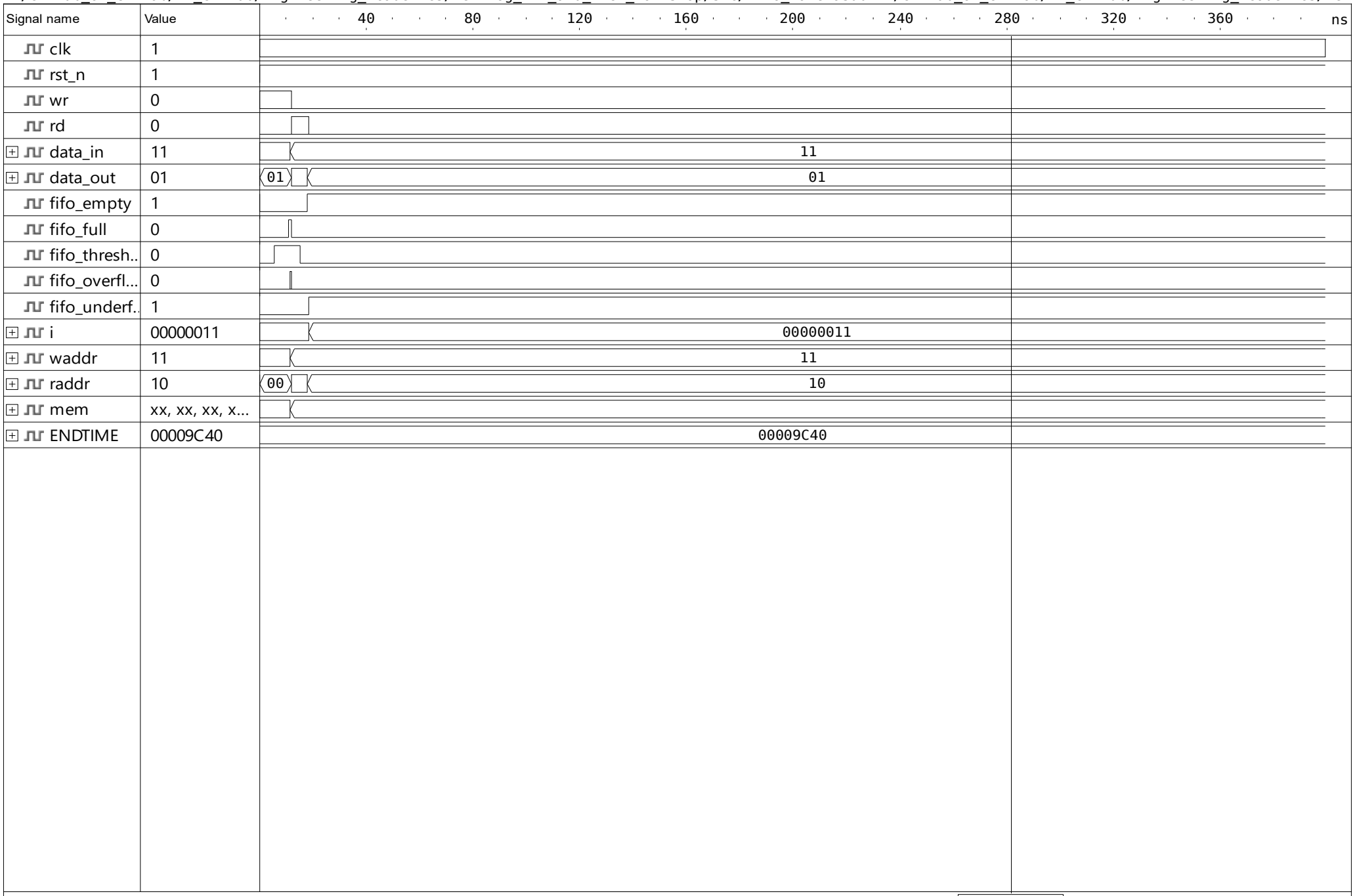
D:/Github_or_Gitlab/MY_Github/Engineering_Academics/Verilog_HDL_and_FPGA_Workshop/src/FIFO_Wave.asdb D:/Github_or_Gitlab/MY_Github/Engineering_Academics/Ver



1/1 (0 ps - 409.87 ns)